

## MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch MM54C374/MM74C374 TRI-STATE Octal D-Type Flip-Flop

### General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE outputs. These outputs have been specially designed to drive high capacitive loads, such as one might find when driving a bus, and to have a fan out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When LATCH ENABLE is high, the Q outputs will follow the D inputs. When LATCH ENABLE goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until LATCH ENABLE returns high again.

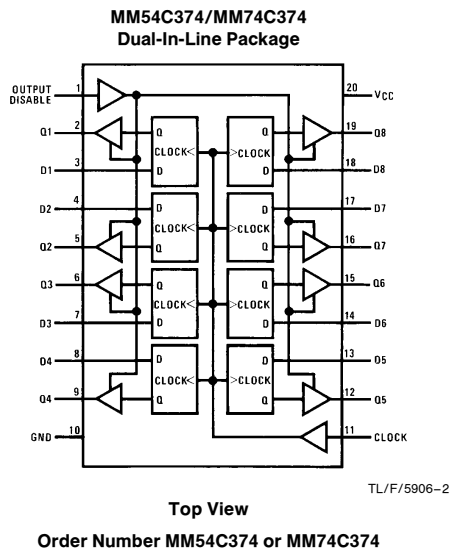
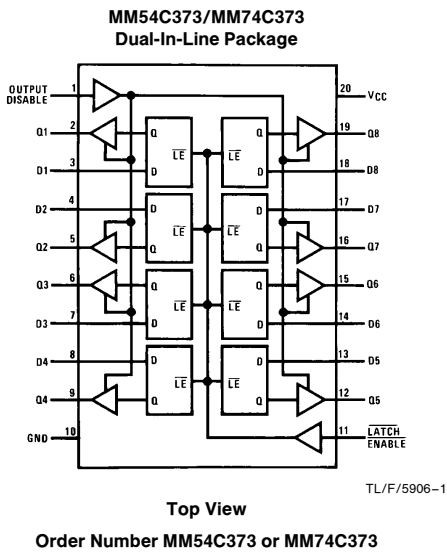
The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

### Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V<sub>CC</sub> (typ.)
- Low power consumption
- TTL compatibility Fan out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/LATCH ENABLE and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

### Connection Diagrams



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MM54C373/MM74C373 TRI-STATE Octal D-Type Latch  
MM54C374/MM74C374 TRI-STATE Octal D-Type Flip-Flop

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range ( $T_A$ )	
MM54C373	-55°C to +125°C
MM74C373	-40°C to +85°C
Storage Temperature Range ( $T_S$ )	-65°C to +150°C

Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating $V_{CC}$ Range	3V to 15V
Absolute Maximum $V_{CC}$	18V
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

### DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$ $V_{CC} = 10V, I_O = 10 \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
$I_{OZ}$	TRI-STATE Leakage Current	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	-1.0	0.005 -0.005	1.0	$\mu A$ $\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	300	$\mu A$
<b>CMOS/LPTTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$		$V_{CC} - 1.5$ $V_{CC} - 1.5$		V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 54C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V, I_O = -360 \mu A$ 74C $V_{CC} = 4.75V, I_O = -360 \mu A$ 54C $V_{CC} = 4.5V, I_O = -1.6 mA$ 74C $V_{CC} = 4.75V, I_O = -1.6 mA$	$V_{CC} - 0.4$ $V_{CC} - 0.4$ 2.4 2.4			V V V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V, I_O = 1.6 mA$ 74C $V_{CC} = 4.75V, I_O = 1.6 mA$			0.4 0.4	V V
<b>OUTPUT DRIVE (Short Circuit Current)</b>						
$I_{SOURCE}$	Output Source Current	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25^\circ C$ (Note 4)	-12	-24		mA
$I_{SOURCE}$	Output Source Current	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$ (Note 4)	-24	-48		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$ (Note 4)	6	12		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$ (Note 4)	24	48		mA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

### AC Electrical Characteristics\*

MM54C373/MM74C373,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 20\text{ ns}$ , unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0}$ , $t_{pd1}$	Propagation Delay, LATCH ENABLE to Output	$V_{CC} = 5\text{V}$ , $C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		165 70 195 85	330 140 390 170	ns ns ns ns
$t_{pd0}$ , $t_{pd1}$	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}} = V_{CC}$ $V_{CC} = 5\text{V}$ , $C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		155 70 185 85	310 140 370 170	ns ns ns ns
$t_{SET-UP}$	Minimum Set-Up Time Data In to $\overline{\text{CLOCK/LATCH ENABLE}}$	$t_{HOLD} = 0\text{ ns}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		70 35	140 70	ns ns
$f_{MAX}$	Maximum LATCH ENABLE Frequency	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	3.5 4.5	6.7 9.0		MHz MHz
$t_{PWH}$	Minimum LATCH ENABLE Pulse Width	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		75 55	150 110	ns ns
$t_r$ , $t_f$	Maximum LATCH ENABLE Rise and Fall Time	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		NA NA		$\mu\text{s}$ $\mu\text{s}$
$t_{H1}$ , $t_{H0}$	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10\text{k}$ , $C_L = 5\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		105 60	210 120	ns ns
$t_{H1}$ , $t_{H0}$	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10\text{k}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		105 45	210 90	ns ns
$t_{THL}$ , $t_{TLH}$	Transition Time	$V_{CC} = 5\text{V}$ , $C_L = 50\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		65 35 110 70	130 70 220 140	ns ns ns ns
$C_{LE}$	Input Capacitance	$\overline{\text{LE}}$ Input (Note 2)		7.5	10	pF
$C_{OD}$	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
$C_{IN}$	Input Capacitance	Any Other Input (Note 2)		5	7.5	pF
$C_{OUT}$	Output Capacitance	High Impedance State (Note 2)		10	15	pF
$C_{PD}$	Power Dissipation Capacitance	Per Package (Note 3)		200		pF

\*AC Parameters are guaranteed by DC correlated testing.

## AC Electrical Characteristics\* (Continued)

MM54C374/MM74C374, T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, t<sub>r</sub> = t<sub>f</sub> = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay, CLOCK to Output	V <sub>CC</sub> = 5V, C <sub>L</sub> = 50 pF V <sub>CC</sub> = 10V, C <sub>L</sub> = 50 pF V <sub>CC</sub> = 5V, C <sub>L</sub> = 150 pF V <sub>CC</sub> = 10V, C <sub>L</sub> = 150 pF		150 65 180 80	300 130 360 160	ns ns ns ns
t <sub>SET-UP</sub>	Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE	t <sub>HOLD</sub> = 0 ns V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V		70 35	140 70	ns ns
t <sub>PWH</sub> , t <sub>PWL</sub>	Minimum CLOCK Pulse Width	V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V		70 50	140 100	ns ns
f <sub>MAX</sub>	Maximum CLOCK Frequency	V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V	3.5 5	7.0 10		MHz MHz
t <sub>1H</sub> , t <sub>0H</sub>	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	R <sub>L</sub> = 10k, C <sub>L</sub> = 50 pF V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V		105 60	210 120	ns ns
t <sub>H1</sub> , t <sub>H0</sub>	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	R <sub>L</sub> = 10k, C <sub>L</sub> = 50 pF V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V		105 45	210 90	ns ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time	V <sub>CC</sub> = 5V, C <sub>L</sub> = 50 pF V <sub>CC</sub> = 10V, C <sub>L</sub> = 50 pF V <sub>CC</sub> = 5V, C <sub>L</sub> = 150 pF V <sub>CC</sub> = 10V, C <sub>L</sub> = 150 pF		65 35 110 70	130 70 220 140	ns ns ns ns
t <sub>r</sub> , t <sub>f</sub>	Maximum CLOCK Rise and Fall Time	V <sub>CC</sub> = 5V V <sub>CC</sub> = 10V	15 5	>2000 >2000		μs μs
C <sub>CLK</sub>	Input Capacitance	CLOCK Input (Note 2)		7.5	10	pF
C <sub>OD</sub>	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C <sub>IN</sub>	Input Capacitance	Any Other Input (Note 2)		5	7.5	pF
C <sub>OUT</sub>	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C <sub>PD</sub>	Power Dissipation Capacitance	Per Package (Note 3)		250		pF

\*AC Parameters are guaranteed by DC correlated testing.

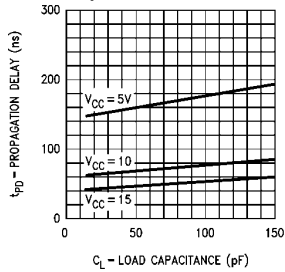
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

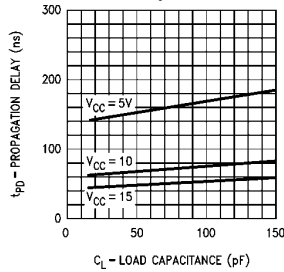
**Note 4:** These are peak output current capabilities. Continuous output current is rated at 12 mA max.

## Typical Performance Characteristics $T_A = 25^\circ\text{C}$

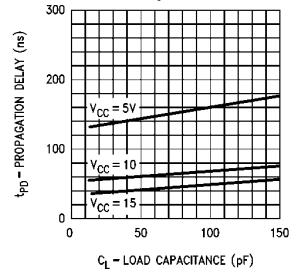
**MM54C373/MM74C373**  
Propagation Delay, LATCH  
ENABLE to Output vs Load  
Capacitance



**MM54C373/MM74C373**  
Propagation Delay,  
Data In to Output  
vs Load Capacitance

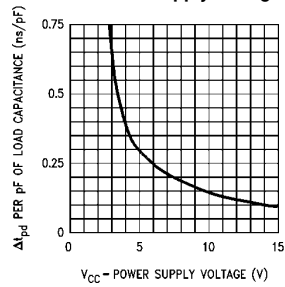


**MM54C374/MM74C374**  
Propagation Delay,  
CLOCK to Output  
vs Load Capacitance

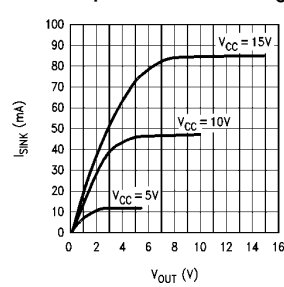


TL/F/5906-3

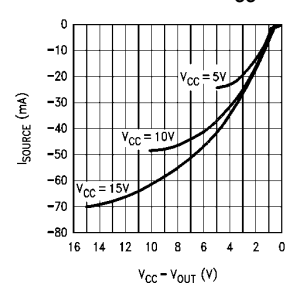
**MM54C373/MM74C373,**  
**MM54C374/MM74C374**  
Change in Propagation Delay per  
pF of Load Capacitance ( $\Delta t_{PD}/\text{pF}$ )  
vs Power Supply Voltage



**MM54C373/MM74C373,**  
**MM54C374/MM74C374**  
Output Sink Current vs  $V_{OUT}$



**MM54C373/MM74C373,**  
**MM54C374/MM74C374** Output  
Source Current vs  $V_{CC} - V_{OUT}$



TL/F/5906-4

## Truth Table

**MM54C373/MM74C373**

Output Disable	LATCH ENABLE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

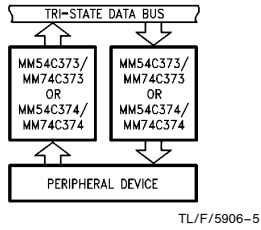
**MM54C374/MM74C374**

Output Disable	Clock	D	Q
L	$\nearrow$	H	H
L	$\searrow$	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

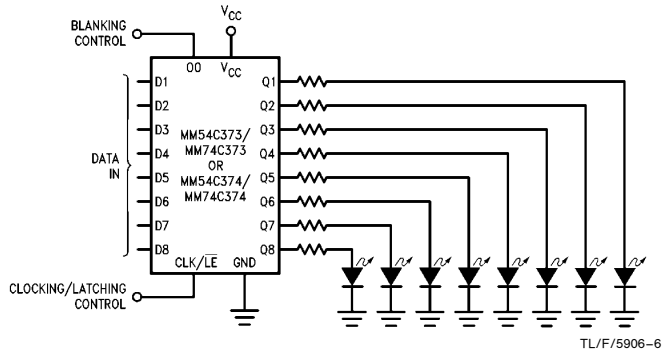
L = Low logic level  
H = High logic level  
X = Irrelevant  
 $\nearrow$  = Low to high logic level transition  
Q = Preexisting output level  
Hi-Z = High impedance output state

## Typical Applications

### Data Bus Interfacing Element

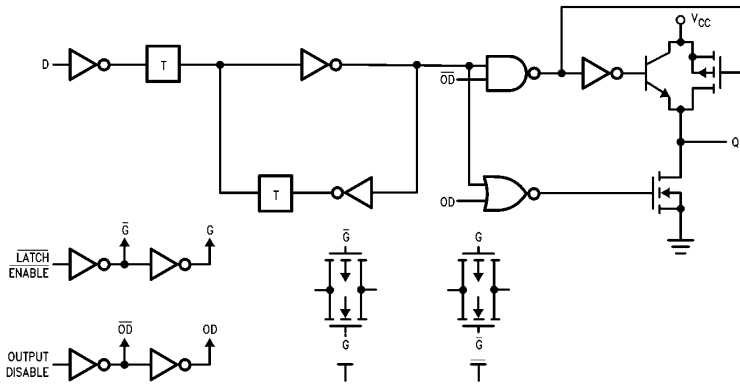


### Simple, Latching, Octal, LED Indicator Driver with Blanking for Use as Data Display, Bus Monitor, $\mu$ P Front Panel Display, Etc.

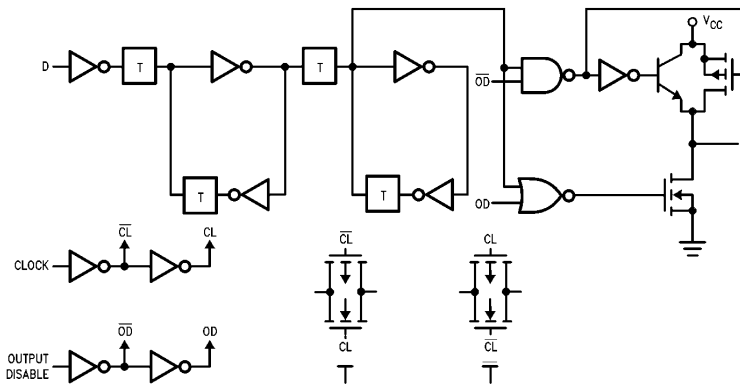


## Logic Diagrams

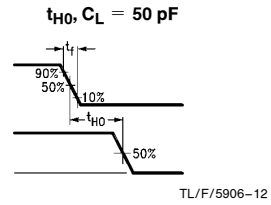
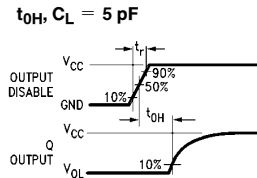
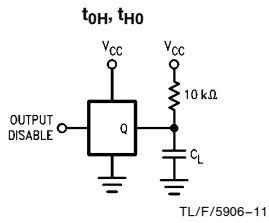
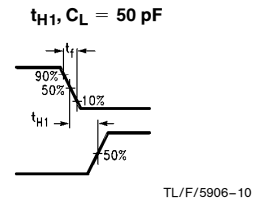
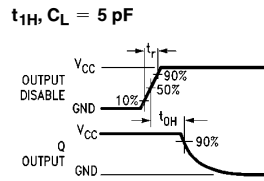
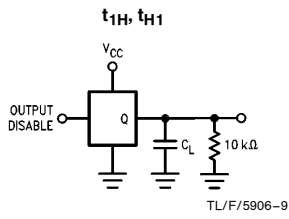
### MM54C373/MM74C373 (1 of 8 Latches)



### MM54C374/MM74C374 (1 of 8 Flip-Flops)

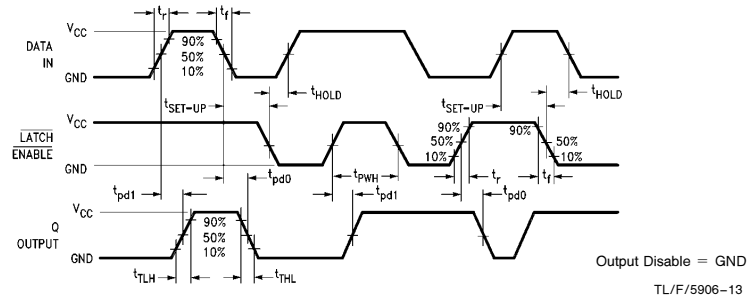


## TRI-STATE Test Circuits and Switching Time Waveforms

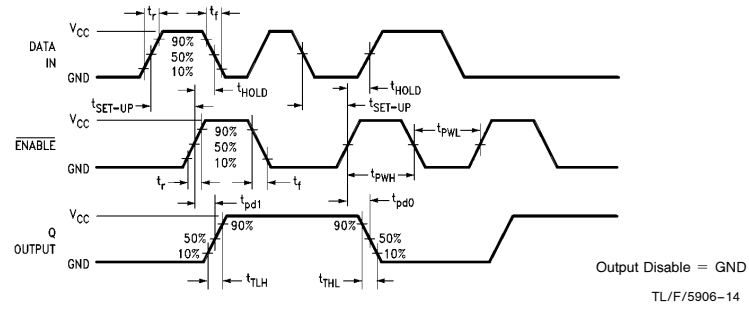


## Switching Time Waveforms

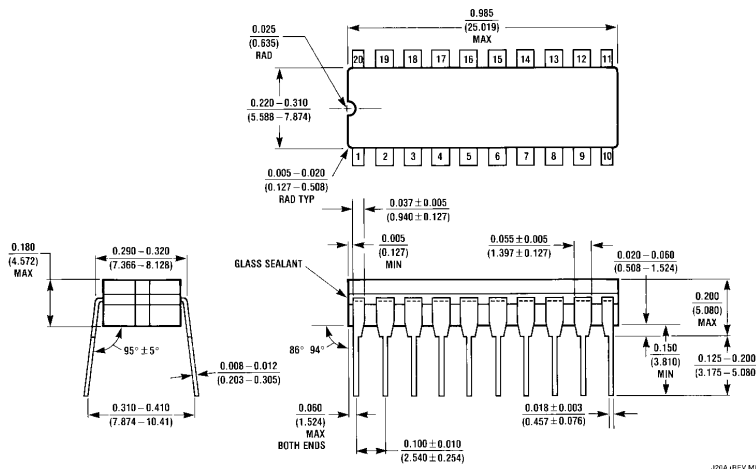
### MM54C373/MM74C373



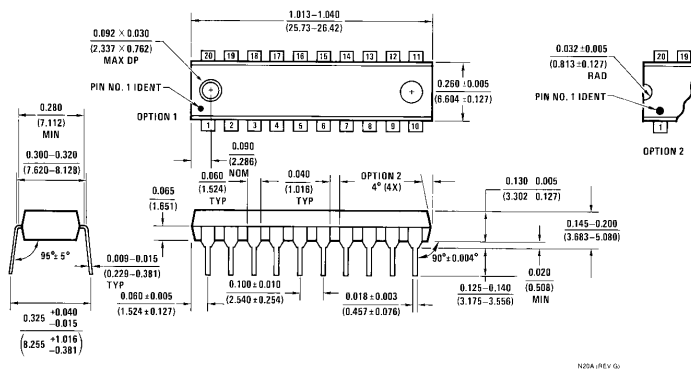
### MM54C374/MM74C374



**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
 Order Number MM54C373J, MM54C374J, MM74C373J or MM74C374J  
 NS Package Number J20A



**Molded Dual-In-Line Package (N)**  
 Order Number MM54C373N, MM54C374N, MM74C373N or MM74C374N  
 NS Package Number N20A

**LIFE SUPPORT POLICY**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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