National Semiconductor

DM54193 Synchronous Up/Down 4-Bit Binary Counter with Dual Clock

General Description

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counter to be used as modulo-N divider by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

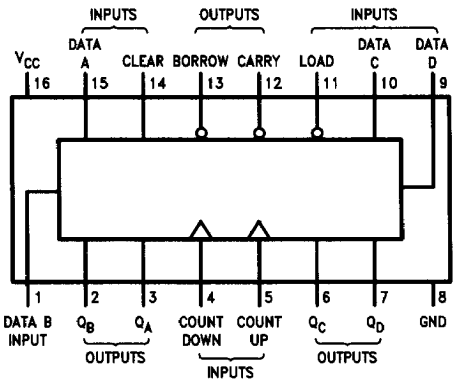
This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count up input when an overflow condition exists. The counter can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

Connection Diagram

Dual-In-Line Package



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Order Number DM54193J or DM54193W
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				16	mA
f_{CLK}	Clock Frequency (Note 4)		0	25	20	MHz
t_W	Pulse Width (Note 4)	Clock Low	30			ns
		Clock, Clear High Load Low	20			
t_{SU}	Data Setup Time (Note 4)		20			ns
t_H	Hold Time (Note 4)		0			ns
T_A	Free Air Operating Temperature		−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		65	89	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time.

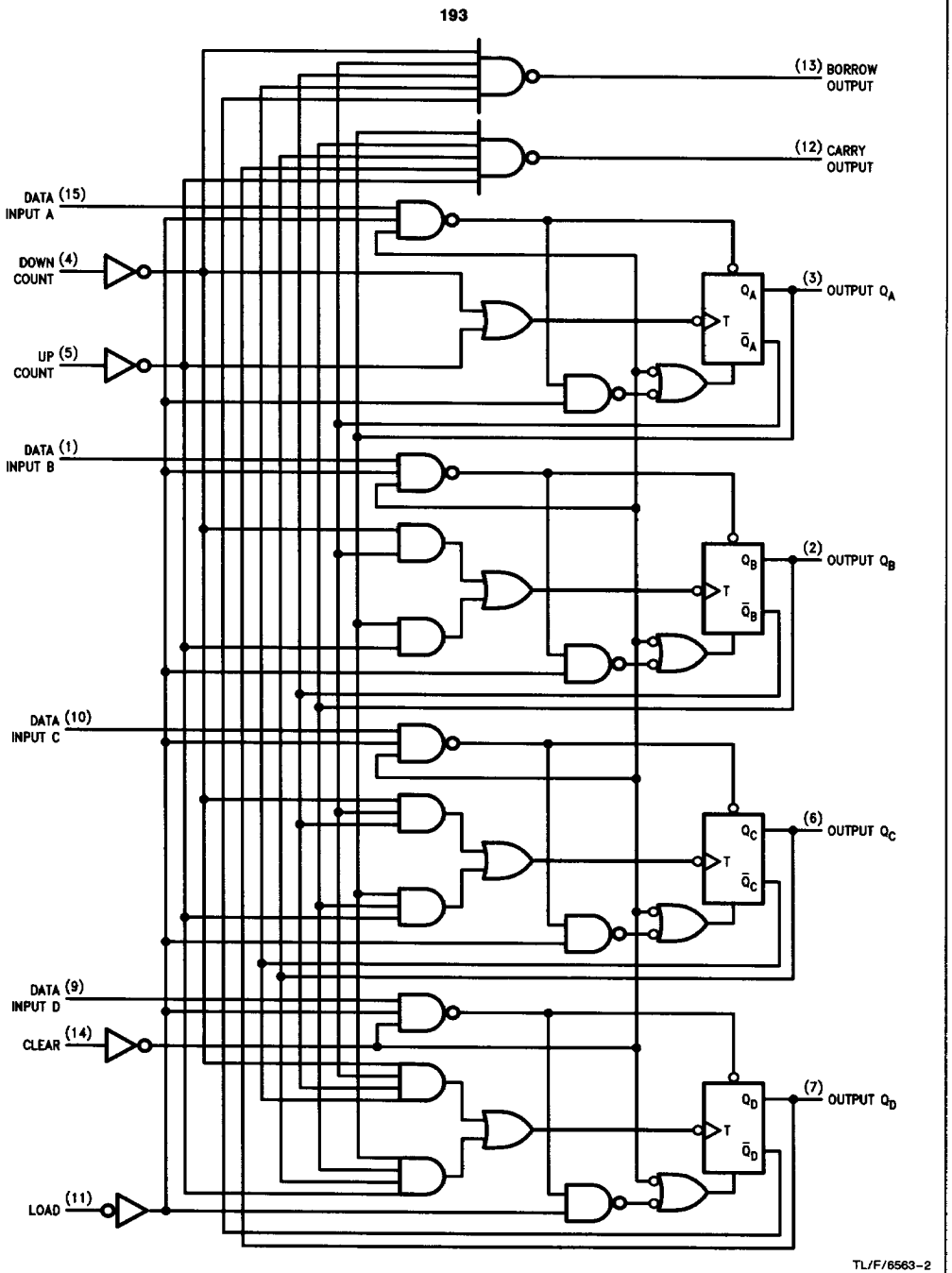
Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Up to Carry		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Up to Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Down to Borrow		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Down to Borrow		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Either Count to Q		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Either Count to Q		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Q		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Q		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35	ns

Logic Diagrams



Timing Diagram

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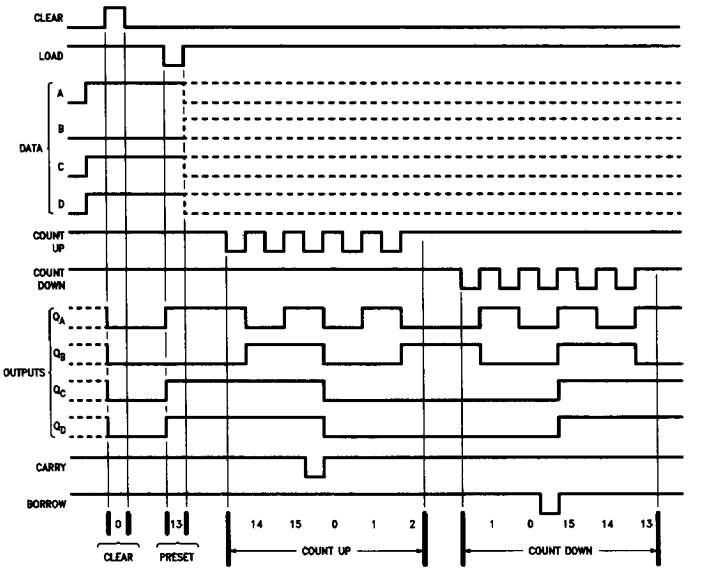
Typical Clear, Load, and Count Sequences



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Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high, when counting down, count-up input must be high.