



MM5387AA, MM53108 digital alarm clocks

general description

The MM5387AA, MM53108 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers with up to four display modes (time, seconds, alarm and sleep) to maximize circuit utility, but are specifically intended for clock-radio applications. Both devices will directly-drive 7-segment LED displays in either a 12 hour format (3½ digits) with lead-zero blanking, AM/PM indication and flashing colon, or 24 hour format (4 digits) through hard-wire pin selection; the timekeeping function operates from either a 50 or 60 Hz input, also through pin selection. Outputs consist of display drivers, sleep (e.g., timed radio turn-off), and alarm enable. A power-fail indication mode is provided to inform the user of incorrect time display by flashing all "ON" digits at a 1 Hz rate, and is cancelled by simply resetting time. The device operates over a supply range of 24–26V which does not require regulation.

The MM53108 is electrically identical to the MM5387AA, but with mirror-image pin-out to facilitate PC board layout when designing a "module" where the LED display and MOS chip are mounted on the same side; the MM5387AA is more suited for "L" shaped module designs (vertical LED display, horizontal component board). Both devices are supplied in a 40-lead dual-in-line package.

features

- 50 or 60 Hz operation
- Single power supply
- 12 or 24 hour display format
- AM/PM outputs
- Leading-zero blanking } 12 hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Elimination of illegal time display at turn "ON"
- Direct interface to LED displays
- 9-minute snooze alarm
- Presetable 59-minute sleep timer
- Available in standard (MM5387AA) or mirror image (MM53108) pin-out

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block diagram

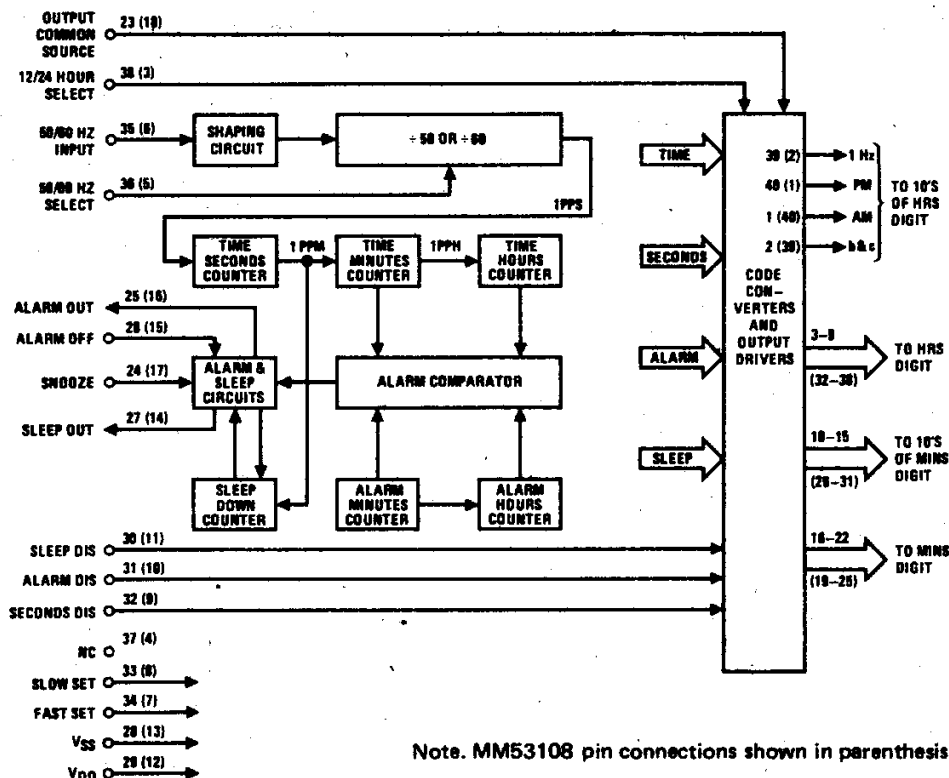


FIGURE 1

absolute maximum ratings

Voltage at Any Pin Except Segment Outputs	$V_{SS} + 0.3$ to $V_{SS} - 30V$
Voltage at Segment Outputs	$V_{SS} + 0.3$ to $V_{SS} - 15V$
Operating Temperature	$-25^{\circ}C$ to $+70^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

electrical characteristics

T_A within operating range, $V_{SS} = 24V-26V$, $V_{DD} = 0V$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	Output Driving Display	24		26	V
	Functional Clock	8		26	V
Power Supply Current	No Output Loads			4	mA
	$V_{SS} = 8V$			5	mA
	$V_{SS} = 26V$				
50/60 Hz Input					
Frequency Voltage	$V_{SS} = 8V$ to $26V$	dc	50 or 60	10k	Hz
Logical High Level		$V_{SS}-1$	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	$V_{DD}+2$	V
Input Leakage				100	μA
All Other Input Voltages					
Logical High Level		$V_{SS}-1$	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Load to V_{DD}	V_{DD}	V_{DD}	$V_{SS}-6$	V
Power Failure Detect Voltage	(V_{SS} Voltage), (Note 2)	1		7.5	V
Count Operating Voltage		8		26	V
Hold Count Voltage		(Note 2)		26	V
Output Current Levels	$V_{SS} = 24V$ to $26V$, Output Common = V_{SS}				
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level, Source	$V_{OH} = V_{SS} - 4V$	16			mA
Logical Low Level, Leakage	$V_{OL} = V_{SS} - 14V$			10	μA
1 Hz Display					
Logical High Level, Source	$V_{OH} = V_{SS} - 4$	24			mA
Logical Low Level, Leakage	$V_{OL} = V_{SS} - 14$			10	μA
All Other Displays					
Logical High Level, Source	$V_{OH} = V_{SS} - 4V$	8		(Note 1)	mA
Logical Low Level, Leakage	$V_{OL} = V_{SS} - 14V$			10	μA
Alarm and Sleep Outputs	$V_{SS} = 24V$				
Logical High, Source	$V_{OH} = V_{SS} - 2$	500			μA
Logical Low, Sink	$V_{OL} = V_{SS} - 2$	1			μA

Note 1: Segment output current must be limited to 11 mA maximum by user; power dissipation must be limited to 900 mW at $70^{\circ}C$ and 1.2W at $25^{\circ}C$.

Note 2: The power-fail detect voltage is 0.5V or more above the hold count voltage. The power-fail latch trips into power-fail mode at least 0.5V above the voltage at which data stored in the time latch is lost.

functional description

A block diagram of the MM5387AA, MM53108 digital clock radio circuit is shown in *Figure 1*. The various display setting modes are listed in Table I, and Table II shows the setting control functions. The following description is based on *Figure 1* and refers to both devices as they are electrically identical.

50 or 60 Hz Input: A shaping circuit (*Figure 3*) is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sine wave input. The circuit is a Schmitt trigger that is designed to provide about 6V of hysteresis. A simple RC filter such as shown in *Figure 7*, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving 50/60 Hz select unconnected; pull-down to VDD is provided by an internal depletion load. Operation at 50 Hz is programmed by connecting 50/60 Hz select to VSS.

Display Mode Select Inputs: In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal depletion pull-down devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying VSS to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the

gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs: Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal depletion pull-down devices are provided; application of VSS to these pins affects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, by selecting seconds display and actuating both slow and fast set inputs.

Output Common Source Connection: All display output drivers are open-drain devices with all sources common (*Figure 4a*). The common source pin should be connected to VSS.

12 or 24 Hour Select Input: By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal depletion pull-down device is again provided. Connecting this pin to VSS programs the 24-hour display format. Segment connections for 10's of Hours in 24-hour mode are shown in *Figure 6*.

Power Fail Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, all "ON" segments will flash at 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal.

connection diagrams

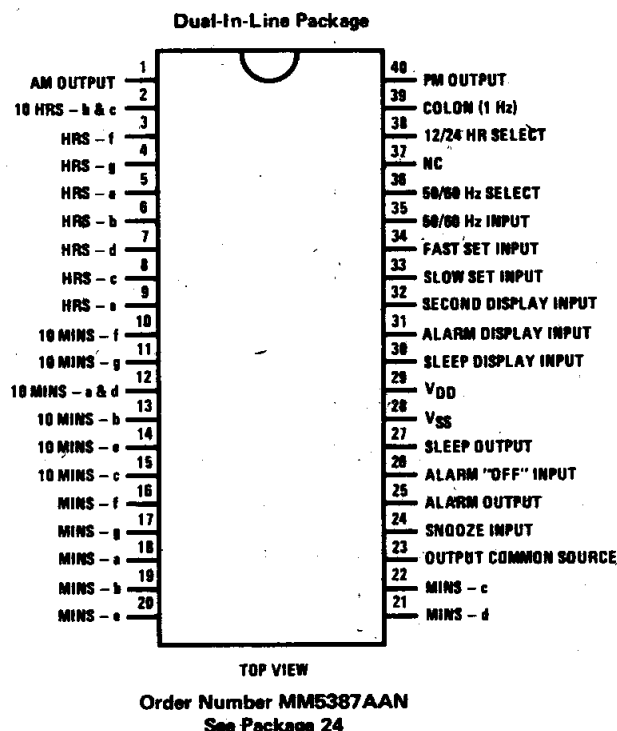


FIGURE 2(a). MM5387AA

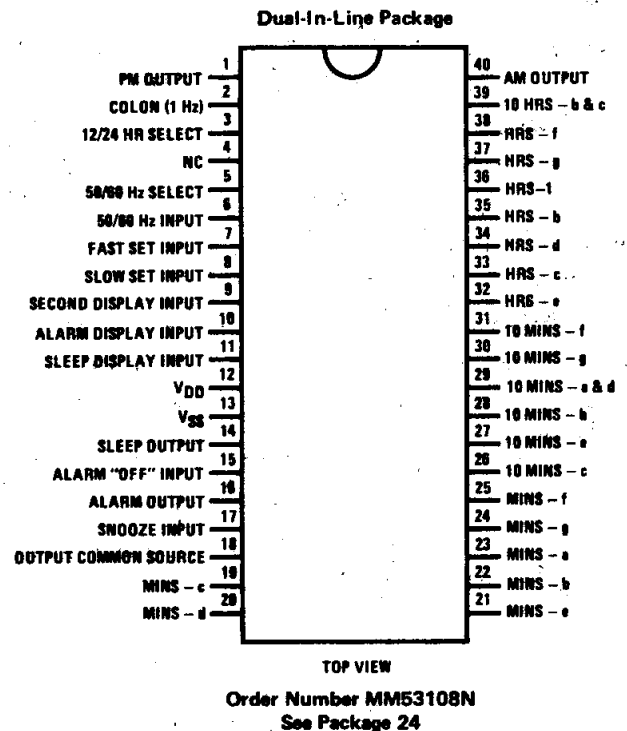


FIGURE 2(b). MM53108 (Mirror Image Pin-Out)

functional description (Continued)

Alarm Operation and Output: The alarm comparator (Figure 1) senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver (Figure 4b) which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input or reset by the alarm "OFF" input.

Snooze Alarm Input: Momentarily connecting snooze to VSS inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to VDD by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm "OFF" Input: Momentarily connecting alarm "OFF" to VSS resets the alarm latch and thereby

silences the alarm. This input is also returned to VDD by an internal depletion device. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at VSS.

Sleep Timer and Output: The sleep output can be used to turn "OFF" a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode, (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output which can be used to turn "ON" a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning "OFF" the radio. This turn "OFF" may also be manually controlled (at any time in the countdown) by a momentary VSS connection to the Snooze input. The output circuitry is the same as the other outputs (Figure 4b).

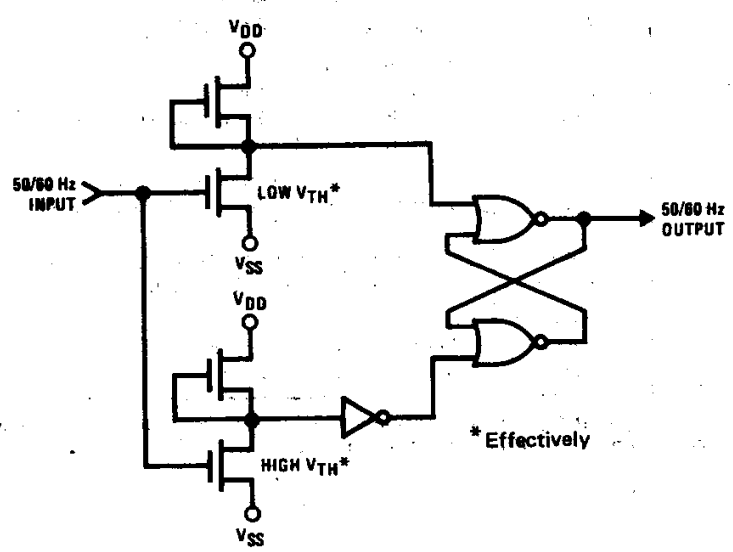


FIGURE 3. 50/60 Hz Input Shaping Circuit

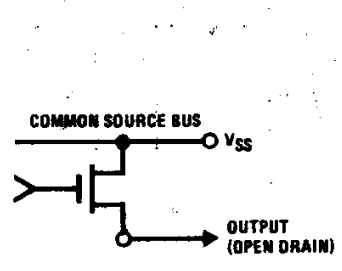


FIGURE 4(a). Segment Outputs

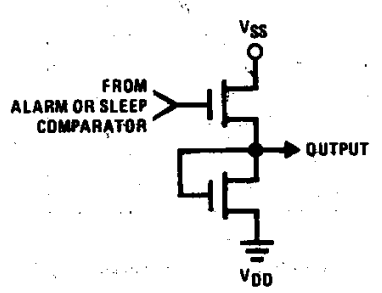


FIGURE 4(b). Alarm and Sleep Outputs

functional description (Continued)

TABLE I. MM5387AA, MM53108 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

* If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE II. MM5387AA, MM53108 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (Midnight) (12-Hour Format)
	Both	Alarm Resets to 00:00 (24-Hour Format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (Midnight) (12-Hour Format)
	Both	Time Resets to 00:00:00 (24-Hour Format)
Sleep	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 60 Hz
	Both	Subtracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

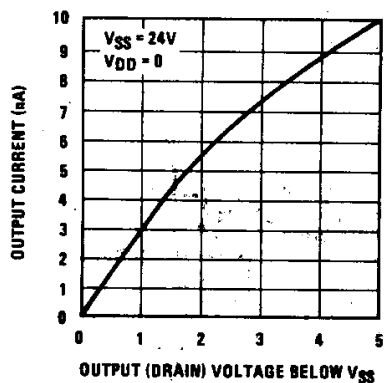
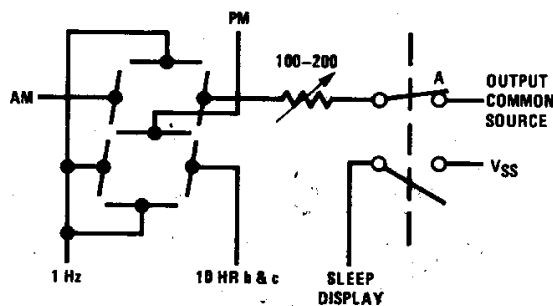


FIGURE 5. Typical Output Current Characteristics of MM5387AA, MM53108



Switch A must be ganged with Sleep display as shown.

FIGURE 6. 24-Hour Operation: 10's of Hours Digit Connections

typical applications

Figure 7 is a schematic diagram of a general purpose alarm clock circuit (12-hour mode) using the MM5387AA or MM53108 and a 3 1/2-digit LED display.

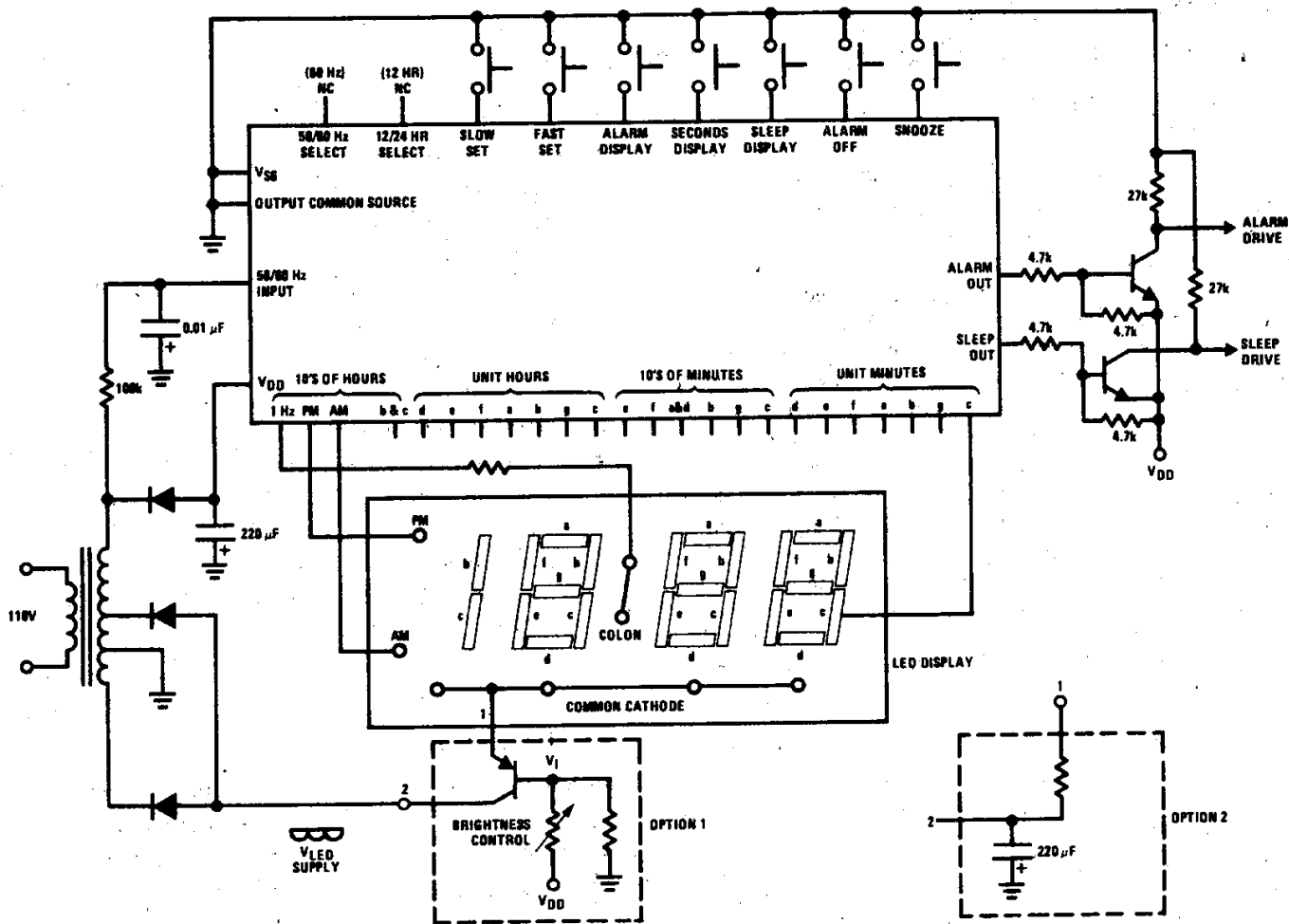


FIGURE 7