National Semiconductor

January 1994

DS3885 BTL Arbitration Transceiver

General Description

The DS3885 is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3885 Arbitration Transceiver is designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. The Arbitration Transceiver incorporates the competition logic internally which simplifies the implementation of a Futurebus+ application by minimizing the on board logic required.

The DS3885 driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state.

The BTL drivers also have high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

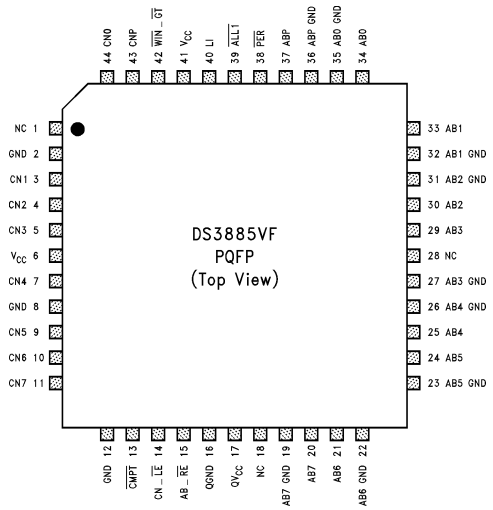
Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semicon-

(Continued)

Features

- 9-bit inverting BTL transceiver
- Meets IEEE 1194.1 standard on Backplane Transceiver Logic (BTL)
- Includes on chip competition logic and parity checking
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low bus-port voltage swing (typically 1V) at 80 mA
- Open collector bus-port output allows Wired-OR connection
- Exceeds 2 kV ESD testing (Human Body Model)
- Individual bus-port ground pins minimize ground bounce
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible driver and control inputs
- Built in bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Product offered in PLCC and PQFP package styles

Connection Diagrams



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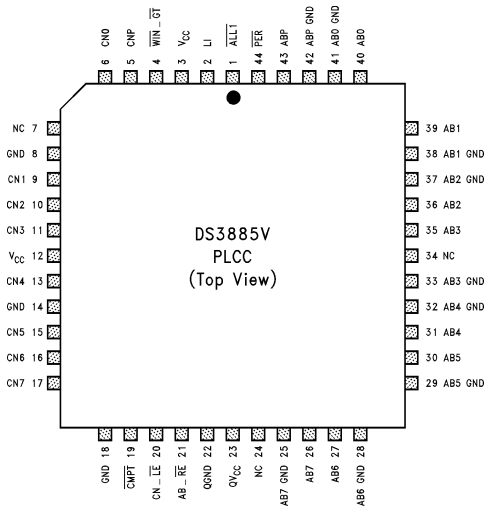

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Order Number DS3885V or DS3885VF
See NS Package Number V44A or VF44B

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General Description (Continued)

ductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. BTL eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The transceiver's control and driver inputs are designed with high impedance PNP input structures and are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The signals ab<7:0> designate the arbitration bus number which this transceiver places on the bus. The signal names AB<7:0> designate the open collector Wired-OR signals on the backplane bus.

The DS3885 implements an odd parity check on the arbitration bus bits AB<7:0>, with ABP being the parity bit. The signal $\overline{PER}$ will indicate the parity check result. For a quick indication of current bus conditions, the bus status block generates $\overline{ALL1}$ (all asserted) status when all bits (AB<7:0>) are asserted by any module. This signal is used by the DS3875 Arbitration Controller to detect the Arbitration message number (during phase 1) or the powerfail message number (during phase 2).

To latch the arbitration number into the transceiver, it is placed onto the CN<7:0> port, and the CN__$\overline{LE}$ signal is asserted. When the $\overline{CMPT}$ signal is asserted, the arbitration number is placed on the bus lines AB<7:0>. The $\overline{WIN}$__$\overline{GT}$ signal serves two purposes during the arbitration cycle. If the $\overline{CMPT}$ signal is not asserted during the arbitration cycle, the transceiver compares its internally latched number to the number on the AB<7:0> bus lines. If the internal number on the transceiver is greater than or equal to the number on the AB<7:0> lines, the $\overline{WIN}$__$\overline{GT}$ signal is asserted. However, if the $\overline{CMPT}$ signal is asserted, the transceiver participates in the competition. If the transceiver wins the arbitration, the $\overline{WIN}$__$\overline{GT}$ signal is asserted to confirm the winning. The AB__$\overline{RE}$ signal is used to enable the on-chip receiver outputs.

The DS3885 supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V_{CC} pin. The DS3885 also provides glitch free power-up/down protection during power sequencing.

The DS3885 has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two V_{CC} pins on the DS3885 that provide the supply voltage for the logic and control circuitry. Multiple power pins reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage difference should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed $\pm$0.5V because of ESD circuitry.

Additionally, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V

There are three different types of ground pins on the DS3885. They are the logic ground (GND), BTL grounds (AB0GND–AB7GND/ABPGND) and the Bandgap reference ground (QGND). All of these reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and AB0GND–AB7GND/ABPGND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3885, it is important to note that any voltage difference between ground pins, QGND, GND or AB0GND–AB7GND and ABPGND should not exceed $\pm$0.5V including power-up/down sequencing.

Three additional transceivers are included in the Futurebus+ family. They are the DS3883A BTL 9-bit Transceiver. The DS3884A BTL Handshake Transceiver features selectable Wired-OR glitch filtering. The DS3886A BTL 9-bit Latching Data Transceiver contains edge triggered latches in the driver which may be bypassed during a fall-through mode. In addition, the device contains a transparent latch in the receiver section.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

The LOGICAL INTERFACE FUTUREBUS+ ENGINE (LIFE) is a high performance Futurebus+ Protocol Controller designed for IEEE 896.1. The LIFE will handle all handshaking signals between the Futurebus+ and the local bus interface. The Protocol Controller supports the Futurebus+ compelled mode data transfer as both master and slave. The Protocol Controller can be configured to operate in compliance to IEEE 896.2 Profile B mode. The LIFE incorporates a DMA controller and 64-bit FIFO's for fast queuing.

All of the transceivers are offered in 44-pin PLCC and PQFP high density package styles.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage		6.5V
Control Input Voltage		6.5V
Driver Input and Receiver Output		5.5V
Receiver Input Current		±15 mA
Bus Termination Voltage		2.4V
Power Dissipation at 25°C	PLCC	2.5W
	PQFP	1.3W
Derate PLCC Package		20 mW/°C
Derate PQFP Package		11.1 mW/°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)		260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.06	2.14	V
Operating Free Air Temperature	0	70	°C

DC Electrical Characteristics (Notes 2 and 3) T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT (CNn CNP, CN__$\overline{LE}$, $\overline{CMPT}$, and AB__$\overline{RE}$)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			100	μA
I_{IH}	Input High Current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Input Low Current	$V_{IN} = 0.5V$			−100	μA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT (ABn and ABP)						
V_{OLB}	Output Low Bus Voltage (Note 5)	CNn = AB__$\overline{RE}$ = 2.4V, CN__$\overline{LE}$ = $\overline{CMPT}$ = 0.5V, I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OLBZ}	Output Low Bus Current	$\overline{CMPT}$ = AB__$\overline{RE}$ = 2.4V, ABn = 0.75V			−100	μA
I_{OHBZ}	Output High Bus Current	$\overline{CMPT}$ = AB__$\overline{RE}$ = 2.4V, ABn = 2.1V			100	μA
V_{TH}	Receiver Input Threshold		1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, I_{ABn} = 1 mA	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, I_{ABn} = 10 mA	2.9	3.9	5.0	V
V_{CLN}	Negative Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V
RECEIVER OUTPUT (CNn, CNP, $\overline{ALL1}$, $\overline{PER}$, and $\overline{WIN}$__$\overline{GT}$)						
V_{OH}	Voltage Output High	ABn = 1.1V, AB__$\overline{RE}$ = 0.5V, $\overline{CMPT}$ = CN__$\overline{LE}$ = 2.4V, $I_{OH} = -2$ mA	2.4	3.2		V
V_{OL}	Voltage Output Low	ABn = 2.1V, AB__$\overline{RE}$ = 0.5V, $\overline{CMPT}$ = CN__$\overline{LE}$ = 2.4V, I_{OL} = 24 mA		0.35	0.5	V
		ABn = 2.1V, AB__$\overline{RE}$ = 0.5V, $\overline{CMPT}$ = CN__$\overline{LE}$ = 2.4V, I_{OL} = 8 mA		0.30	0.4	V
I_{OZ}	TRI-STATE Leakge Current	CNn = CNP = 2.4V, = 2.4V, AB__$\overline{RE}$ = 2.4V			40	μA
		CNn = CNP = 0.5V, AB__$\overline{RE}$ = 2.4V			−100	μA
I_{OS}	Output Short Circuit Current	ABn = 1.1V, AB__$\overline{RE}$ = 0.5V, $\overline{CMPT}$ = CN__$\overline{LE}$ = 2.4V (Note 4)	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CC}	Supply Current: Includes V_{CC}, QV_{CC} and LI	$\overline{CMPT}$ = CN__$\overline{LE}$ = 0.5V, All CNn = AB__$\overline{RE}$ = 2.4V		75	100	mA
		$\overline{CMPT}$ = CN__$\overline{LE}$ = AB__$\overline{RE}$ = 2.4V		26	40	mA
I_{LI}	Live Insertion Current	$\overline{CMPT}$ = AB__$\overline{RE}$ = CNn = 2.4V, CN__$\overline{LE}$ = 0.5V		1.5	3	mA
		$\overline{CMPT}$ = CN__$\overline{LE}$ = 0.5V, All CNn = AB__$\overline{RE}$ = 2.4		3	5	mA

DC Electrical Characteristics (Notes 2 and 3) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Continued)

Note 1: Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed $V_{CC} + 0.5V$ and shall not exceed the absolute maximum rating at any time, including power-up and power-down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions: $V_{CC} = 5V$ and $T_A = 25°C$, unless otherwise stated.

Note 4: Only one output should be shorted at a time, and duration of the short not to exceed one second.

Note 5: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 6)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER (*Figures 1* and *2*)							
t_{PHL}	CN__$\overline{LE}$ to AB7	Propagation Delay	$\overline{CMPT} = 0V$, AB__$\overline{RE} = 3V$	7	13	18	ns
t_{PLH}				6	10	17	ns
t_r	Transition Time—Rise/Fall 20% to 80%		AB__$\overline{RE} = 3V$, $\overline{CMPT}$ = CN__$\overline{LE} = 0$		3		ns
t_f			AB__$\overline{RE} = 3V$, $\overline{CMPT}$ = CN__$\overline{LE} = 0$		1		ns
DRIVER TIMING REQUIREMENTS (*Figures 1* and *2*)							
t_S	CNn to CN__$\overline{LE}$	Set-Up Time	AB__$\overline{RE} = 3V$, $\overline{CMPT} = 0V$	9			ns
t_H	CN__$\overline{LE}$ to CNn	Hold Time	AB__$\overline{RE} = 3V$, $\overline{CMPT} = 0V$	0			ns
t_{PW}	CN__$\overline{LE}$ Pulse Width		AB__$\overline{RE} = 3V$, $\overline{CMPT} = 0V$	15			ns
RECEIVER							
t_{PHL}	ABn to CNn	Propagation Delay	AB__$\overline{RE} = 0V$, $\overline{CMPT}$ = CN__$\overline{LE} = 3V$ (*Figures 4* and *5*)	5	13	22	ns
t_{PLH}				3	15	23	ns
t_{PLZ}	AB__$\overline{RE}$ to CNn	Disable Time	$\overline{CMPT}$ = CN__$\overline{LE} = 3V$, ABn = 2.1V (*Figures 6* and *7*)	3	6	11	ns
t_{PZL}		Enable Time		5	9	13	ns
t_{PHZ}		Disable Time	$\overline{CMPT}$ = CN__$\overline{LE} = 3V$, ABn = 1.1V (*Figures 6* and *7*)	4	7	12	ns
t_{PZH}		Enable Time		3	6	11	ns
OTHERS							
t_{PHL}	AB0 to $\overline{ALL1}$ All Asserted Condition	Propagation Delay	AB <7:1> = 1.1V (*Figures 4* and *8*)	7	16	28	ns
t_{PLH}				7	16	26	ns
t_{PHL}	AB0 to $\overline{WIN}$__$\overline{GT}$ Win Condition	Propagation Delay	$\overline{CMPT}$ = CN__$\overline{LE} = 0V$, AB__$\overline{RE} = 3V$, CN <7:0> = 0V AB<7:0> = 2.1V (*Figures 4* and *9*)	6	14	23	ns
t_{PLH}				6	14	23	ns
t_{PHL}	AB0 to $\overline{WIN}$__$\overline{GT}$ Greater Than Condition	Propagation Delay	$\overline{CMPT}$ = AB__$\overline{RE} = 3V$, CN__$\overline{LE} = 0V$, CN <7:1> = 0V, CN0 = 3V AB<7:0> = 2.1V (*Figures 4* and *9*)	6	16	27	ns
t_{PLH}				6	16	26	ns
t_{PHL}	ABP to $\overline{PER}$ Parity Error Condition	Propagation Delay	$\overline{CMPT}$ = CN__$\overline{LE}$ = AB__$\overline{RE} = 3V$, AB <7:1> = 1.1V, AB0 = 2.1V (*Figures 4* and *8*)	6	13	23	ns
t_{PLH}				4	13	23	ns
t_{PHL}	ABn to AB <n−1>	Propagation Delay	$\overline{CMPT}$ = CN__$\overline{LE} = 0V$, AB__$\overline{RE} = 3V$, CNn = 0V, CN <n−1> = 3V, CN <7:n+1> = 0V, AB <7:n+1> = 2.1V (*Figures 1* and *10*)	5	12	22	ns
t_{PLH}				5	13	23	ns
t_{PHL}	$\overline{CMPT}$ to AB7	Propagation Delay	CN__$\overline{LE} = 0V$, AB__$\overline{RE}$ = CN7 = 3V (*Figures 1* and *3*)	4	8	14	ns
t_{PLH}				5	9	16	ns
t_{PHL}	AB7 to ABP	Propagation Delay	$\overline{CMPT}$ = CN__$\overline{LE} = 0V$, AB__$\overline{RE}$ = CNP = 3V, CN <7:0> = 0V (*Figures 1* and *10*)		36	60	ns
t_{PLH}					36	60	ns

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 6) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PARAMETERS NOT TESTED						
C_{output}	Capacitance at Bn	(Note 7)		5		pF
t_{NR}	Noise Rejection	(Note 8)		1		ns

Note 6: All input rise/fall times should be 3 ns.

Note 7: This parameter is tested using TDR techniques described in 1194.0 BTL Backplane Design Guide.

Note 8: This parameter is tested during device characterization. The measurement revealed that the part will typically reject 1 ns pulse width.

Pin Description

Pin Name	Number of Pins	Input/ Output	Description
$\overline{ALL1}$	1	O	TTL—All asserted (A logic ''1'' indicates that all the competition bits are asserted.)
AB<7:0>	8	I/O	BTL—Futurebus+ Wired-OR competition bits
ABP	1	I/O	BTL—Futurebus+ Wired-OR competition parity bit
AB<7:0> and ABP GND	9	NA	Parallel driver grounds reduce ground bounce due to high current switching of driver outputs (Note 9)
CN<7:0>	8	I/O	TTL TRI-STATE—Module competition bits
CNP	1	I	TTL TRI-STATE—Module competition parity bit
$\overline{CMPT}$	1	I	TTL—Competition bit (A logic ''0'' indicates that the module will compete in the arbitration.)
GND	3	NA	Ground for switching circuits. (Note 9)
CN__$\overline{LE}$	1	I	TTL—CNn latch enable (A logic ''0'' indicates that the CN<n> logic states are latched with corresponding parity bit).
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 10)
NC	3	NA	No connect
$\overline{PER}$	1	O	TTL—ABn odd parity (A logic ''0'' indicates parity error)
AB__$\overline{RE}$	1	I	TTL—Receiver Enable (A logic ''0'' enables receivers)
QGND	1	NA	Ground for receiver input bandgap reference and non-switching circuits. (Note 9)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits. (Note 2)
V_{CC}	2	NA	V_{CC} supply for switching circuits. (Note 10)
$\overline{WIN}$__$\overline{GT}$	1	O	TTL—Win signal (active low). During competition, $\overline{WIN}$__$\overline{GT}$ indicates that the module has won the competition. For a module not participating in the competition, $\overline{WIN}$__$\overline{GT}$ indicates that the module has a number which is greater than winner's number.

Note 9: The multiplicity of parallel ground paths, reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance (i.e., ground plane with power pins and many signal pins connected to the backplane ground). If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

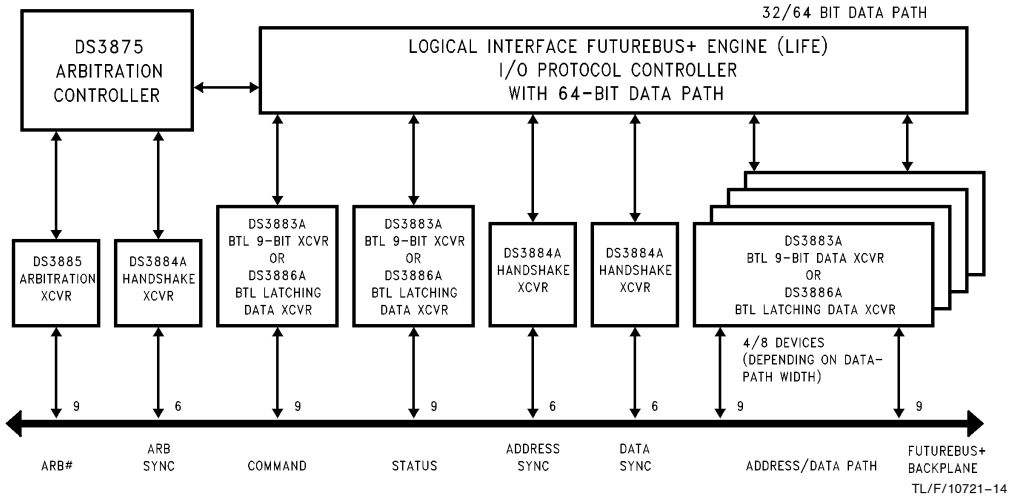
Note 10: The same considerations for ground are used for V_{CC} in reducing lead inductance. (See Note 9) QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Package Thermal Characteristics

Linear Feet Per Minute Air Flow (LFPM)	θ_{ja} (°C/W)	
	44-Pin PQFP	44-Pin PLCC
0	82	45
225	68	35
500	60	30
900	53	26

Note: The above values are typical values and are different from the Absolute Maximum Rating values, which include guardbands.

Typical Application



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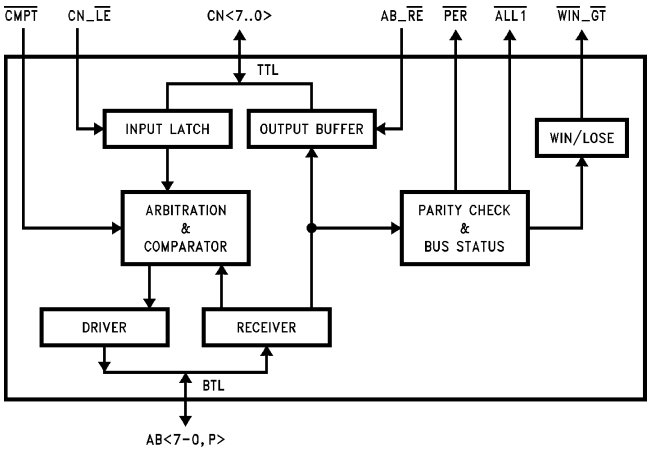
DS3885 Block Diagram



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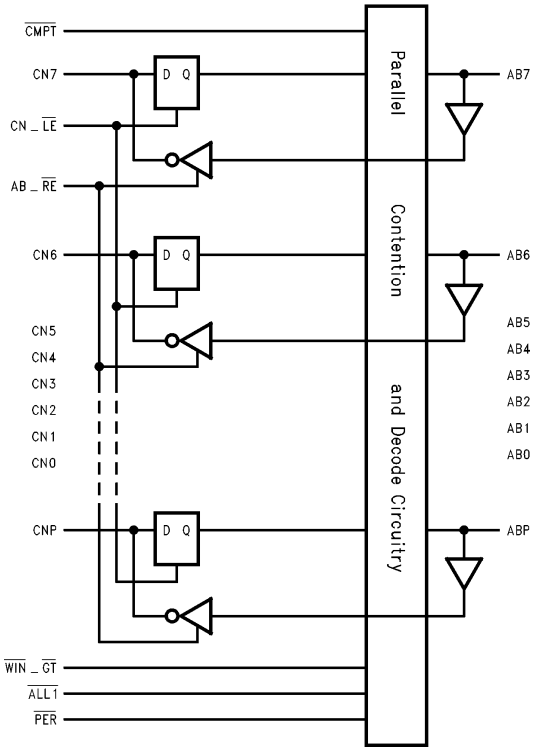
Function Diagram

Parallel Implementation of Parallel Contention Logic



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Test Circuits and Timing Waveforms

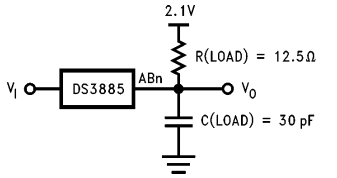

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FIGURE 1. Driver Propagation Delay Set-up

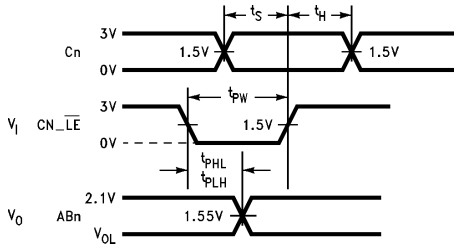

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FIGURE 2. Driver: CN__$\overline{LE}$ to AB7, t_S, t_H, t_{PW}

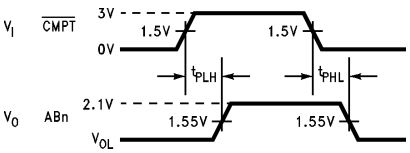

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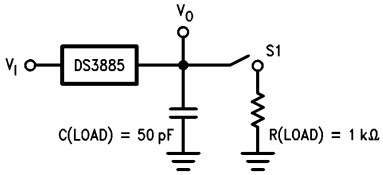
FIGURE 3. Driver: $\overline{CMPT}$ to AB7



Switch Position

	t_{PLH}	t_{PHL}
S1	open	close

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FIGURE 4. Receiver Propagation Delay Set-Up

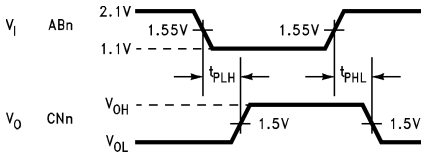

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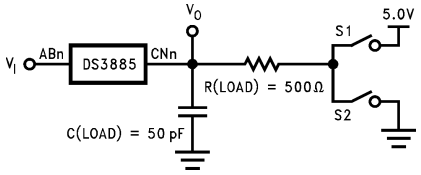
FIGURE 5. Receiver: ABn to CNn

Test Circuits and Timing Waveforms (Continued)



Switch Position		
	t_{PZL} t_{PLZ}	t_{PZH} t_{PHZ}
S1	close	open
S2	open	close

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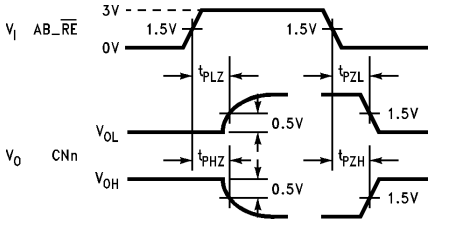
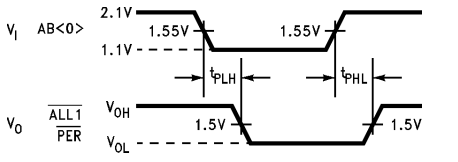
FIGURE 6. Receiver Enable/Disable Set-Up



TL/F/10721–9

FIGURE 7. Receiver: AB__$\overline{RE}$ to CNn



TL/F/10721–10

FIGURE 8. AB0 to $\overline{ALL1}$, AB0 to $\overline{PER}$

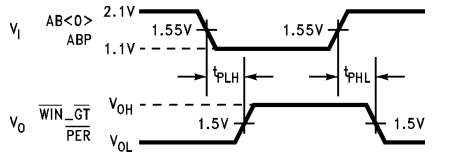


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FIGURE 9. AB0 to $\overline{WIN}$__$\overline{GT}$, ABP TO $\overline{PER}$

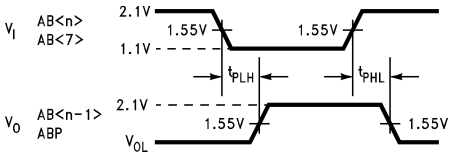

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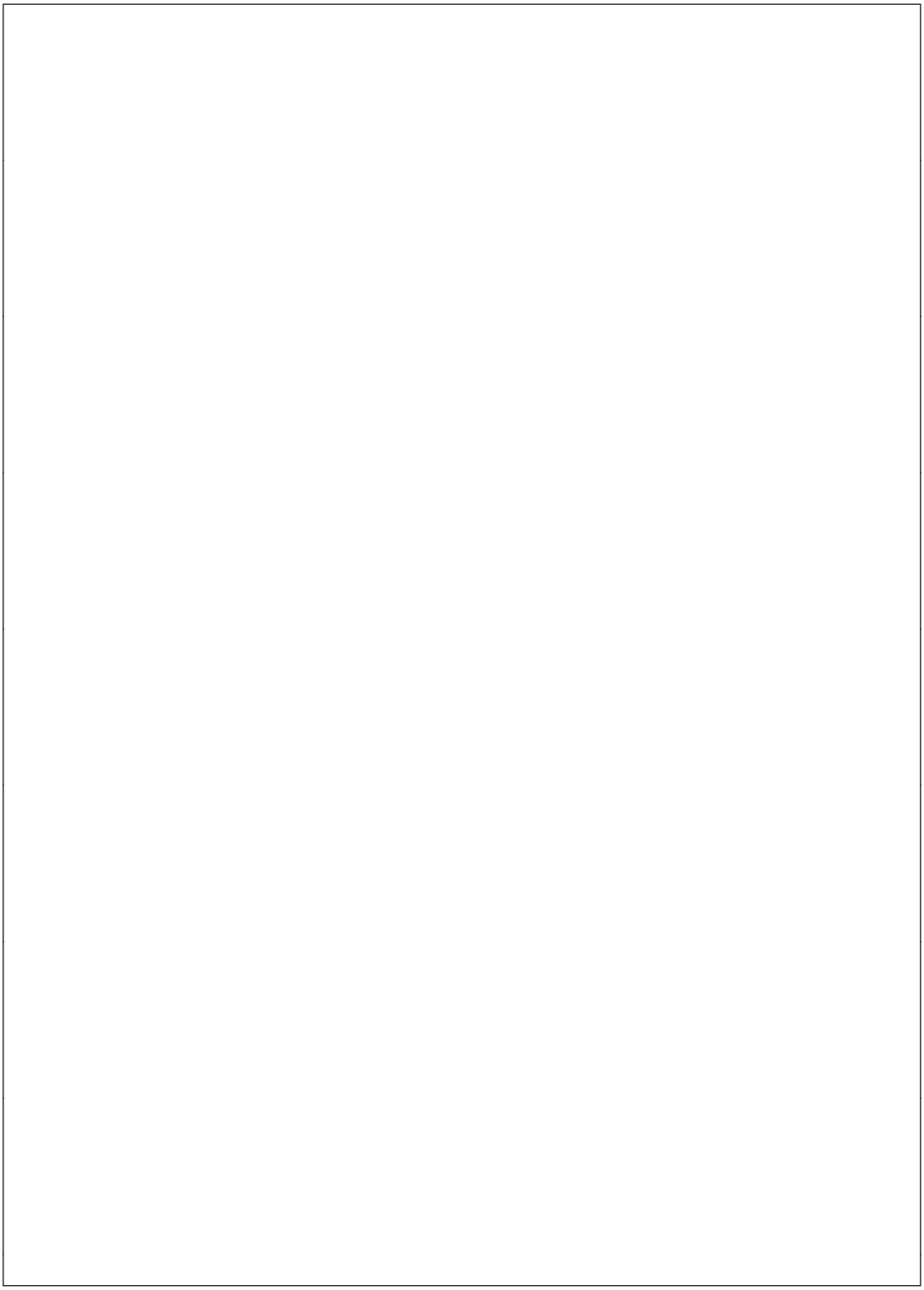
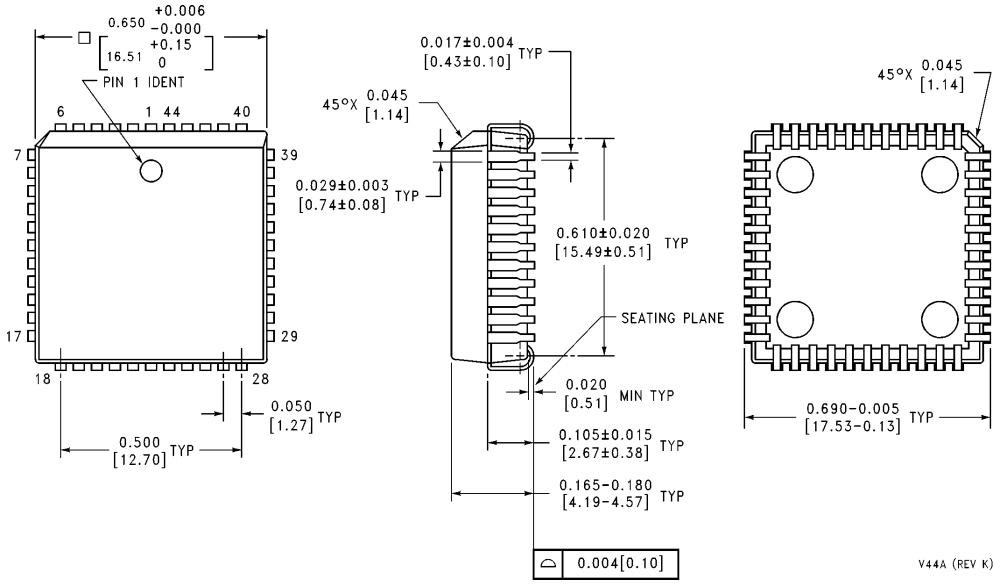
FIGURE 10. ABn to AB<n-1>, AB7 to ABP

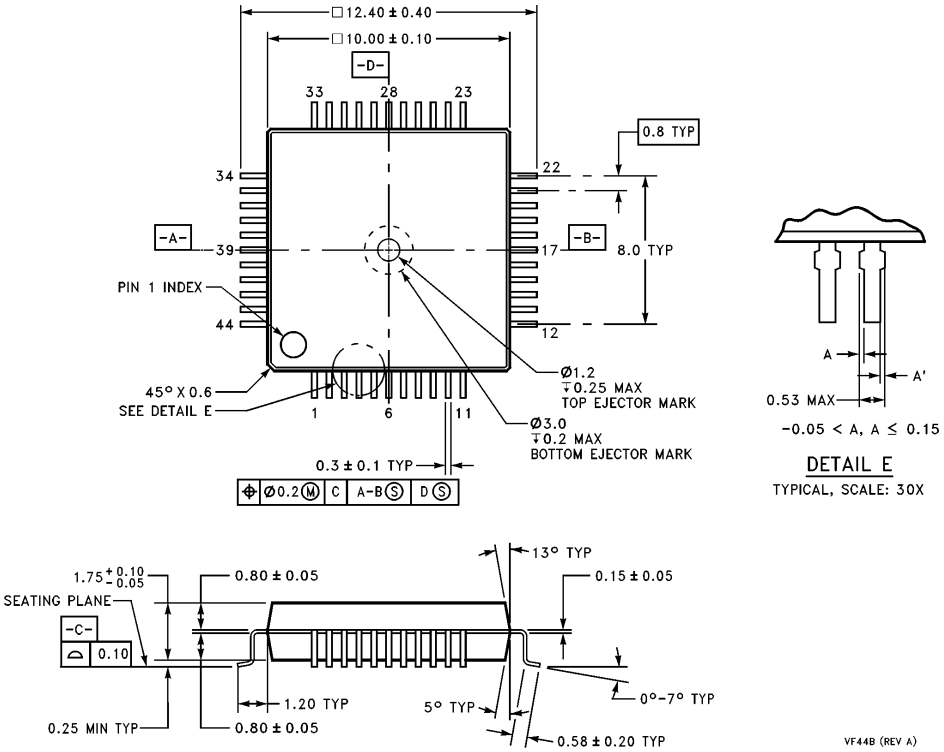


Physical Dimensions inches (millimeters)



44-Lead Plastic Chip Carrier
Order Number DS3885V
NS Package Number V44A

Physical Dimensions inches (millimeters) (Continued)



VF44B (REV A)

44-Lead Plastic Quad Flatpack
Order Number DS3885VF
NS Package Number VF44B

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