January 2002

National Semiconductor

LMH6672
Dual, High Output Current, High Speed Op Amp

General Description

The LMH6672 is a low cost, dual high speed op amp capable of driving signals to within 1V of the power supply rails. It features the high output drive with low distortion required for the demanding application of a single supply xDSL line driver.

When connected as a differential output driver, the LMH6672 can drive a 50Ω load to 16.8V_{PP} swing with only −93dBc distortion, fully supporting the peak upstream power levels for upstream full-rate ADSL. The LMH6672 is fully specified for operation with 5V and 12V supplies. Ideal for PCI modem cards and xDSL modems.

Applications

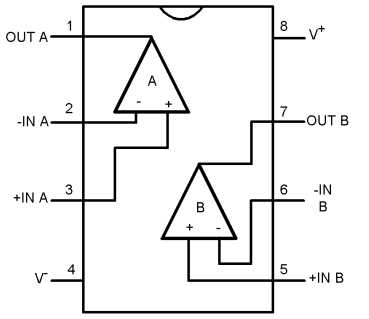
- ADSL PCI modem cards
- xDSL external modems
- Line drivers

Features

- **High Output Drive**
  - 19.2V_{PP} differential output voltage, R_L = 50Ω
  - 9.6V_{PP} single-ended output voltage, R_L = 25Ω
- **High Output Current**
  - ±200mA @ V_O = 9$_{VPP}$, V_S = 12V
- **Low Distortion**
  - 93dB SFDR @ 100KHz, V_O = 8.4V_{PP}, R_L = 25Ω
  - 92dB SFDR @ 1MHz, V_O = 2V_{PP}, R_L = 100Ω
- **High Speed**
  - 130MHz 3dB bandwidth (G = 2)
  - 160V/µs slew rate
- **Low Noise**
  - 4.5nV/$\sqrt{Hz}$: input noise voltage
  - 1.7pA/$\sqrt{Hz}$: input noise current
- Low supply current: 6.2mA/amp
- Single-supply operation: 5V to 12V
- Available in 8-pin SOIC, PSOP and LLP

Connection Diagram

8-Pin SOIC/PSOP/LLP



Top View

Typical Application

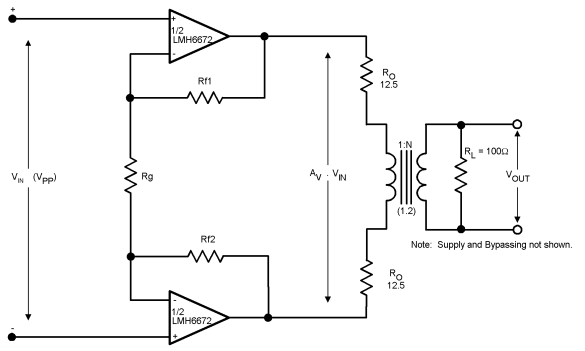


Figure 1

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6672MA	LMH6672MA	Rails	M08A
	LMH6672MAX	LMH6672MA	2.5k Units Tape and Reel	
8-Pin PSOP	LMH6672MR	LMH6672MR	Rails	MRA08A
	LMH6672MRX	LMH6672MR	2.5k Units Tape and Reel	
8-Pin LLP	LMH6672LD	L6672LD	1k Units Tape and Reel	LDC08A
	LMH6672LDX	L6672LD	4.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	(Note 2)
Human Body Model	2kV
Machine Model	200V
V_{IN} Differential	±1.2V
Output Short Circuit Duration	(Note 2)
Supply Voltage ($V^+ - V^-$)	13.2V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature	+150˚C (Note 4)
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	±2.5V to ±6.5V
Junction Temperature Range	−40˚C to 150˚C
Package Thermal Resistance (θ_{JA})	
8-pin SOIC	172˚C/W
8-pin PSOP	58.6˚C/W
8-pin LLP	40˚C/W

Electrical Characteristics

T_J = 25˚C, G = +2, V_S = ±2.5 to ±6V, R_f = R_{IN} = 470Ω, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
	−3dB Bandwidth			130		MHz
	0.1dB Bandwidth	V_S = ±6V		22		MHz
	Slew Rate	V_S = ±6V, 4V Step, 10-90%		170		V/µs
	Rise and Fall Time	V_S = 6V, 4V Step, 10-90%		18.5		ns
Distortion and Noise Response						
	2nd Harmonic Distortion	V_O = 8.4V_{PP}, f = 100KHz, R_L = 25Ω		−95		dBc
		V_O = 8.4V_{PP}, f = 1MHz, R_L = 100Ω		−92		dBc
	3rd Harmonic Distortion	V_O = 8.4V_{PP}, f = 100KHz, R_L = 25Ω		−93		dBc
		V_O = 2V_{PP}, f = 1MHz, R_L = 100Ω		−95		dBc
	Input Noise Voltage	f = 100KHz		4.5		nV $\sqrt{Hz}$
	Input Noise Current	f = 100KHz		1.7		pA/ $\sqrt{Hz}$
Input Characteristics						
V_{OS}	Input Offset Voltage	T_J = −40˚C to 150˚C	−5.5	−0.2	5.5	mV
			−4	−0.2	4	
I_B	Input Bias Current	T_J = −40˚C to 150˚C		8	14	µA
I_{OS}	Input Offset Current	T_J = −40˚C to 150˚C	−2.1	0	2.1	µA
CMVR	Common Voltage Range	V_S = ±6V	−6.0		4.5	V
CMRR	Common-Mode Rejection Ratio	V_S = ±6V, T_J = −40˚C to 150˚C	150	9.5		µV/V
Transfer Characteristics						
A_{VOL}	Voltage Gain	R_L = 1k, T_J = −40˚C to 150˚C	1.0	2.5		V/mV
		R_L = 25Ω, T_J = −40˚C to 150˚C	0.67	1.7		V/mV
	Output Swing	R_L = 25Ω, V_S = ±6V	−4.5	±4.8	4.5	V
		R_L = 25Ω, T_J = −40˚C to 150˚C, V_S = ±6V	−4.4	±4.8	4.4	
	Output Swing	R_L = 1k, V_S = ±6V	−4.8	±4.8	4.8	V
		R_L = 1k, T_J = −40˚C to 150˚C, V_S = ±6V	−4.7	±4.8	4.7	
I_{SC}	Output Current (Note 3)	V_O = 0, V_S = ±6V	400	788		mA
		V_O = 0, V_S = ±6V, T_J = −40˚C to 150˚C	260	600		mA
Power Supply						

Electrical Characteristics (Continued)

T_J = 25˚C, G = +2, V_S = ±2.5 to ±6V, R_f = R_{IN} = 470Ω, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_S	Supply Current/Amp	V_S = ±6V			8	mA
		V_S = ±6V, T_J = −40˚C to 150˚C		6.2	9	
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±6V, T_J = −40˚C to 150˚C	72	78		dB

±2.5V Electrical Characteristics

T_J = 25˚C, G = +2, V_S = ±2.5 to ±6V, R_f = R_{IN} = 470Ω, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
	−3dB Bandwidth			125		MHz
	0.1dB Bandwidth			32		MHz
	Slew Rate	0.4V Step, 10-90%		115		V/µs
	Rise and Fall Time	0.4V Step, 10-90%		2.75		ns
Distortion and Noise Response						
	2nd Harmonic Distortion	V_O = $2V_{PP}$, f = 100KHz, R_L = 25Ω		−85		dBc
		V_O = $2V_{PP}$, f = 1MHz, R_L = 100Ω		−87		dBc
	3rd Harmonic Distortion	V_O = $2V_{PP}$, f = 100KHz, R_L = 25Ω		−90		dBc
		V_O = $2V_{PP}$, f = 1MHz, R_L = 100Ω		−88		dBc
Input Characteristics						
V_{OS}	Input Offset Voltage	T_J = −40˚C to 150˚C	−5.5		5.5	mV
			−4.0	1.1	4.0	
I_B	Input Bias Current	T_J = −40˚C to 150˚C		8.0	14	µA
CMVR	Common-Mode Voltage Range		−2.5		1.0	V
CMRR	Common-Mode Rejection Ratio	T_J = −40˚C to 150˚C	150	57		µV/V
Transfer Characteristics						
A_{VOL}	Voltage Gain	R_L = 25Ω, T_J = −40˚C to 150˚C	0.67	1.54		V/mV
		R_L = 1k, T_J = −40˚C to 150˚C	1.0	2.0		
Output Characteristics						
V_O	Output Voltage Swing	R_L = 25Ω	1.20	1.45		V
		R_L = 25Ω, T_J = −40˚C to 150˚C	1.10	1.35		
		R_L = 1k	1.30	1.60		
		R_L = 1k, T_J = −40˚C to 150˚C	1.25	1.50		
Power Supply						
I_S	Supply Current/Amp				8.0	mA
		T_J = −40˚C to 150˚C		5.6	9.0	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Note 3: Shorting the output to either supply or ground will exceed the absolute maximum T_J and can result in failure.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

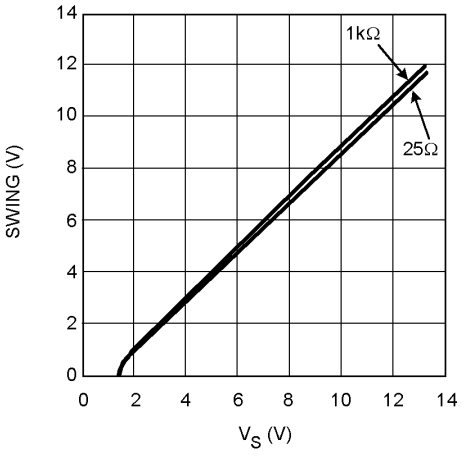
Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing, characterization or statistical analysis.

Typical Performance Characteristics

At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified.

Output Swing R_L = 25Ω, 1kΩ @ −40˚C, 25˚C, 85˚C



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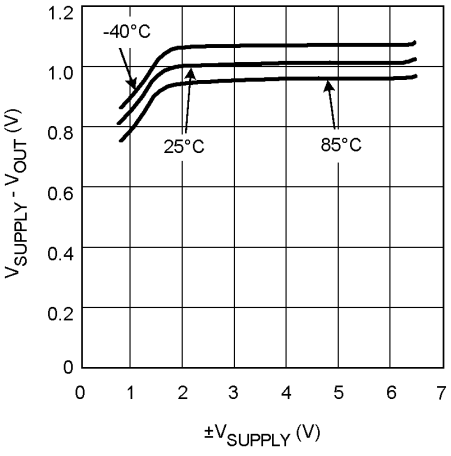
Positive Output Swing into 1kΩ



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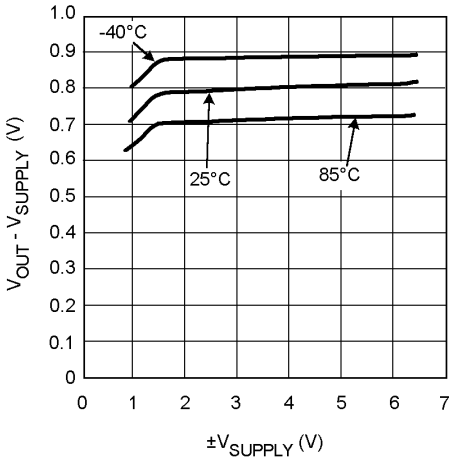
Negative Output Swing into 1kΩ



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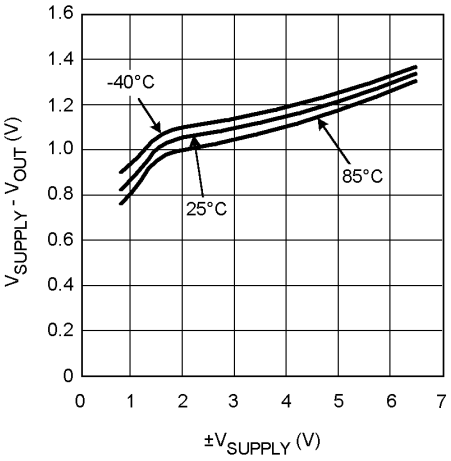
Positive Output Swing into 25Ω



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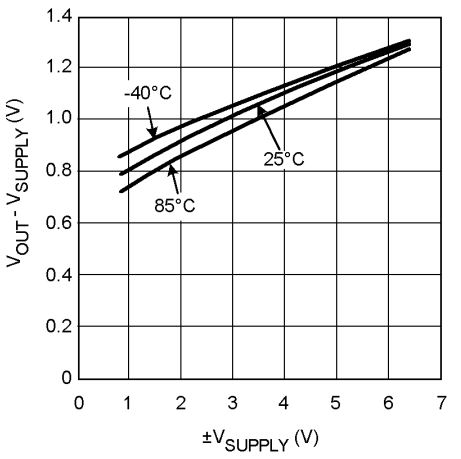
Negative Output Swing into 25Ω



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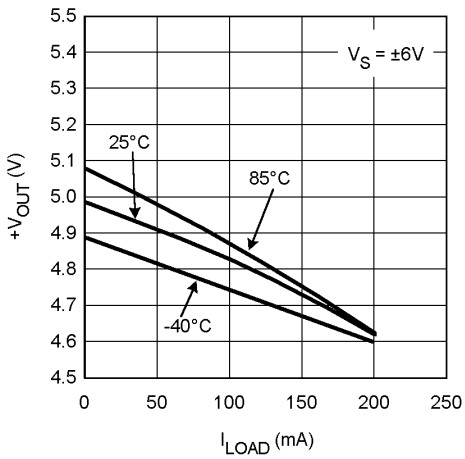
$+V_{OUT}$ vs. I_{LOAD}



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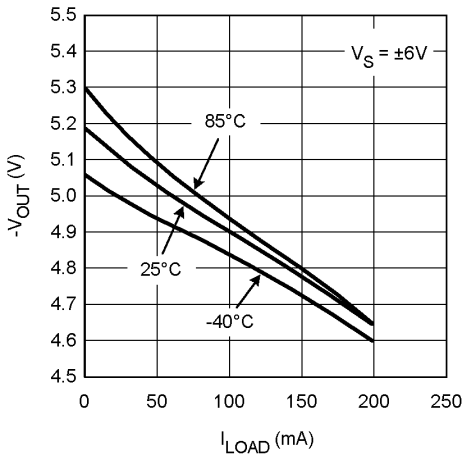
Typical Performance Characteristics

At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

$-V_{OUT}$ vs. I_{LOAD}



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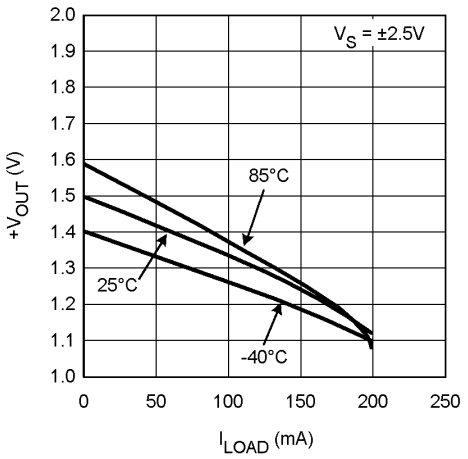
$+V_{OUT}$ vs. I_{LOAD}



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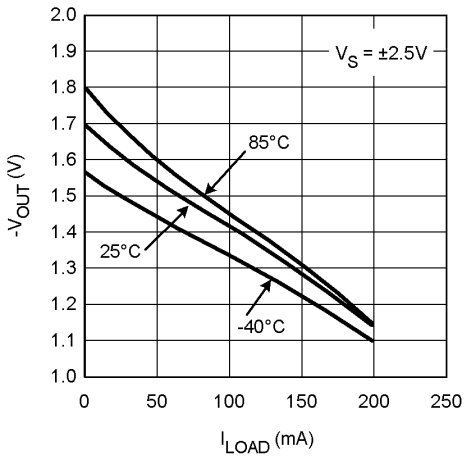
$-V_{OUT}$ vs. I_{LOAD}



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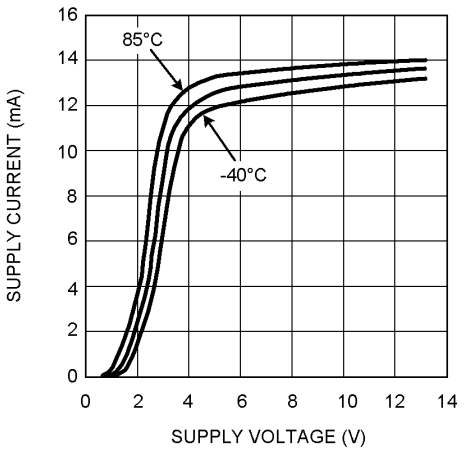
Supply Current vs. Supply Voltage



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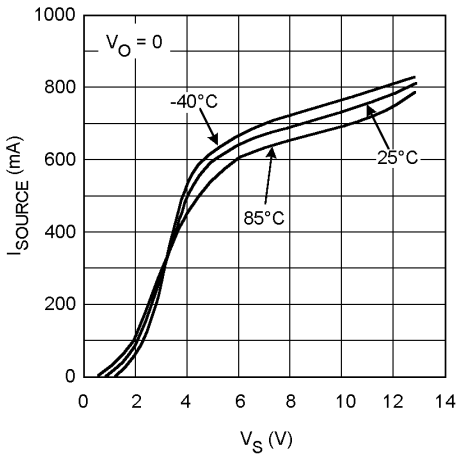
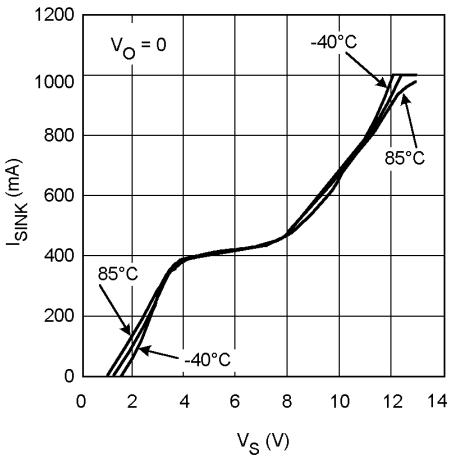
Sourcing Current vs. Supply Voltage



20016633

Sinking Current vs. Supply Voltage

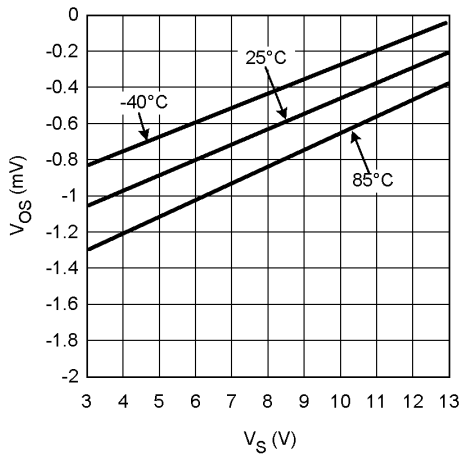


20016634

Typical Performance Characteristics

At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

V_{OS} vs. V_S



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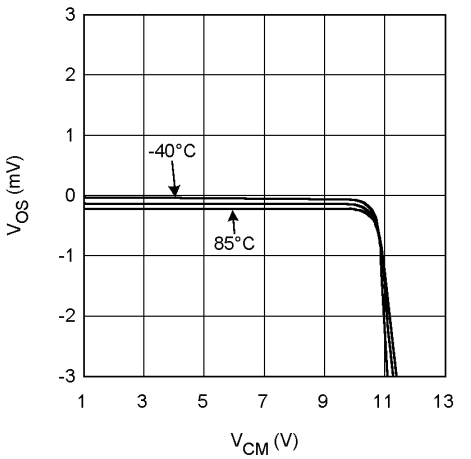
V_{OS} vs. V_{CM}, V_S = 12V



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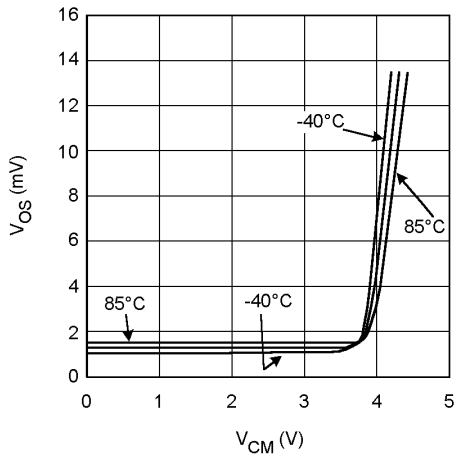
V_{OS} vs. V_{CM}, V_S = 5V



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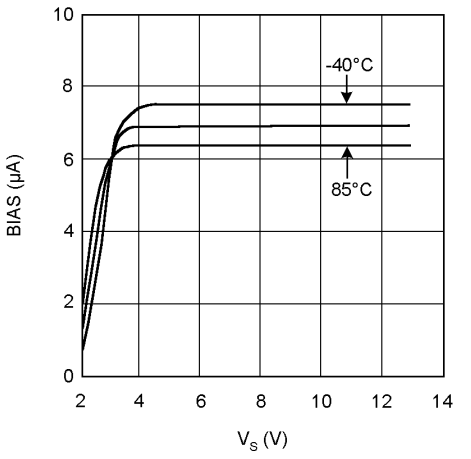
Bias Current vs. V_{SUPPLY}



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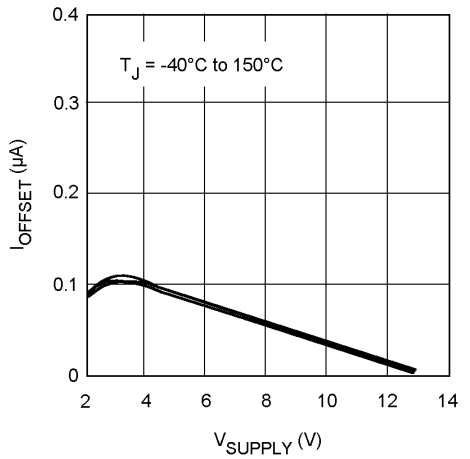
Offset Current vs. V_{SUPPLY}



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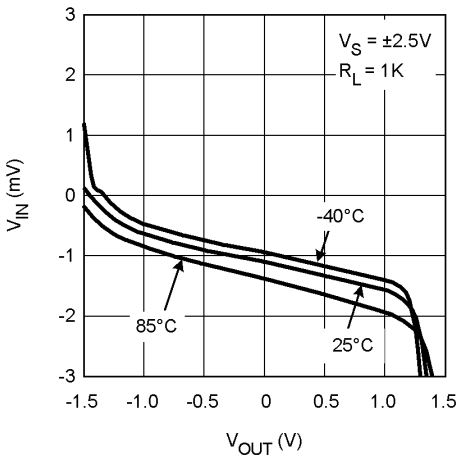
V_{OUT} vs. V_{IN}

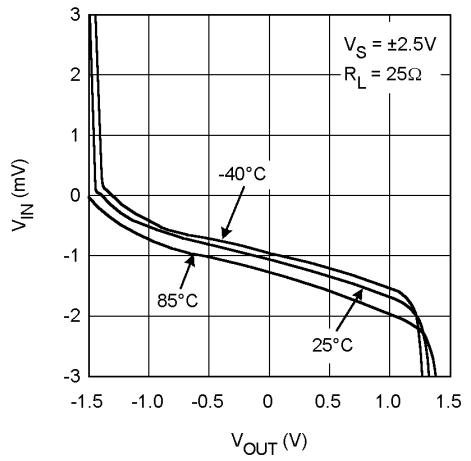


20016639

Typical Performance Characteristics

At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

V_{OUT} vs. V_{IN}



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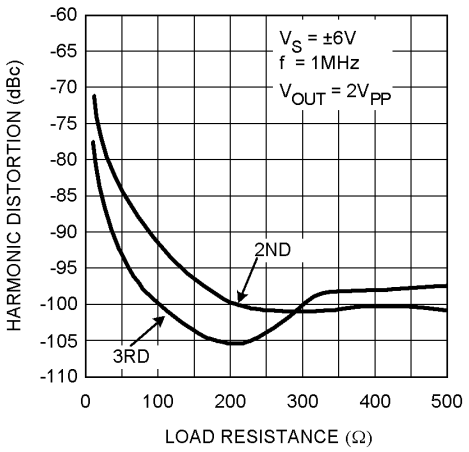
Harmonic Distortion vs. Load



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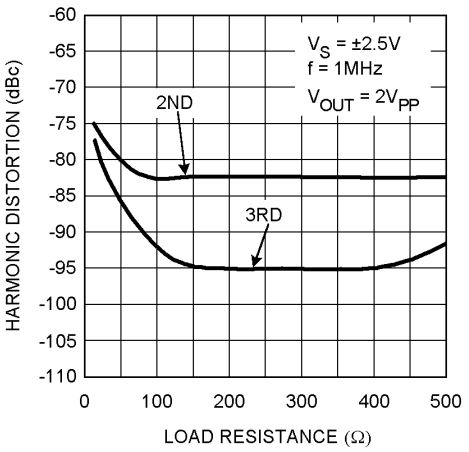
Harmonic Distortion vs. Load



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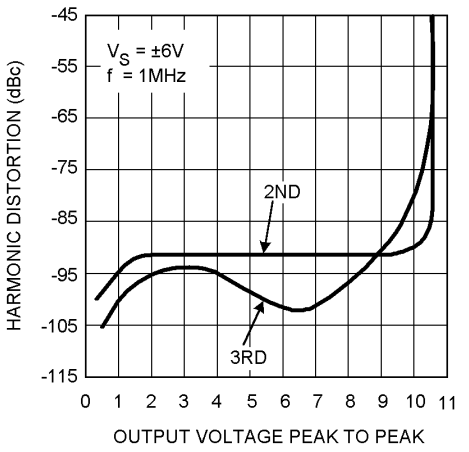
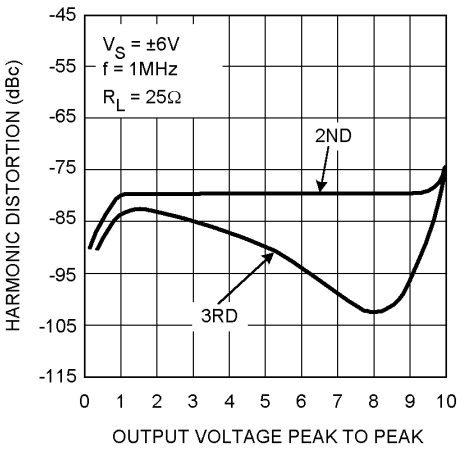
Harmonic Distortion vs. Output Voltage



20016614

Harmonic Distortion vs. Output Voltage



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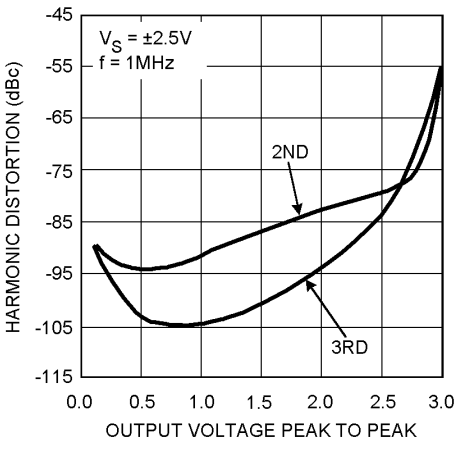
Harmonic Distortion vs. Output Voltage

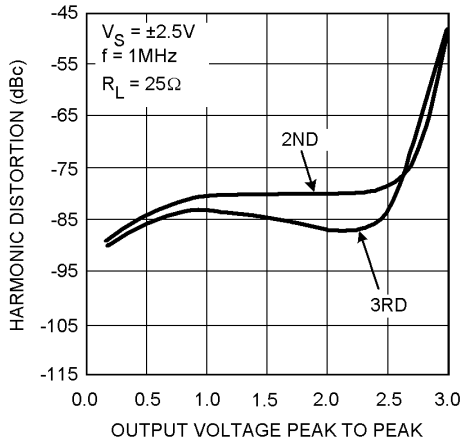


20016612

Typical Performance Characteristics

At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

Harmonic Distortion vs. Output Voltage



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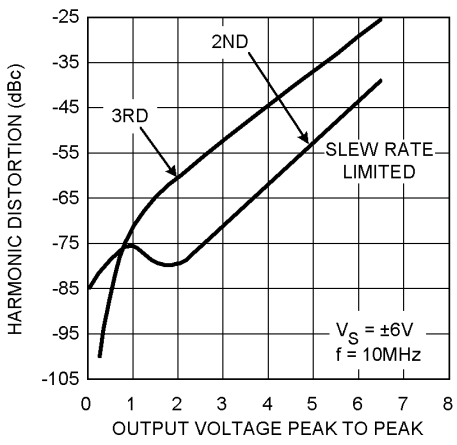
Harmonic Distortion vs. Output Voltage



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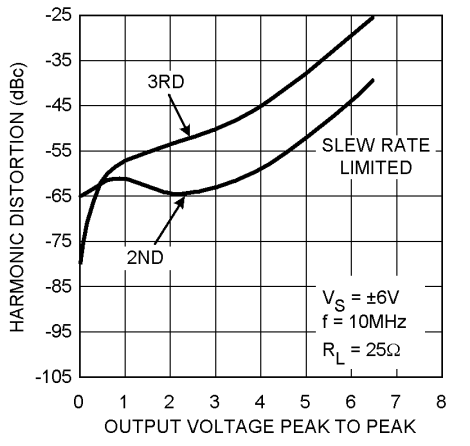
Harmonic Distortion vs. Output Voltage



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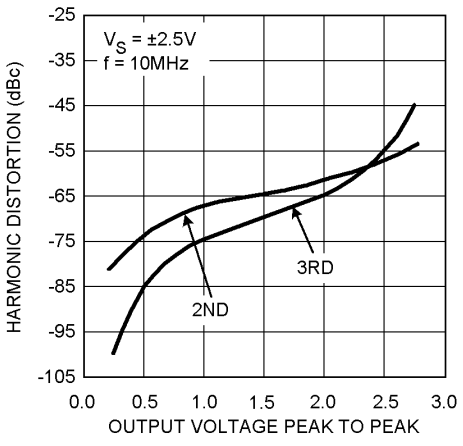
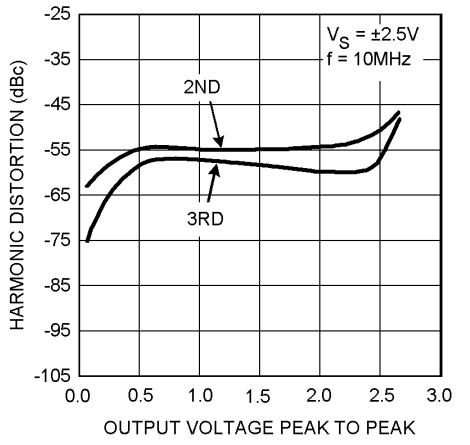
Harmonic Distortion vs. Output Voltage



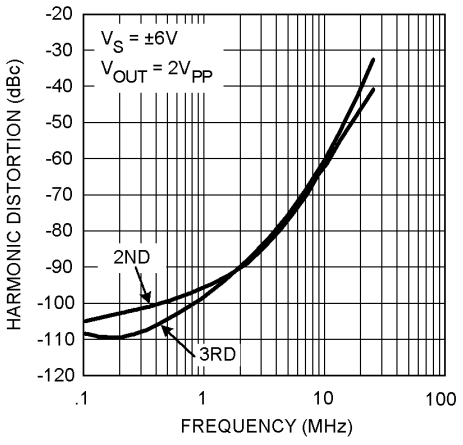
20016616

Harmonic Distortion vs. Output Voltage



20016618

Harmonic Distortion vs. Frequency

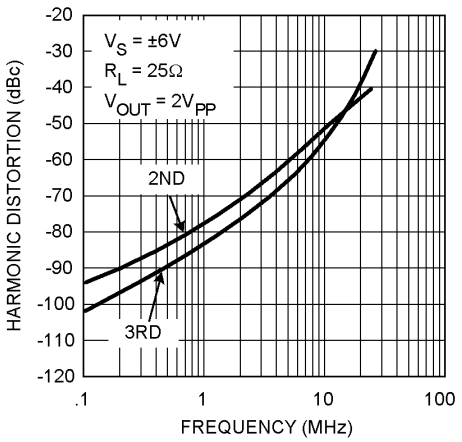


20016622

Typical Performance Characteristics

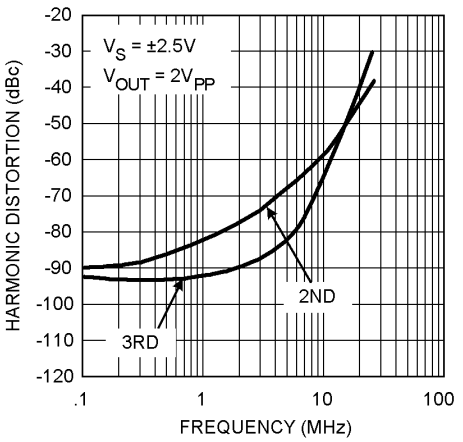
At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

Harmonic Distortion vs. Frequency



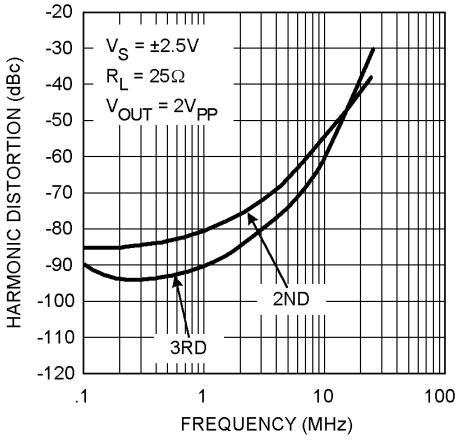
20016621

Harmonic Distortion vs. Frequency



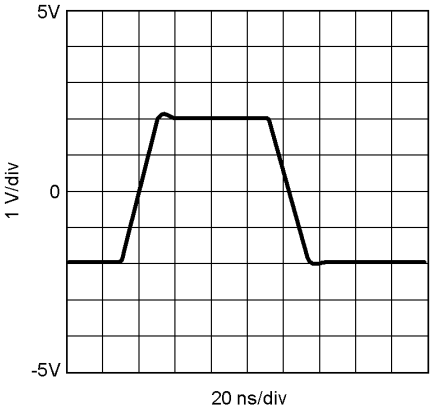
20016623

Harmonic Distortion vs. Frequency



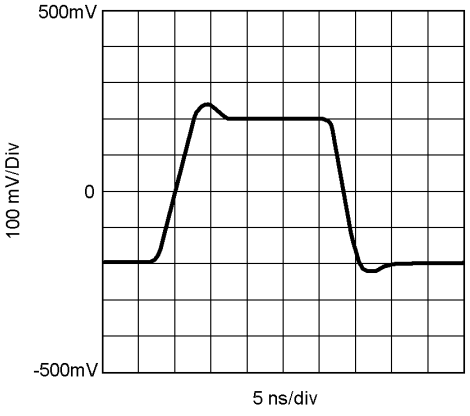
20016624

Pulse Response, V_S = ±6V



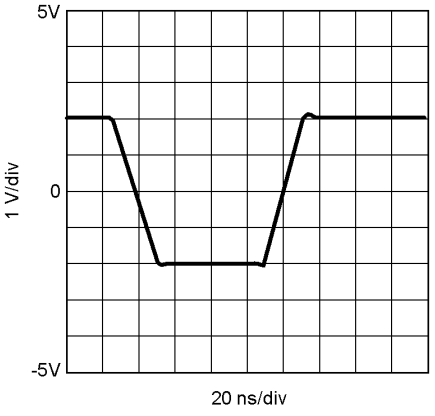
20016627

Pulse Response, V_S = ±2.5V, ±6V



20016628

Pulse Response, (A_{VCL} = −1, V_S = ±6V)

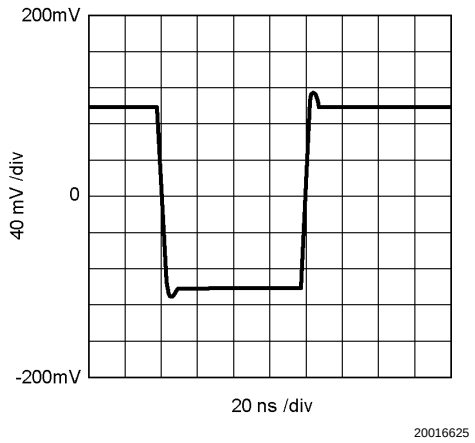


20016626

Typical Performance Characteristics

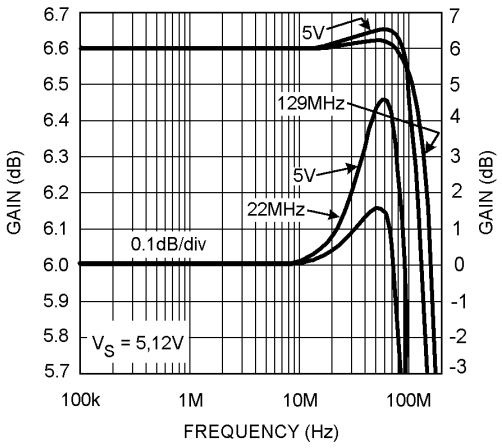
At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

Pulse Response, (A_{VCL} = −1, V_S = ±2.5V, ±6V)



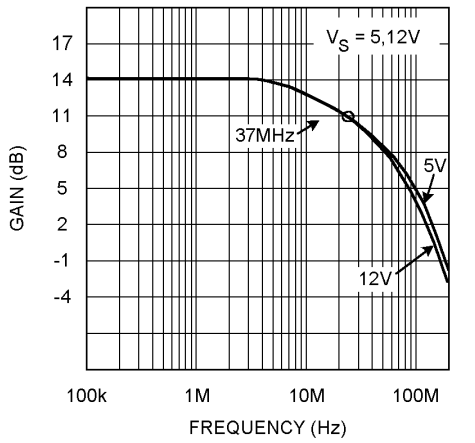
20016625

Frequency Response



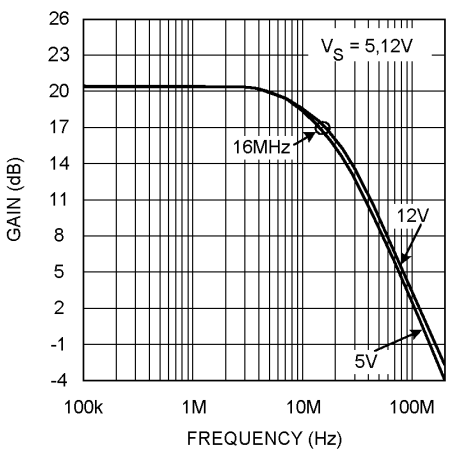
20016650

Frequency Response, A_{VCL} = +5V



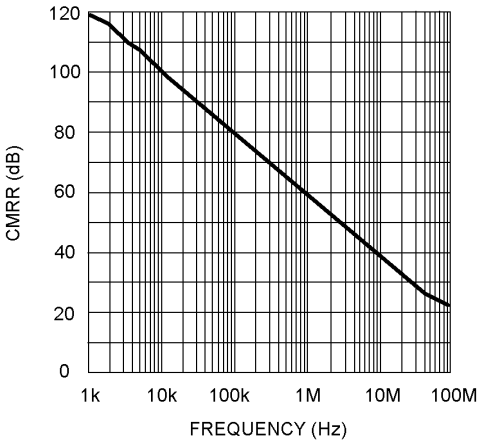
20016649

Frequency Response, A_{VCL} = +10



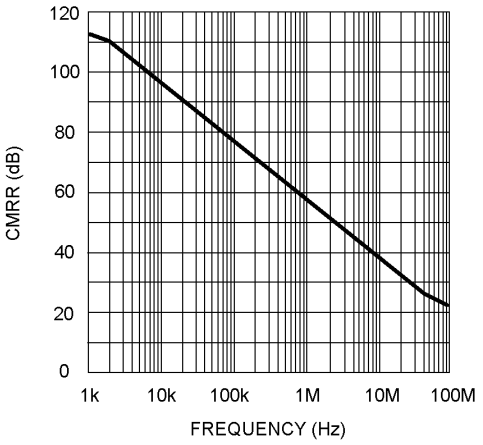
20016648

CMRR vs. Frequency @ 12V



20016606

CMRR vs. Frequency @ 5V

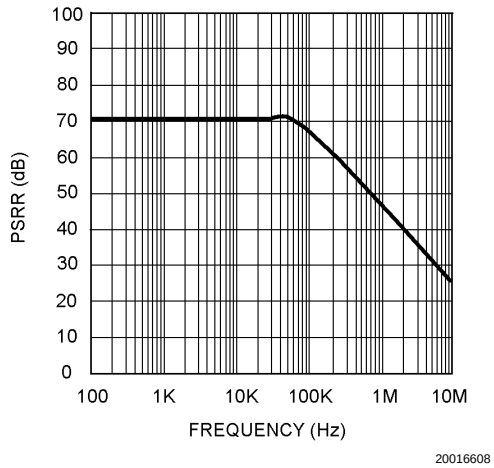


20016605

Typical Performance Characteristics

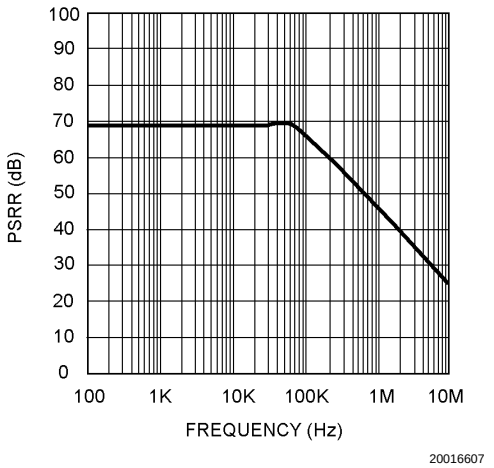
At T_J = 25˚C, R_F = 470Ω gain = +2, R_L = 100Ω. Unless otherwise specified. (Continued)

PSRR vs. Frequency @ 12V



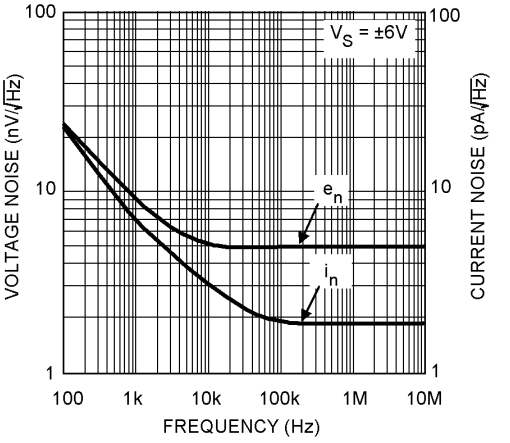
20016608

PSRR vs. Frequency @ 5V



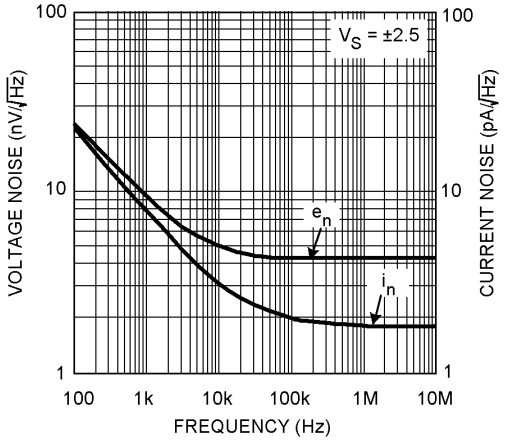
20016607

e_n & i_n vs. Frequency @ 12V



20016610

e_n & i_n vs. Frequency @ 5V



20016609

Application Notes

Thermal Management

The LMH6672 is a high-speed, high power, dual operational amplifier with a very high slew rate and very low distortion. For ease of use, it uses conventional voltage feedback. These characteristics make the LMH6672 ideal for applications where driving low impedances of 25-100Ω such as xDSL and active filters.

A class AB output stage allows the LMH6672 to deliver high currents to low impedance loads with low distortion while consuming low quiescent supply current. For most op-amps, class AB topology means that internal power dissipation is rarely an issue, even with the trend to smaller surface mount packages. However, the LMH6672 has been designed for applications where high levels of power dissipation may be encountered.

Several factors contribute to power dissipation and consequently higher junction temperatures. These factors need to be well understood if the LMH6672 is to perform to specifications in all applications. This section will examine the typical application that is shown on the front page of this data sheet as an example. (Figure 1) Because both amplifiers are in a single package, the calculations will for the total power dissipated by both amplifiers.

There are two separate contributors to the internal power dissipation:

1. The product of the supply voltage and the quiescent current when no signal is being delivered to the external load.

2. The additional power dissipated while delivering power to the external load.

The first of these components appears easy to calculate simply by inspecting the data sheet. The typical quiescent supply current for this part is 6.2mA per amplifier, therefore, with a (6 volt supply, the total power dissipation is:

$P_D = V_S \times 2 \times I_Q = 12 \times (12.4 \times 10^{-3}) = 149$ mW

($V_S = V_{CC} + V_{EE}$)

With a thermal resistance of 172˚C/W for the SOIC package, this level of internal power dissipation will result in a junction temperature (T_J) of 26˚C above ambient.

Using the worst-case maximum supply current of 18mA and an ambient of 85˚C, a similar calculation results in a power dissipation of 216 mW, or a T_J of 122˚C.

This is approaching the maximum allowed T_J of 150˚C before a signal is applied. Fortunately, in normal operation, this term is reduced, for reasons that will soon be explained.

The second contributor to high T_J is the power dissipated internally when power is delivered to the external load. This cause of temperature rise is more difficult to calculate, even when the actual operating conditions are known.

To maintain low distortion, in a Class AB output stage, an idle current, I_Q, is maintained through the output transistors when there is little or no output signal. In the LMH6672, about 4.8 mA of the total quiescent supply current of 12.4 mA flows through the output stages.

Under normal large signal conditions, as the output voltage swings positive, one transistor of the output pair will conduct the load current, while the other transistor shuts off, and dissipates no power. During the negative signal swing this situation is reversed, with the lower transistor sinking the load current while the upper transistor is cut off. The current in each transistor will approximate a half wave rectified version of the total load current.

Because the output stage idle current is now routed into the load, 4.8mA can be subtracted from the quiescent supply current when calculating the quiescent power when the output is driving a load.

The power dissipation caused by driving a load in a DSL application, using a 1:2 turns ratio transformer driving 20 mW into the subscriber line and 20mW into the back termination resistors, can be calculated as follows:

$P_{DRIVER} = P_{TOT} - (P_{TERM} + P_{LINE})$ where

P_{DRIVER} is the LMH6672 power dissipation

P_{TOT} is the total power drawn from the power supply

P_{TERM} is the power dissipated in the back termination resistors

P_{LINE} is the power sent into the subscriber line

At full specified power, $P_{TERM} = P_{LINE} = 20$mW, $P_{TOT} = V_S \times I_S$.

In this application, $V_S = 12$V.

$I_S = I_Q + A_{VG} |I_{OUT}|$.

I_Q = the LMH6672 quiescent current minus the output stage idle current.

$I_Q = 12.4 - 4.8 = 7.6$mA

$A_{VG} |I_{OUT}|$ for a full-rate ADSL CPE application, using a 1:2 turns ratio transformer, is $\sqrt{(40\text{ mW}/50\Omega)} = 28.28$mA RMS.

For a Gaussian signal, which the DMT ADSL signal approximates, $A_{VG} |I_{OUT}| = \sqrt{2/\pi} \times I_{RMS} = 22.6$mA. Therefore, P_{TOT} = (22.6mA + 7.6mA) x 12V = 362mW and P_{DRIVER} is 362-40 = 322mW.

In the SOIC package, with a θ_{JA} of 172˚C/W, this causes a temperature rise of 55˚C. With an ambient temperature at the maximum recommended 85˚C, the T_J is at 140˚C, well below the specified 150˚C maximum.

Even if we assume the absolute maximum I_S over temperature of 18mA, when we scale up the I_Q proportionally to 7mA, the P_{DRIVER} only goes up by 41mW causing a 62˚C rise to 147˚C.

Although very few CPE applications will ever operate in an environment as hot as 85˚C, if a lower T_J is desired or the LMH6672 is to be used in an application where the power dissipation is higher, the PSOP package provides a much lower θ_{JA} of only 58.6˚C/W.

Using the same P_{DRIVER} as above, we find that the temperature rise is only 19˚ and 21˚C, resulting in T_J's in an 85˚C ambient of 104˚C and 106˚C respectively.

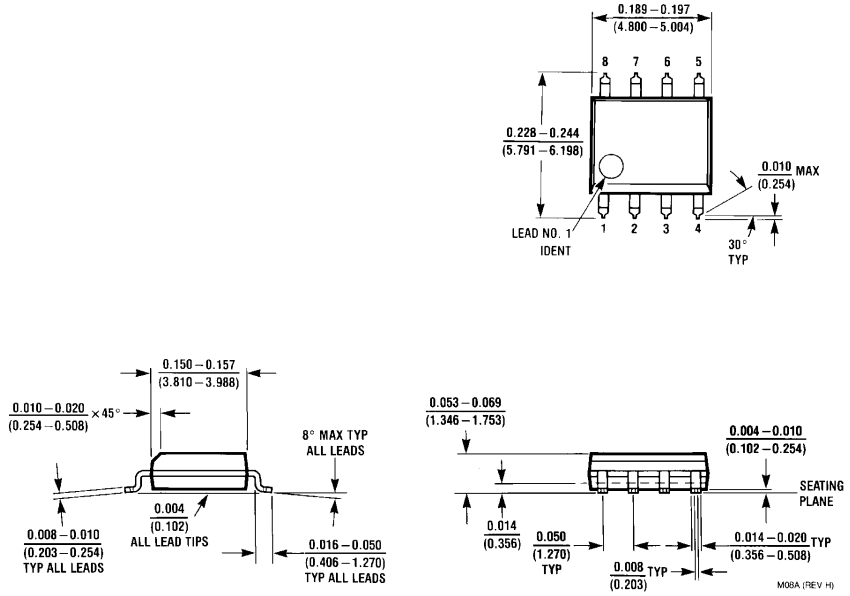
Circuit Layout Considerations

National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Since the exposed PAD (or DAP) of the PSOP and LLP package is internally floating, the footprint for DAP could be connected to ground plane in PCB for better heat dissipation.

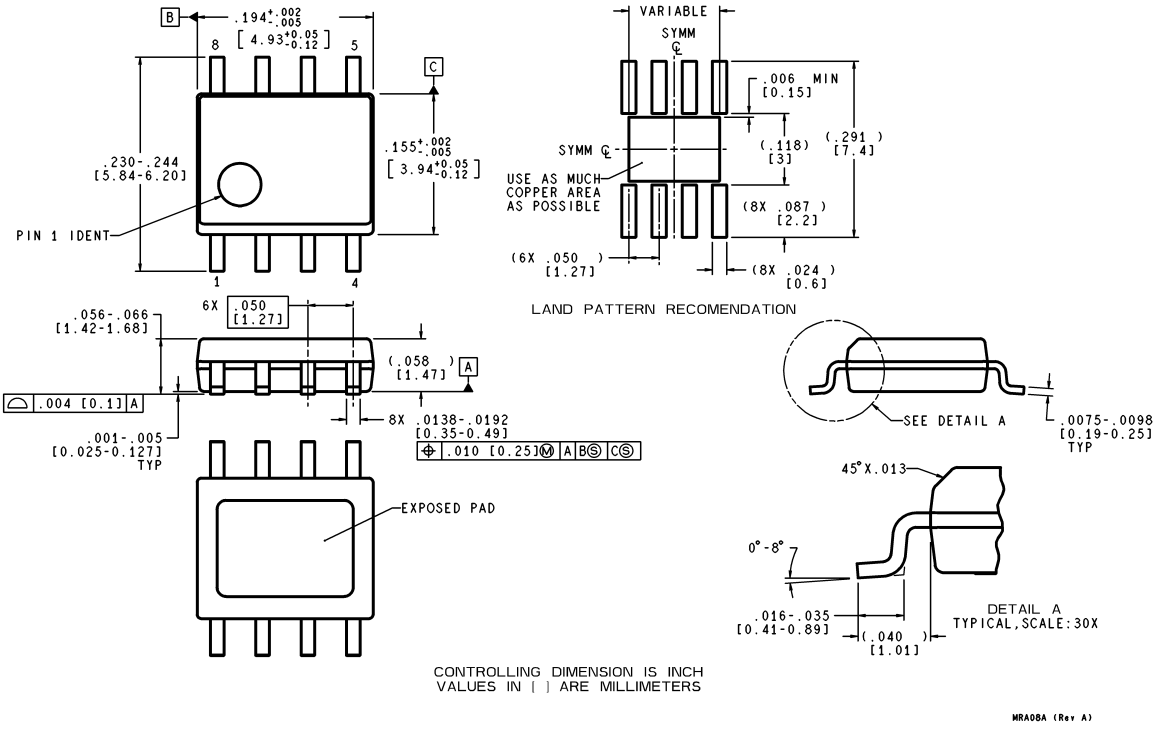
Device	Package	Evaluation Board PN
LMH6672MA	8-Pin SOIC	CLC730036
LMH6672LD	8-Pin LLP	CLC730114
LMH6672MR	8-Pin PSOP	CLC730121

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters)
unless otherwise noted

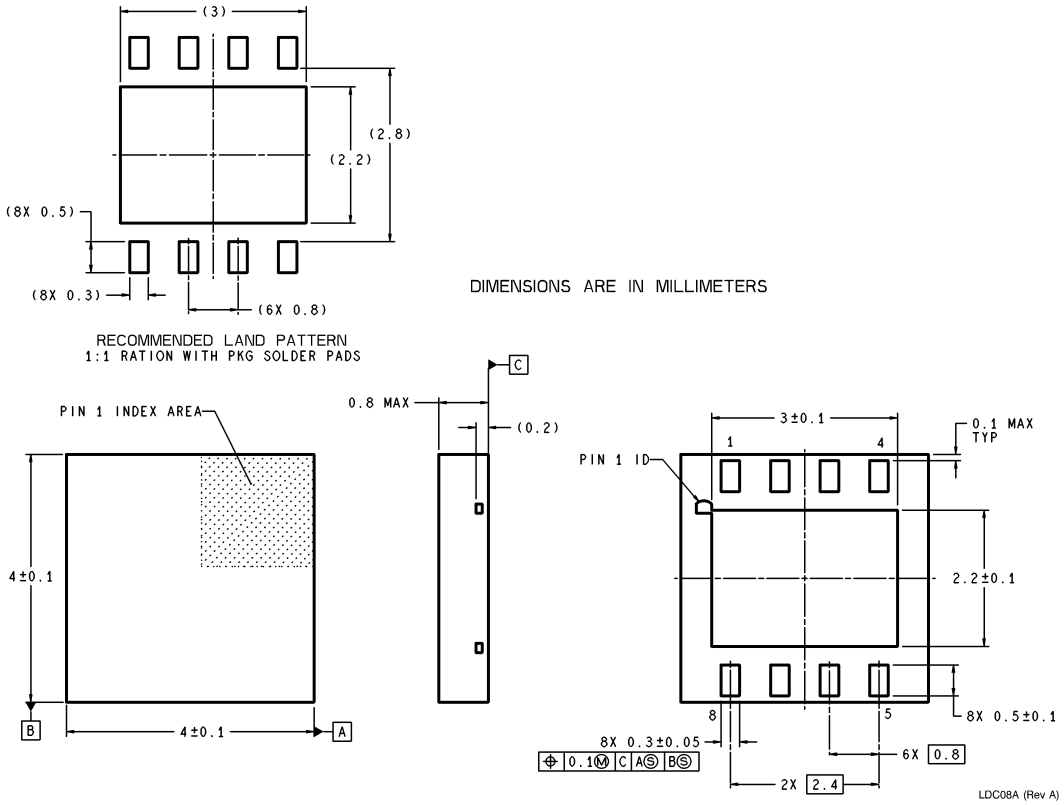


8-Pin SOIC
NS Package Number M08A



8-Pin PSOP
NS Package Number MRA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Pin LLP
NS Package Number LDC08A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507