National Semiconductor

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LM1237
150 MHz I²C Compatible RGB Preamplifier with Internal 254 Character OSD and 4 DACs

General Description

The LM1237 pre-amp is an integrated CMOS CRT preamp. It has an I²C compatible interface which allows control of all the parameters necessary to directly setup and adjust the gain and contrast in the CRT display. Brightness and bias can be controlled through the DAC outputs which are well matched to the LM2479 and LM2480 integrated bias clamp ICs. The LM1237 preamp is also designed to be compatible with the LM246x high gain driver family.

Black level clamping of the video signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional clamp capacitors. Horizontal and vertical blanking of the outputs is provided. Vertical blanking is optional and its duration is register programmable.

The IC is packaged in an industry standard 24 lead DIP molded plastic package.

Features

- I²C compatible microcontroller interface
- Internal 254 character OSD usable as either (a) 190 2-color plus 64 4-color characters, (b) 318 2-color characters, or (c) some combination in between.
- OSD override allows OSD messages to override video and the use of burn-in screens with no video input
- 4 DAC outputs (8-bit resolution) for bus controlled CRT bias and brightness
- Spot killer which blanks the video outputs when V_{CC} falls below the specified threshold
- Suitable for use with discrete or integrated clamp, with software configurable brightness mixer
- H and V blanking (V blanking is optional and has register programmable width)
- Power Saving Mode with 80% power reduction
- Matched to LM246x driver and LM2479/80 drivers

Applications

- Low end 15" and 17" bus controlled monitors with OSD
- 1024x768 displays up to 85 Hz requiring OSD capability
- Very low cost systems with LM246x driver

Block and Connection Diagram

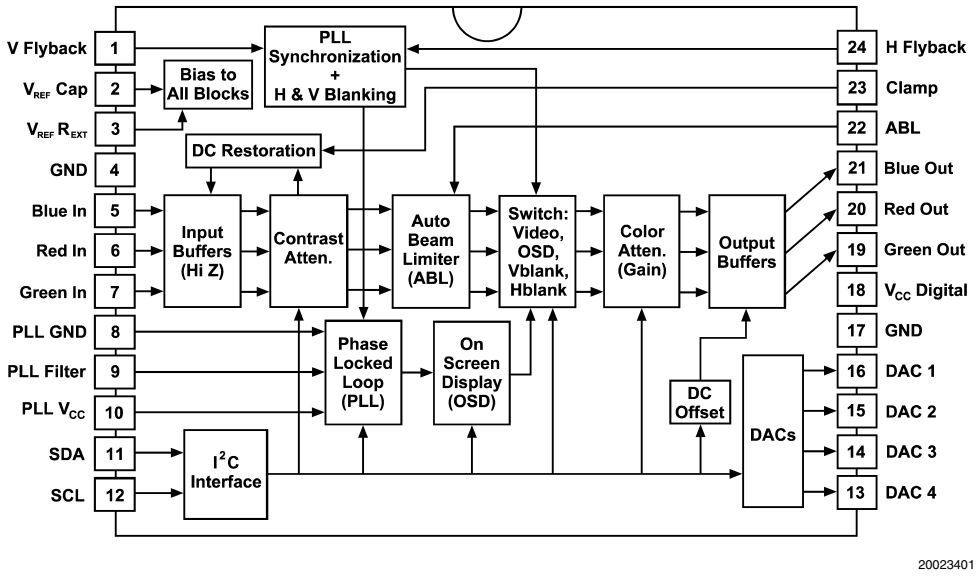


FIGURE 1. Order Number LM1237AAF/NA
See NS Package Number N24D

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, Pins 15 and 19	6.0V
Peak Video DC Output Source Current (Any One Amp) Pins 18, 19 or 20	1.5 mA
Voltage at Any Input Pin (V_{IN})	V_{CC} +0.5 > V_{IN} > −0.5V
Video Inputs (pk-pk)	0.0 < V_{IN} < 1.2V
Thermal Resistance to Ambient (θ_{JA})	51˚C/W
Power Dissipation (P_D) (Above 25˚C Derate Based on θ_{JA} and T_J)	2.4W
Thermal Resistance to case (θ_{JC})	32˚C/W
Junction Temperature (T_J)	150˚C
ESD Susceptibility (Note 4)	3.5 kV
ESD Machine Model (Note 13)	350V
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	265˚C

Operating Ratings (Note 2)

Temperature Range	0˚C to +70˚C
Supply Voltage V_{CC}	4.75V < V_{CC} < 5.25V
Video Inputs (pk-pk)	0.0V < V_{IN} < 1.0V

Video Signal Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.70 V_{P-P}, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. Setting numbers refer to the definitions in Table 1. See Note 7 for Min and Max parameters and Note 6 for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply Current	Test Setting 1, both supplies, no output loading. See Note 8.		170	225	mA
I_{S-PS}	Supply Current, Power Save Mode	Test Setting 1, both supplies, no output loading. See Note 8.		60	82	mA
$V_{O\ BLK}$	Active Video Black Level Output Voltage	Test Setting 4, no AC input signal, DC offset (register 0x8438 set to 0xd5).		1.2		VDC
$V_{O\ BLK\ STEP}$	Active Video Black Level Step Size	Test Setting 4, no AC input signal.		100		mVDC
V_O Max	Maximum Video Output Voltage	Test Setting 3, Video in = 0.70 V_{P-P}	4.0	4.4		V
LE	Linearity Error	Test Setting 4, staircase input signal (see Note 9).		5		%
t_r	Video Rise Time	Note 5, 10% to 90%, Test Setting 4, AC input signal.		3.1		ns
OS_R	Rising Edge Overshoot	Note 5, Test Setting 4, AC input signal.		2		%
t_f	Video Fall Time	Note 5, 90% to 10%, Test Setting 4, AC input signal.		2.9		ns
OS_F	Falling Edge Overshoot	Note 5, Test Setting 4, AC input signal.		2		%
BW	Channel bandwidth (−3 dB)	Note 5, Test Setting 4, AC input signal.		150		MHz
V_{SEP} 10 kHz	Video Amplifier 10 kHz Isolation	Note 14, Test Setting 8.		−60		dB
V_{SEP} 10 MHz	Video Amplifier 10 MHz Isolation	Note 14, Test Setting 8.		−50		dB
A_V Max	Maximum Voltage Gain	Test Setting 8, AC input signal.	3.8	4.2		V/V
A_V C-50%	Contrast Attenuation @ 50%	Test Setting 5, AC input signal.		−5.2		dB
A_V Min/A_V Max	Maximum Contrast Attenuation in dB	Test Setting 2, AC input signal.		−20		dB
A_V G-50%	Gain Attenuation @ 50%	Test Setting 6, AC input signal.		−3.6		dB
A_V G-Min	Maximum Gain Attenuation	Test Setting 7, AC input signal.		−10		dB
A_V Match	Maximum Gain Match between channels	Test Setting 3, AC input signal.		±0.5		dB

Video Signal Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.70 V_{P-P}, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. Setting numbers refer to the definitions in Table 1. See Note 7 for Min and Max parameters and Note 6 for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A_V Track	Gain Change between channels	Tracking when changing from Test Setting 8 to Test Setting 5. See Note 11.		±0.5		dB
V_{ABL} TH	ABL Control Range upper limit	Note 12, Test Setting 4, AC input signal.		4.8		V
V_{ABL} Range	ABL Gain Reduction Range	Note 12, Test Setting 4, AC input signal.		2.8		V
$A_{V\ 3.5}/A_{V\ Max}$	ABL Gain Reduction at 3.5V	Note 12, Test Setting 4, AC input signal. V_{ABL} = 3.5V		–3		dB
$A_{V\ 2.0}/A_{V\ Max}$	ABL Gain Reduction at 2.0V	Note 12, Test Setting 4, AC input signal. V_{ABL} = 2.0V		–11		dB
I_{ABL} Active	ABL Input bias current during ABL	Note 12, Test Setting 4, AC input signal. V_{ABL} = V_{ABL} MIN GAIN			10	µA
I_{ABL} Max	ABL input current sink capability	Note 12, Test Setting 4, AC input signal.			1.0	mA
V_{ABL} Max	Maximum ABL Input voltage during clamping	Note 12, Test Setting 4, AC input signal. I_{ABL} = I_{ABL} MAX			V_{CC} + 0.1	V
A_V ABL Track	ABL Gain Tracking Error	Note 9, Test Setting 4, 0.7 V_{P-P} input signal, ABL voltage set to 4.5V and 2.5V.			4.5	%
R_{IP}	Minimum Input resistance pins 5, 6, 7.	Test Setting 4.		20		MΩ

OSD Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V. See Note 7 for Min and Max parameters and Note 6 for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OSDHIGH}$ max	Maximum OSD Level with OSD Contrast 11	Palette Set at 111, OSD Contrast = 11, Test Setting 3		3.8		V
$V_{OSDHIGH}$ 10	Maximum OSD Level with OSD Contrast 10	Palette Set at 111, OSD Contrast = 10, Test Setting 3		3.1		V
$V_{OSDHIGH}$ 01	Maximum OSD Level with OSD Contrast 01	Palette Set at 111, OSD Contrast = 01, Test Setting 3		2.4		V
$V_{OSDHIGH}$ 00	Maximum OSD Level with OSD Contrast 00	Palette Set at 111, OSD Contrast = 00, Test Setting 3		1.7		V
ΔV_{OSD} (Black)	Difference between OSD Black Level and Video Black Level (same channel)	Register 08=0x18, Input Video = Black, Same Channel, Test Setting 8		20		mV
ΔV_{OSD} (White)	Output Match between Channels	Palette Set at 111, OSD Contrast = 11, Maximum difference between R, G and B		3		%
$V_{OSD\text{-}out}$ (Track)	Output Variation between Channels	OSD contrast varied from max to min		3		%

DAC Output Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See Note 7 for Min and Max parameters and Note 6 for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{Min\ DAC}$	Min output voltage of DAC	Register Value = 0x00		0.5	0.7	V

DAC Output Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See Note 7 for Min and Max parameters and Note 6 for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{Max\ DAC}$ Mode 00	Max output voltage of DAC	Register Value = 0xFF, DCF[1:0] = 00b	3.7	4.2		V
$V_{Max\ DAC}$ Mode 01	Max output voltage of DAC in DCF mode 01	Register Value = 0xFF, DCF[1:0] = 01b	1.85	2.35		V
$\Delta V_{Max\ DAC}$ (Temp)	Variation in voltage of DAC with temperature	0 < T < 70˚C ambient		±0.5		mV/˚C
$\Delta V_{Max\ DAC}$ (V_{CC})	Variation in voltage of DAC with V_{CC}	4.75 < V_{CC} < 5.25V		±50		mV/V
Linearity	Linearity of DAC over its range			5		%
Monotonicity	Monotonicity of the DAC	Excluding dead zones		±0.5		LSB
I_{MAX}	Max Load Current		–1.0		1.0	mA

System Interface Signal Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See Note 7 for Min and Max parameters and Note 6 for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VTH+}	VFLYBACK positive switching guarantee.	Vertical Blanking triggered	2.0			V
V_{SPOT}	Spot Killer Voltage	Note 17, V_{CC} Adjusted to Activate	3.4	3.9	4.25	V
V_{Ref}	V_{Ref} Output Voltage		1.25	1.45	1.65	V
V_{IL} (SCL, SDA)	Logic Low Input Voltage		–0.5		1.5	V
V_{IH} (SCL, SDA)	Logic High Input Voltage		3.0		V_{CC} + 0.5	V
I_L (SCL, SDA)	Logic Low Input Current	SDA or SCL, Input Voltage = 0.4V		±10		µA
I_H (SCL, SDA)	Logic High Input Voltage	SDA or SCL, Input Voltage = 4.5V		±10		µA
V_{OL} (SCL, SDA)	Logic Low Output Voltage	I_O = 3 mA		0.5		V
f_H Min	Minimum Horizontal Frequency	PLL & OSD Operational; PLL Range = 0		25		kHz
f_H Max	Maximum Horizontal Frequency	PLL & OSD Operational; PLL Range = 3		110		kHz
$I_{HFB\ IN}$ Max	Horizontal Flyback Input Current	Absolute Maximum During Flyback			5	mA
I_{IN}	Peak Current during flyback	Design Value		4		mA
$I_{HFB\ OUT}$ Max	Horizontal Flyback Input Current	Absolute Maximum During Scan	–700			µA
I_{OUT}	Peak Current during Scan	Design Value		–550		µA
$I_{IN\ THRESHOLD}$	I_{IN} H-Blank Detection Threshold			0		µA
$t_{H\text{-}BLANK\ ON}$	H-Blank Time Delay - On	+ Zero crossing of I_{HFB} to 50% of output blanking start. I_{24} = +1.5mA		45		ns
$t_{H\text{-}BLANK\ OFF}$	H-Blank Time Delay - Off	– Zero crossing of I_{HFB} to 50% of output blanking end. I_{24} = –100µA		85		ns
V_{BLANK} Max	Maximum Video Blanking Level	Test Setting 4, AC input signal.	0		0.25	V
$f_{FREERUN}$	Free Run H Frequency, including H Blank			42		kHz
$t_{PW\ CLAMP}$	Minimum Clamp Pulse Width	See Note 15	200			ns
$V_{CLAMP\ MAX}$	Maximum Low Level Clamp Pulse Voltage	Video Clamp Functioning			2.0	V
$V_{CLAMP\ MIN}$	Minimum High Level Clamp Pulse Voltage	Video Clamp Functioning	3.0			V
I_{CLAMP} Low	Clamp Gate Low Input Current	V_{23} = 2V		–0.4		µA
I_{CLAMP} High	Clamp Gate High Input Current	V_{23} = 3V		0.4		µA

System Interface Signal Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See Note 7 for Min and Max parameters and Note 6 for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{CLAMP-VIDEO}$	Time from End of Clamp Pulse to Start of Video	Referenced to Blue, Red and Green inputs	50			ns

Note 1: Limits of Absolute Maximum Ratings indicate below which damage to the device must not occur.

Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Input from signal generator: t_r, t_f < 1 ns.

Note 6: Typical specifications are specified at +25˚C and represent the most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL; (Average Outgoing Quality Level).

Note 8: The supply current specified is the quiescent current for V_{CC} and 5V Dig with R_L = ∞. Load resistors are not required and are not used in the test circuit, therefore all the supply current is used by the pre-amp.

Note 9: Linearity Error is the maximum variation in step height of a 16 step staircase input signal waveform with a 0.7 V_{P-P} level at the input. All 16 steps equal, with each at least 100 ns in duration.

Note 10: dt/dV_{CC} = 200*(t5.5V–t4.5V)/ ((t5.5V + t4.5V)) %/V, where:

t5.5V is the rise or fall time at V_{CC} = 5.5V, and t4.5V is the rise or fall time at V_{CC} = 4.5V.

Note 11: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three gain stages. It is the difference in gain change between any two amplifiers with the contrast set to A_VC–50% and measured relative to the A_V max condition. For example, at A_V max the three amplifiers' gains might be 12.1 dB, 11.9 dB, and 11.8 dB and change to 2.2 dB, 1.9 dB and 1.7 dB respectively for contrast set to A_VC–50%. This yields a typical gain change of 10.0 dB with a tracking change of ±0.2 dB.

Note 12: ABL should provide smooth decrease in gain over the operational range of 0 dB to –5 dB

$\Delta A_{ABL} = A(V_{ABL} = V_{ABL\ MAX\ GAIN}) - A\ (V_{ABL} = V_{ABL\ MIN\ GAIN})$

Beyond –5 dB the gain characteristics, linearity and pulse response may depart from normal values.

Note 13: Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specific voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Note 14: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for $V_{SEP\ 10\ MHZ}$.

Note 15: A minimum pulse width of 200 ns is the guaranteed minimum for a horizontal line of 15 kHz. This limit is guaranteed by design. If a lower line rate is used then a longer clamp pulse may be required.

Note 16: Adjust input frequency from 10 MHz (A_V max reference level) to the –3 dB corner frequency ($f_{-3\ dB}$).

Note 17: Once the spot killer has been activated, the LM1237 remains in the off state until V_{CC} is cycled (reduced below 0.5V andthen restored to 5V).

Hexadecimal and Binary Notation

Hexadecimal numbers appear frequently throughout this document, representing slave and register addresses, and register values. These appear in the format "0x...". For example, the slave address for writing the registers of the LM1237 is hexadecimal BA, written as 0xBA. On the other hand, binary values, where the individual bit values are shown, are indicated by a trailing "b". For example, 0xBA is equal to 10111010b. A subset of bits within a register is referred to by the bit numbers in brackets following the register value. For example, the OSD contrast bits are the fourth and fifth bits of register 0x8438. Since the first bit is bit 0, the OSD contrast register is 0x8438[4:3].

Register Test Settings

Table 1 shows the definitions of the Test Settings 1–8 referred to in the specifications sections. Each test setting is a combination of five hexadecimal register values, Contrast, Gain (Blue, Red, Green) and DC offset.

TABLE 1. Test Setting Definitions

Control	No. of Bits	Test Settings							
		1	2	3	4	5	6	7	8
Contrast	7	0x7F (Max)	0x00 Min	0x7F (Max)	0x7F (Max)	0x40 (50.4%)	0x7F (Max)	0x7F (Max)	0x7F (Max)
B, R, G Gain	7	0x7F (Max)	0x7F (Max)	0x7F (Max)	Set V_O to 2 V_{P-P}	0x7F (Max)	0x40 (50%)	0x00 (Min)	0x7F (Max)
DC Offset	3	0x00 (Min)	0x05	0x07 (Max)	0x05	0x05	0x05	0x05	0x05

LM1253A Compatibility

In order to maintain register compatibility with the LM1253A preamplifier datasheet assignments for bias and brightness, the color assignments are recommended as shown in Table 2. If datasheet compatibility is not required, then the DAC assignments can be arbitrary.

TABLE 2. LM1253A Compatibility

	DAC Bias Outputs			
LM1237 Pin:	DAC 1	DAC 2	DAC 3	DAC 4
Assignment:	Blue	Green	Red	Brightness

OSD vs Video Intensity

The OSD amplitude has been increased over the LM1253A level. During monitor alignment, the three gain registers are used to achieve the desired front of screen color balance. This also causes the OSD channels to be adjusted accordingly, since these are inserted into the video channels prior to the gain attenuators. This provides the means to fine tune the intensity of the OSD relative to the video as follows. If a typical starting point for the alignment is to have the gains at maximum (0x7F) and the contrast at 0x55, the resultant OSD intensity will be higher than if the starting point is with the gains at 0x55 and the contrast at maximum (0x7F). This tradeoff allows fine tuning the final OSD intensity relative to the video. In addition, the OSD contrast register, 0x8438 [4:3], provides 4 major increments of intensity. Together, these allow setting the OSD intensity to the most pleasing level.

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified

System Interface Signals

The Horizontal and Vertical Blanking and the Clamping input signals are important for proper functionality of the LM1237. Both blanking inputs must be present for OSD synchronization. In addition, the Horizontal blanking input also assists in setting the proper cathode black level, along with the Clamping pulse. The Vertical blanking input initiates a blanking level at the LM1237 outputs which is programmable from 3 to 127 lines (we recommend at least 10). This can be optionally disabled so there is no vertical blanking.

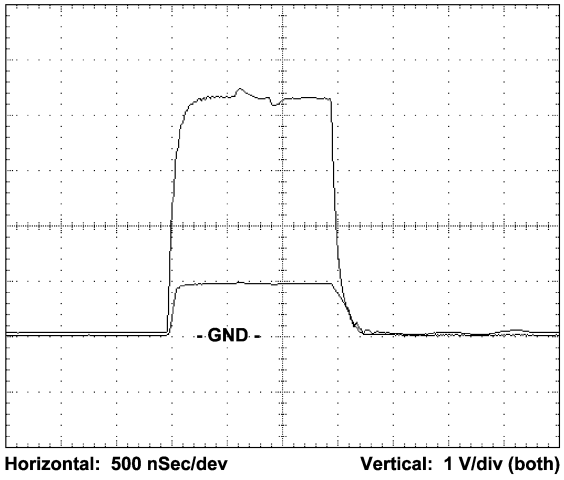


FIGURE 2. Logic Horizontal Blanking

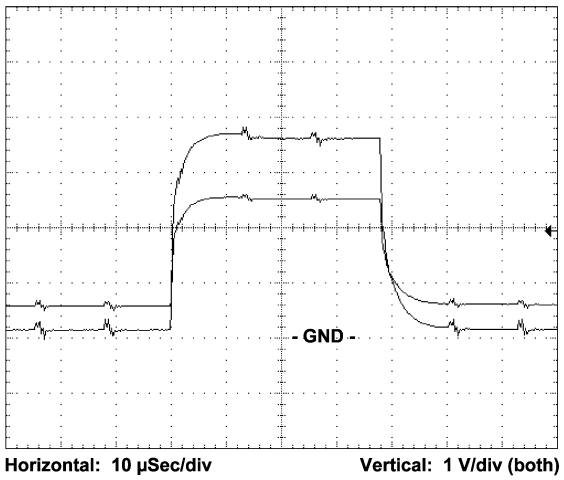


FIGURE 3. Logic Vertical Blanking

Figure 2 and *Figure 3* show the case where the Horizontal and Vertical inputs are logic levels. *Figure 2* shows the smaller pin 24 voltage superimposed on the horizontal blanking pulse input to the neck board with R_H = 4.7K and C_{17} = 0.1µF. Note where the voltage at pin 24 is clamped to about 1 volt when the pin is sinking current. *Figure 3* shows the smaller pin 1 voltage superimposed on the vertical blanking input to the neck board with C_4 jumpered and R_V = 4.7K. These component values correspond to the application circuit of *Figure 15*.

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

Figure 4 and *Figure 5* show the case where the horizontal and vertical inputs are from deflection. *Figure 4* shows the pin 24 voltage which is derived from a horizontal flyback pulse of 35 volts peak to peak with R_H = 8.2K and C_{17} jumpered. *Figure 5* shows the pin 1 voltage which is derived from a vertical flyback pulse of 55 volts peak to peak with C_4 = 1500pF and R_V = 120K.

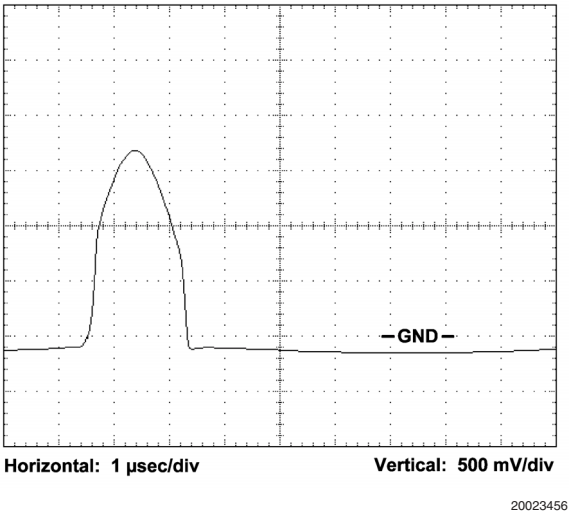


FIGURE 4. Deflection Horizonal Blanking

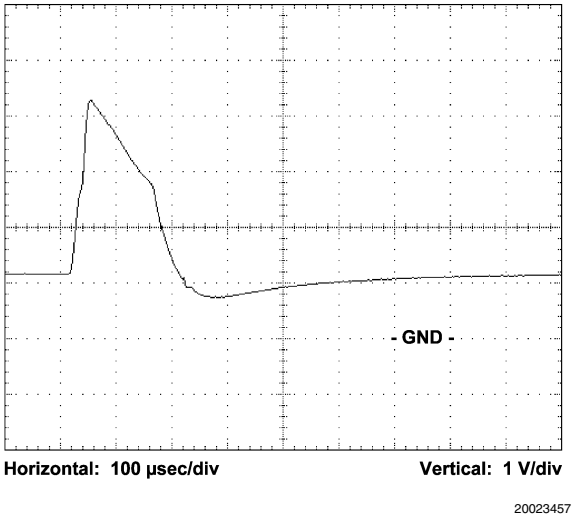


FIGURE 5. Deflection Vertical Blanking

Figure 6 shows the pin 23 clamp input voltage superimposed on the neck board clamp logic input pulse. R_{31} = 1K and should be chosen to limit the pin 23 voltage to about 2.5V peak to peak. This corresponds to the application circuit given in *Figure 9*.

Cathode Response

Figure 7 shows the response at the red cathode for the application circuit in *Figures 9, 10*. The input video risetime is 1.5 nanoseconds. The resulting leading edge has a 7.1 nanosecond risetime and a 7.6% overshoot, while the trailing edge has a 7.1 nanosecond risetime and a 6.9% overshoot with an LM2467 driver.

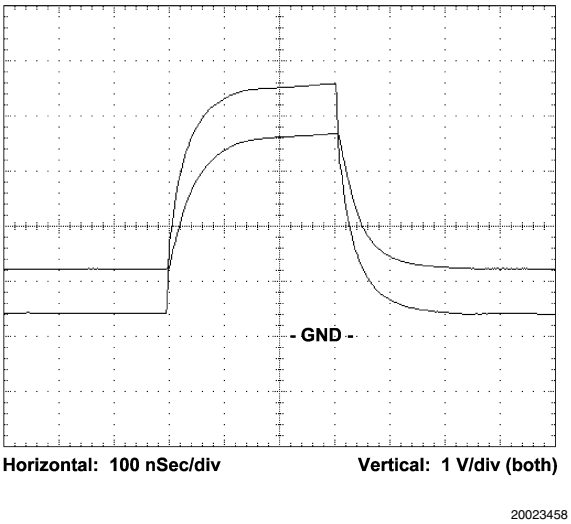


FIGURE 6. Logic Clamp Pulse

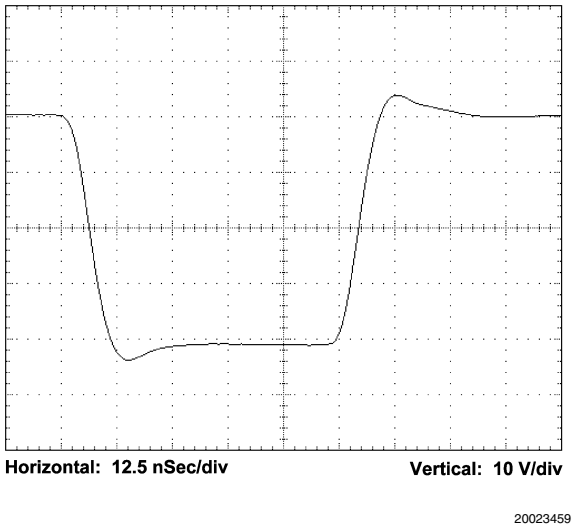


FIGURE 7. Red Cathode Response

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

ABL Gain Reduction

The ABL function reduces the contrast level of the LM1237 as the voltage on pin 22 is lowered from V_{CC} to around 2 volts. *Figure 8* shows the amount of gain reduction as the voltage is lowered from V_{CC} (5.0V) to 2V. The gain reduction is small until V_{22} reaches the knee anound 3.7V, where the slope increases. Many system designs will require about 3 to 5 dB of gain reduction in full beam limiting. Additional attenuation is possible, and can be used in special circumstances. However, in this case, video performance such as video linearity and tracking between channels will tend to depart from normal specifications.

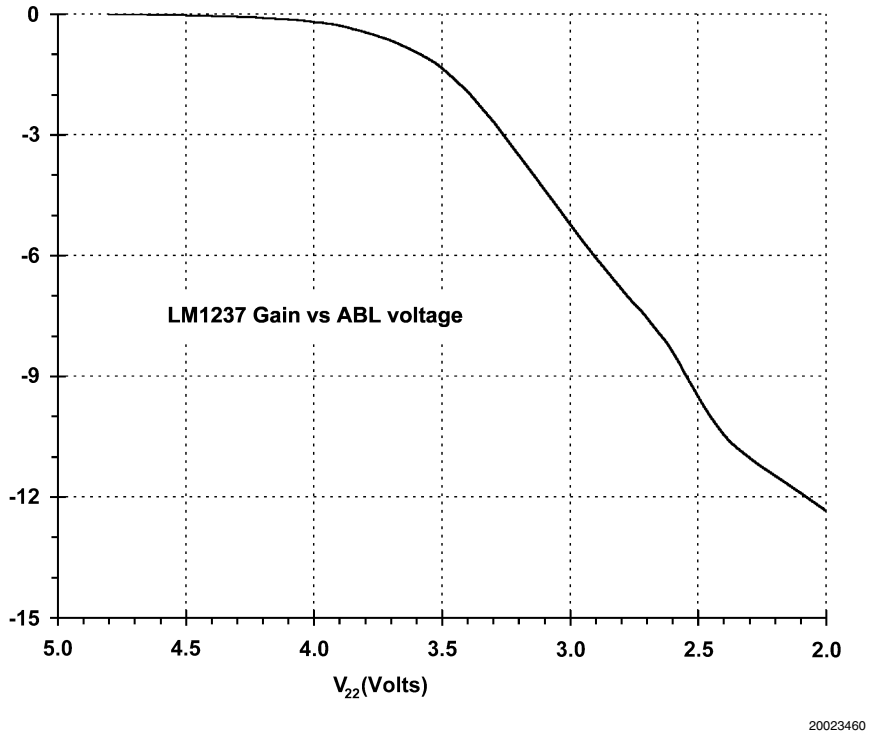


FIGURE 8. ABL Gain Reduction Curve

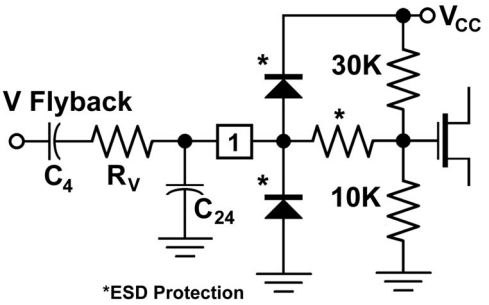
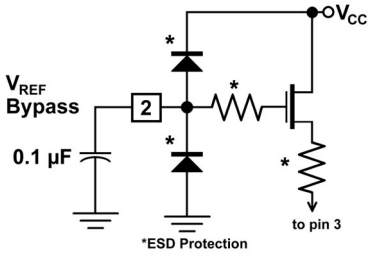
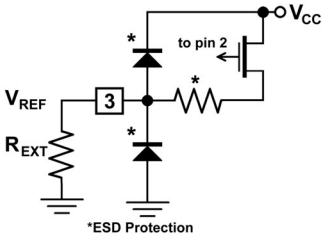
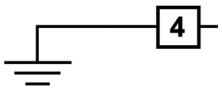
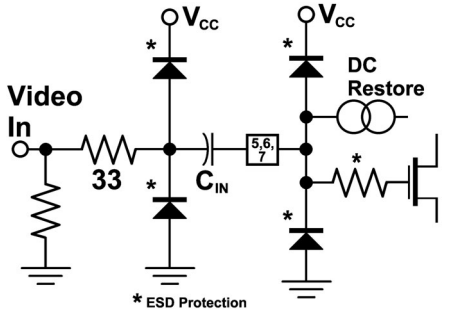
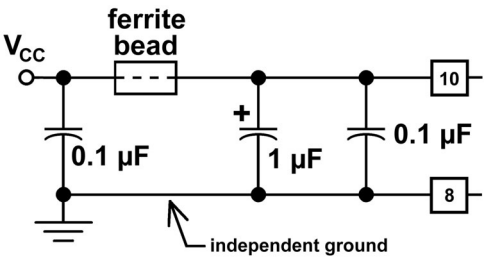
OSD Phase Locked Loop

Table 3 shows the recommended horizontal scan rate ranges (in kHz) for each combination of PLL register setting, 0x843E [1:0], and the pixels per line register setting, 0x8401 [7:5]. These ranges are recommended for chip ambient temperatures of 50°C to 70°C. While the OSD PLL will lock for other register combinations and at scan rates outside these ranges, the performance of the loop will be improved if these recommendations are followed. NR means the combination of PLL and PPL is not recommended for any scan rate.

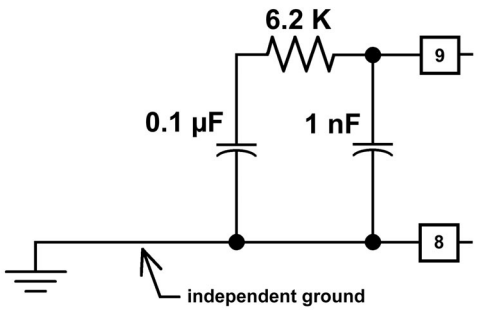
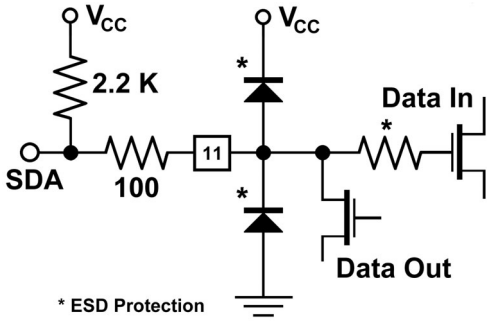
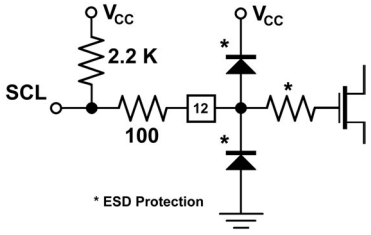
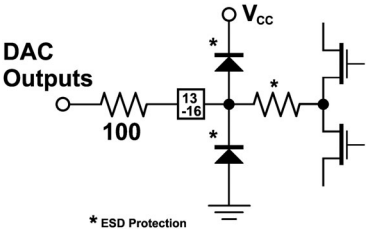
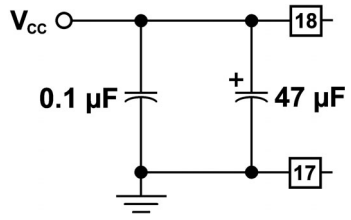
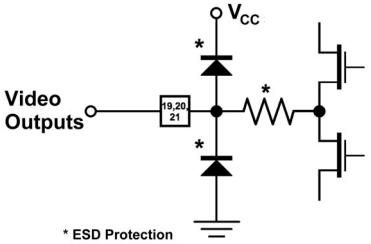
TABLE 3. OSD Register recommendations

	PPL=0	PPL=1	PPL=2	PPL=3	PPL=4	PPL=5	PPL=6	PPL=7
PLL=1	27 - 57	26 - 49	25 - 45	25 - 41	25 - 37	25 - 34	25 - 32	25 - 30
PLL=2	NR	NR	45 - 89	41 - 82	37 - 75	34 - 69	32 - 64	30 - 60
PLL=3	NR	NR	NR	82 - 110	75 - 110	69 - 110	64 - 110	60 - 110

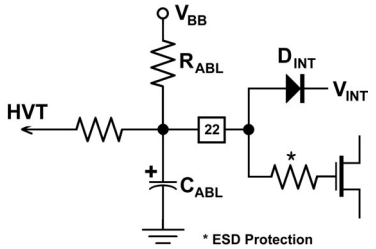
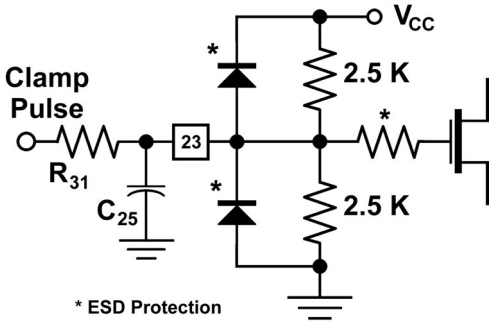
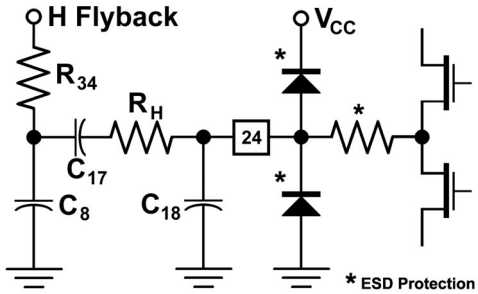
Pin Descriptions and Application Information

Pin No.	Pin Name	Schematic	Description
1	V Flyback		Required for OSD synchronization and is also used for vertical blanking of the video outputs. The actual switching threshold is about 35% of V_{CC}. For logic level inputs C_4 can be a jumper, but for flyback inputs, an AC coupled differentiator is recommended, where R_V is large enough to prevent the voltage at pin 1 from exceeding V_{CC} or going below GND. C_4 should be small enough to flatten the vertical rate ramp at pin 1. C_{24} may be needed to reduce noise.
2	V_{REF} Bypass		Provides filtering for the internal voltage which sets the internal bias current in conjunction with R_{EXT}. A minimum of 0.1 µF is recommended for proper filtering. This capacitor should be placed as close to pin 2 and the pin 4 ground return as possible.
3	V_{REF} Current Set		External resistor, 10k 1%, sets the internal bias current level for optimum performance of the LM1237. This resistor should be placed as close to pin 3 and the pin 4 ground return as possible.
4	Analog Ground		This is the ground for the input analog portions of the LM1237 internal circuitry.
5 6 7	Blue Video In Red Video In Green Video In		These video inputs must be AC coupled with a .0047 µF cap. Internal DC restoration is done at these inputs. A series resistor of about 33Ω and external ESD protection diodes should also be used for protection from ESD damage.
8 10	Digital Ground PLL V_{CC}		The ground pin should be connected to the rest of the circuit ground by a short but independent PCB trace to prevent contamination by extraneous signals. The V_{CC} pin should be isolated from the rest of the V_{CC} line by a ferrite bead and bypassed to pin 8 with an electrolytic capacitor and a high frequency ceramic.

Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
9	PLL Filter		Recommended topology and values are shown to the left. It is recommended that both filter branches be bypassed to the independent ground as close to pin 8 as possible. Great care should be taken to prevent external signals from coupling into this filter from video, I^2C, etc.
11	SDA		The I^2C compatible data line. A pull-up resistor of about 2 Kohms should be connected between this pin and V_{CC}. A resistor of at least 100Ω should be connected in series with the data line for additional ESD protection.
12	SCL		The I^2C compatible clock line. A pull-up resistor of about 2 kΩ should be connected between this pin and V_{CC}. A resistor of at least 100Ω should be connected in series with the clock line for additional ESD protection.
13 14 15 16	DAC 4 Output DAC 2 Output DAC 3 Output DAC 1 Output		DAC outputs for cathode cut-off adjustments and brightness control. DAC 4 can be set to change the outputs of the other three DACs, acting as a brightness control. The DAC values and the special DAC 4 function are set through the I^2C compatible bus. A resistor of at least 100Ω should be connected in series with these outputs for additional ESD protection.
17 18	Ground V_{CC}		Ground pin for the output analog portion of the LM1237 circuitry, and power supply pin for both analog and digital sections of the LM1237. Note the recommended charge storage and high frequency capacitors which should be as close to pins 17 and 18 as possible.
19 20 21	Green Output Red Output Blue Output		These are the three video output pins. They are intended to drive the LM246x family of cathode drivers. Nominally, about 2V peak to peak will produce 40V peak to peak of cathode drive.

Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
22	ABL		The Automatic Beam Limiter input is biased to the desired beam current limit by R_{ABL} and V_{BB} and normally keeps D_{INT} forward biased. When the current resupplying the CRT capacitance (averaged by C_{ABL}) exceeds this limit, then D_{INT} begins to turn off and the voltage at pin 22 begins to drop. The LM1237 then lowers the gain of the three video channels until the beam current reaches an equilibrium value.
23	CLAMP		This pin accepts either TTL or CMOS logic levels. The internal switching threshold is approximately one-half of V_{CC}. An external series resistor, R_{31}, of about 1k is recommended to avoid overdriving the input devices. In any event, R_{EXT} must be large enough to prevent the voltage at pin 23 from going higher than V_{CC} or below GND.
24	H Flyback		Proper operation requires current reversal. R_H should be large enough to limit the peak current at pin 24 to about +4 ma during blanking, and −500 µA during scan. C_{17} is usually needed for logic level inputs and should be large enough to make the time constant, R_HC_{17} significantly larger than the horizontal period. R_{34} and C_8 are typically 300 ohms and 330 pf when the flyback waveform has ringing and needs filtering. C_{18} may be needed to filter extraneous noise and can be up to 100 pF.

Schematic Diagram

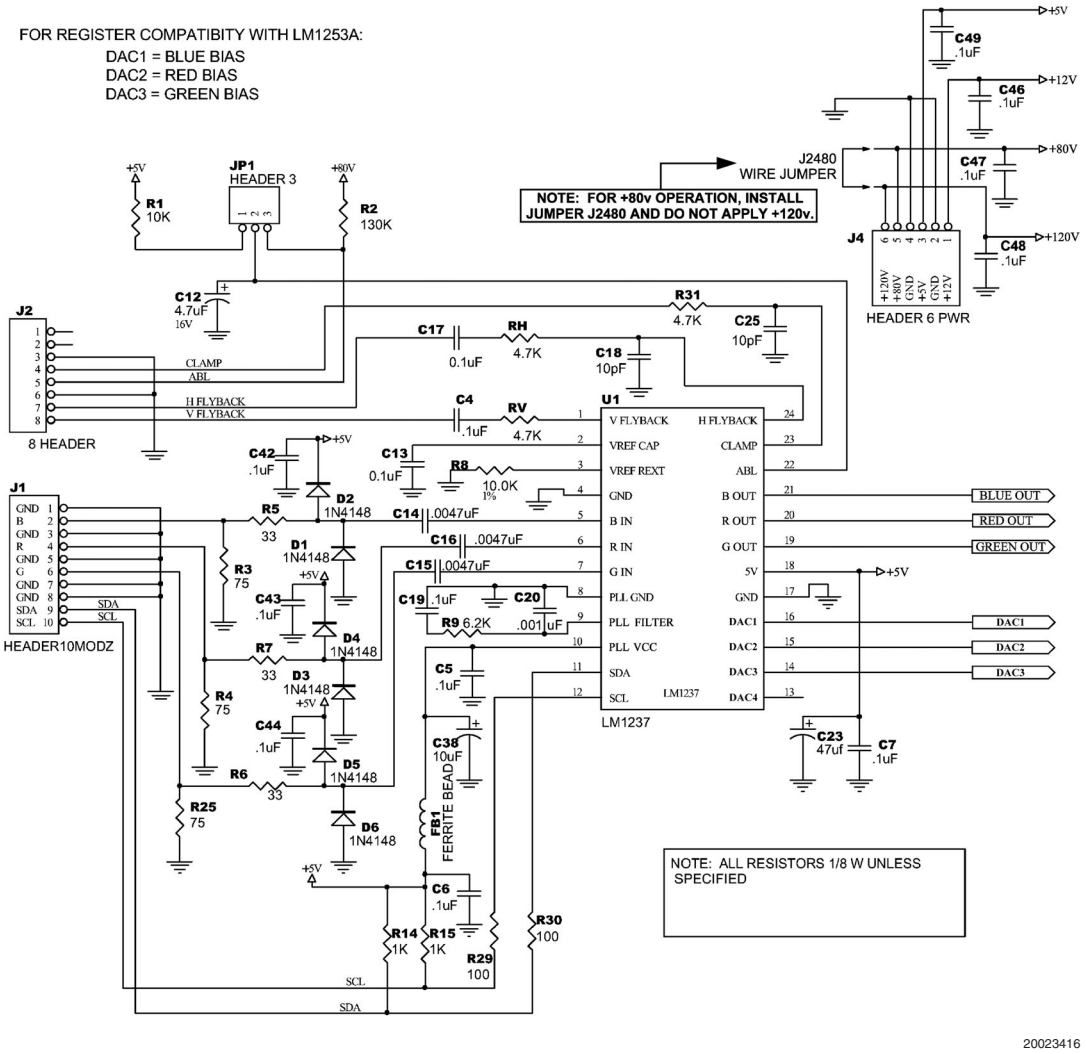
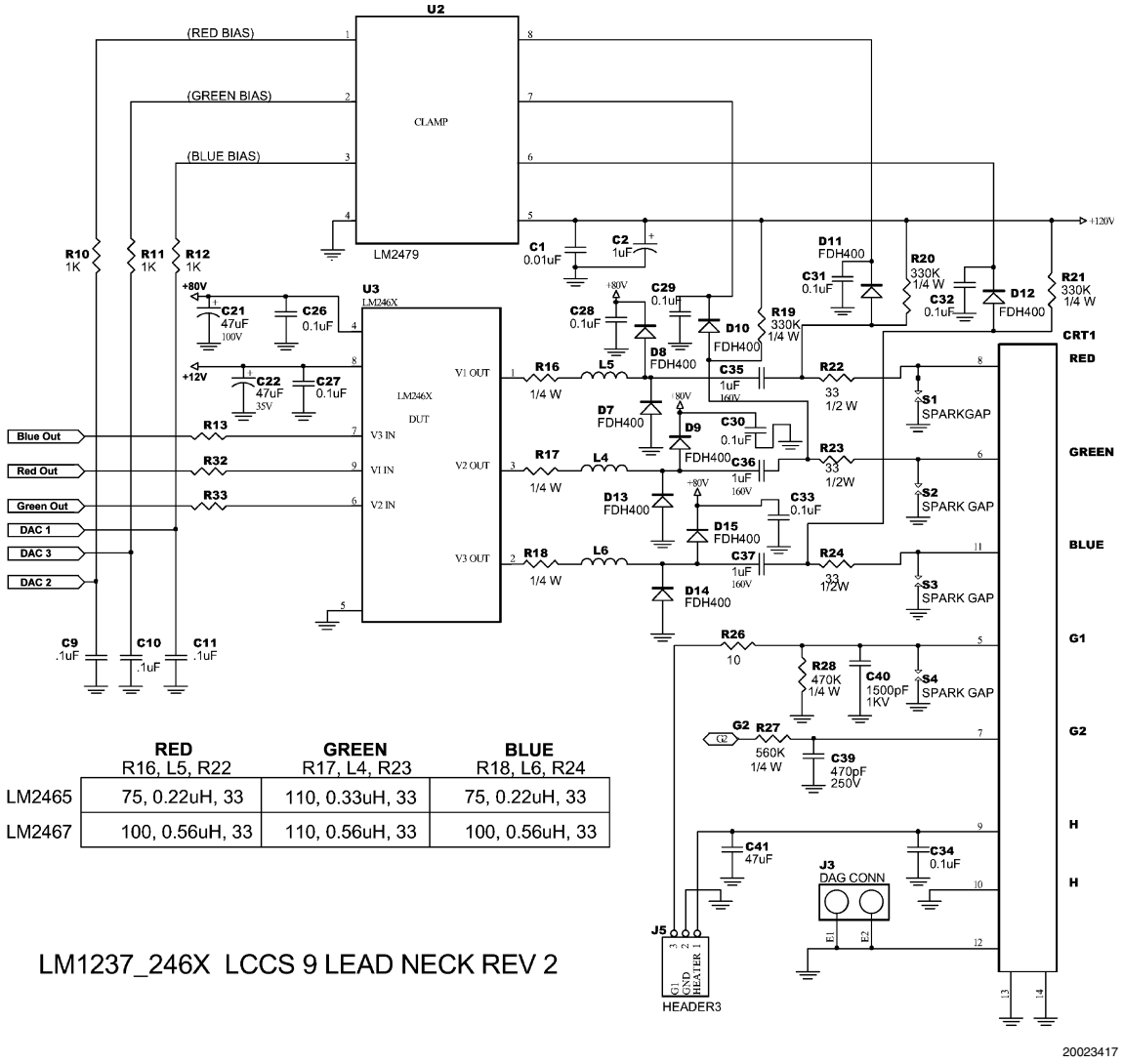


FIGURE 9. LM123x-LM246x Demo Board Schematic

Schematic Diagram



	RED R16, L5, R22	GREEN R17, L4, R23	BLUE R18, L6, R24
LM2465	75, 0.22uH, 33	110, 0.33uH, 33	75, 0.22uH, 33
LM2467	100, 0.56uH, 33	110, 0.56uH, 33	100, 0.56uH, 33

FIGURE 10. LM123x-LM246x Demo Board Schematic (continued)

PCB Layout

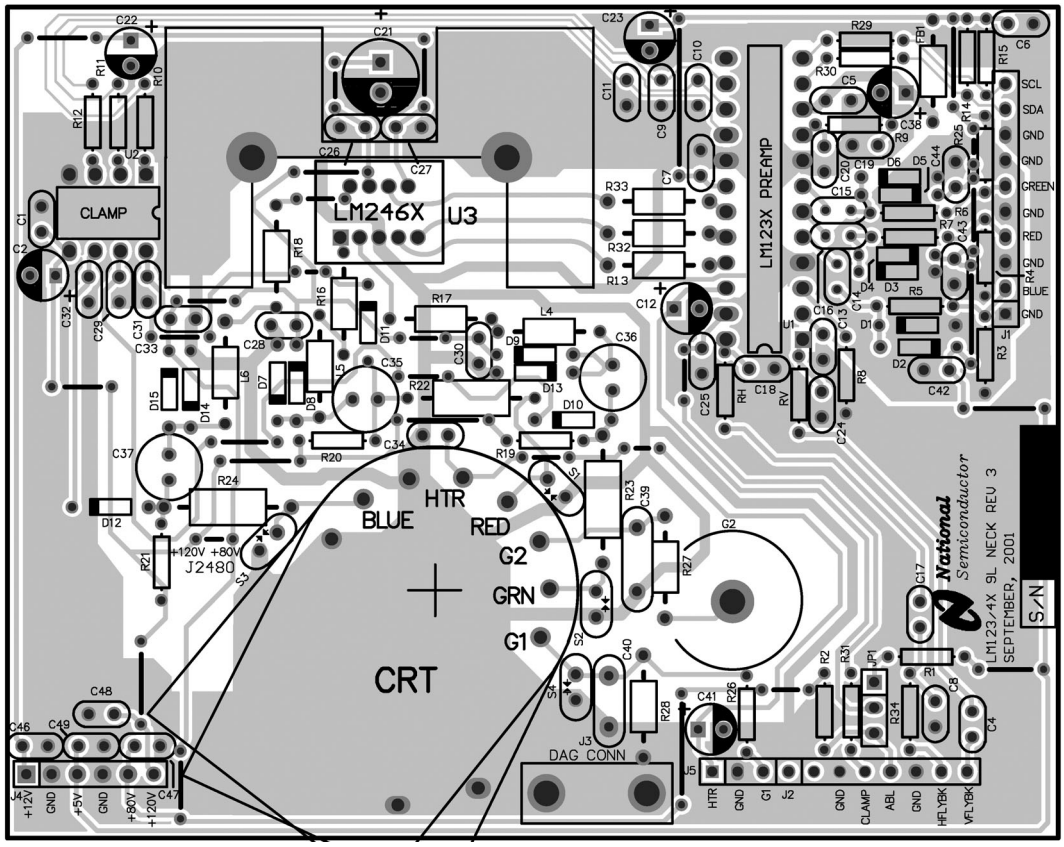


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FIGURE 11. LM123x-LM246x Demo Board Layout

OSD Generator Operation

PAGE OPERATION

Figure 12. shows the block diagram of the OSD generator.

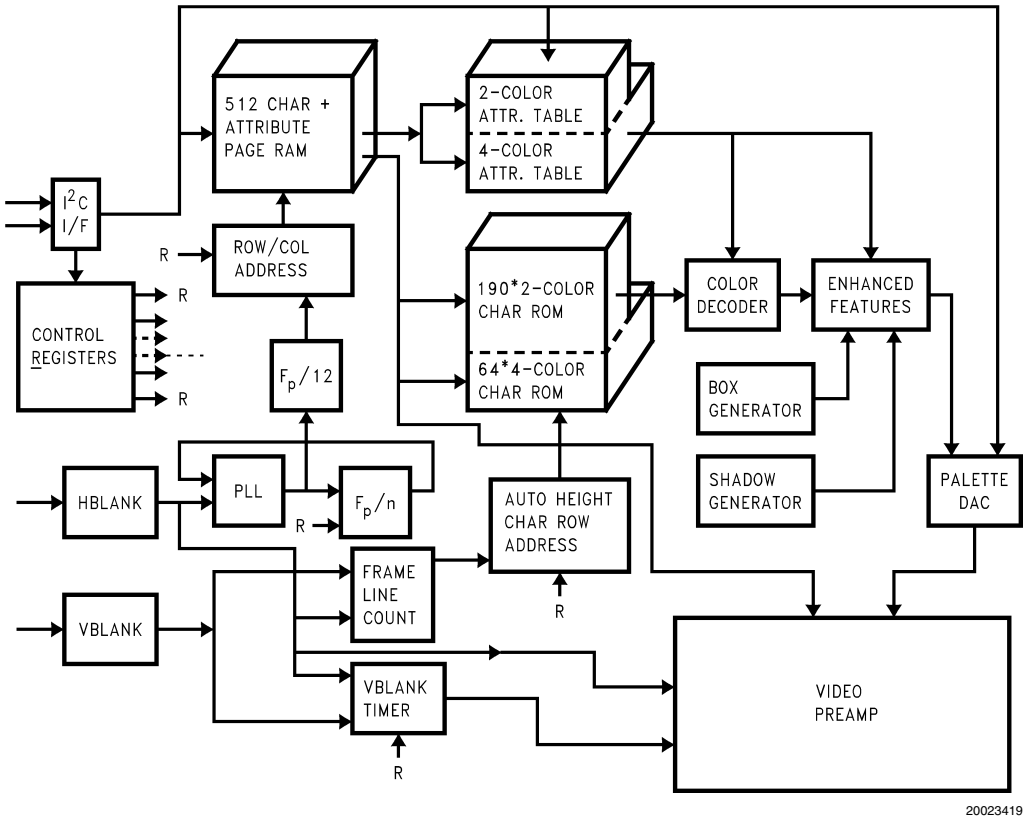


FIGURE 12. Block Diagram of the OSD Generator

Video information is created using any of the 256 predefined characters stored in the mask programmed ROM. Each character has a unique 8-bit code that is used as its address. Consecutive rows of characters make up the displayed window. These characters can be stored in the page RAM, written under I^2C compatible commands by the monitor microcontroller. Each row can contain any number of characters up to the limit of the displayable line length, although some restrictions concerning the enhanced features apply on character rows longer than 32 characters.

The number of characters across the width and height of the page can be varied under I^2C compatible control, but the total number of characters that can be stored and displayed on the screen is limited to 512 including any character row end characters. The horizontal and vertical start position can also be programmed through the I^2C compatible bus.

OSD VIDEO DAC

The OSD DAC is controlled by the 9-bit (3x3 bits) OSD video information coming from the pixel serializer look-up table. The look-up table in the OSD palette is programmed to select 4 color levels out of 8 linearly spaced levels per channel. The OSD DAC is shown in *Figure 13*, where the gain is programmable by the 2-bit OSD CONTRAST register, in 4 stages to give the required OSD signal. The OSD DACs use the reference voltage, V_{REF}, to bias the OSD outputs.

OSD Generator Operation (Continued)

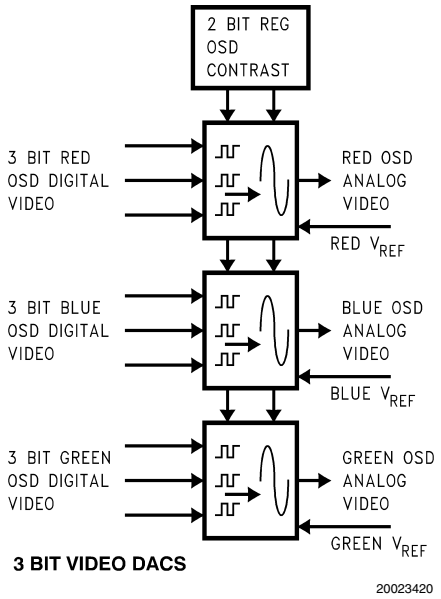


FIGURE 13. Block Diagram of OSD DACs

OSD VIDEO TIMING

The OSD SELECT signal switches the source of video information within the preamplifier from external video to the internally generated OSD video.

WINDOWS

Two separate windows can be opened, utilizing the data stored in the page RAM. Each window has its own horizontal and vertical start position, although the second window should be horizontally spaced at least two character spaces away from the first window, and should never overlap the first window when both windows are on. The OSD window must be placed within the active video.

CHARACTER CELL

Each character is defined as a 12 wide by 18 high matrix of picture elements, or 'pixels'. The character font is shown in *Figure 25*. There are two types of characters defined in the character ROM:

1. Two-color: There are 190 two-color characters. Each pixel of these characters is defined by a single bit value. If the bit value is 0, then the color is defined as 'Color 1' or the 'background' color. If the bit value is 1, then the color is defined as 'Color 2', or the 'foreground' color. An example of a character is shown in *Figure 14*.
2. Four-color: There are 64 four-color characters stored in the character ROM. Each pixel of the four-color character is defined by two bits of information, and thus can define four different colors, Color 1, Color 2, Color 3, and Color 4. Color 1 is defined as the 'background' color. All other colors are considered 'foreground' colors, although for most purposes, any of the four colors may be used in any way. Because each four-color character has two bits, the LM1237 internally has a matrix of two planes of ROM as shown in *Figure 15*.

OSD Generator Operation (Continued)

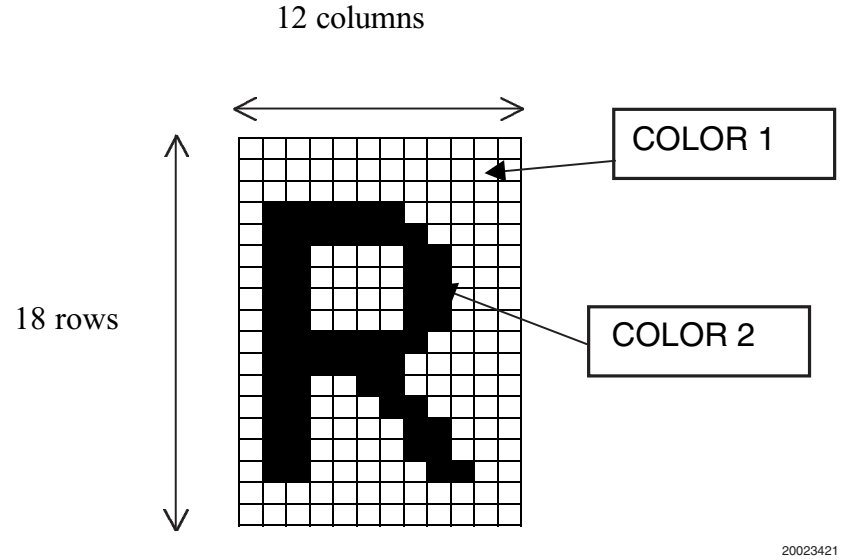


FIGURE 14. A Two-Color Character

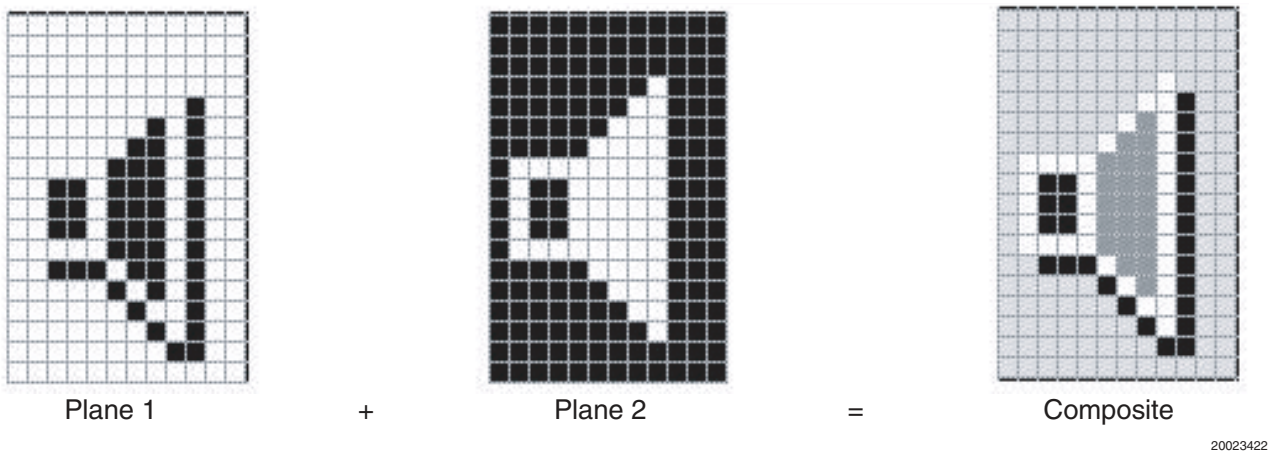


FIGURE 15. A Four-Color Character

ATTRIBUTE TABLES

Each character has an attribute value assigned to it in the page RAM. The attribute value is 4 bits wide, making each character entry in the page RAM 12 bits wide in total. The attribute value acts as an address which points to one of 16 entries in either the two-color attribute table RAM or the four-color attribute table RAM. The attribute word in the table contains the coding information which defines which color is represented by color1 and color2 in the two color attribute table and color1, color2, color3, color4 in the four-color attribute table. Each color is defined by a 9-bit value, with 3 bits assigned to each channel of RGB. A dynamic look-up table defines each of the 16 different color combination selections or 'palettes'. As the look-up table can be dynamically coded by the microcontroller over the I^2C compatible interface, each color can be assigned to any one of 2^9 (i.e. 512) choices. This allows a maximum of 64 different colors to be used within one page using the 4-color characters, with up to 4 different colors within any one character and 32 different colors using the 2-color characters, with 2 different colors within any one character.

TRANSPARENT DISABLE

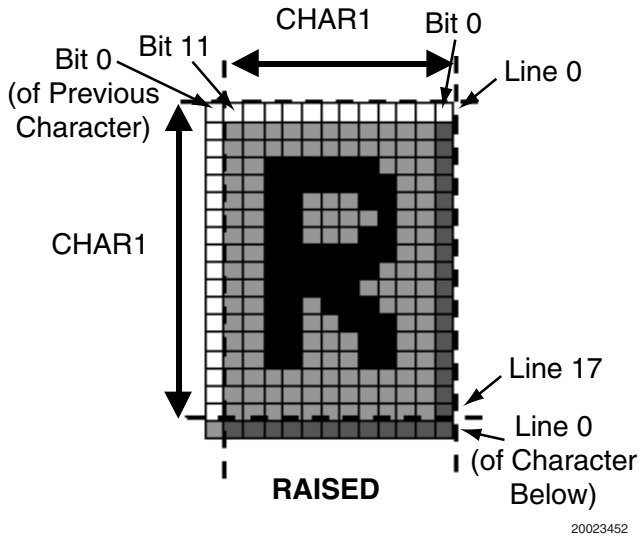
In addition to the 9 lines of video data, a tenth data line is generated by the transparent disable bit. When this line is activated, the black color code will be translated as 'transparent' or invisible. This allows the video information from the PC system to be visible on the screen when this is present. Note that this feature is enabled on any black color in of the first 8 attribute table entries.

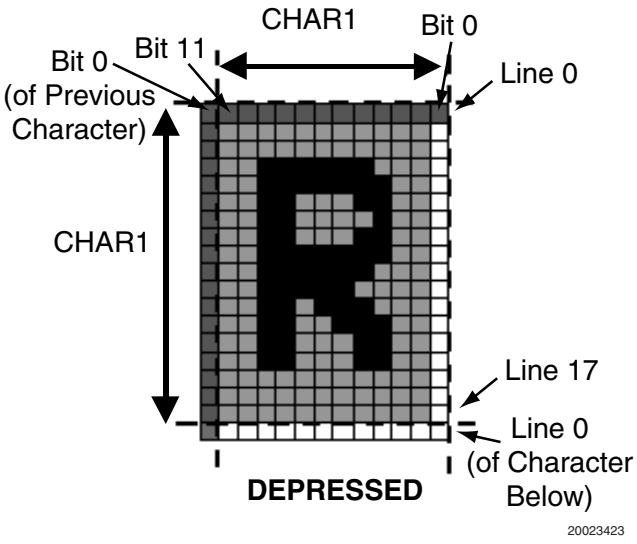
OSD Generator Operation (Continued)

ENHANCED FEATURES

In addition to the wide selection of colors for each character, additional character features can be selected on a character by character basis. There are 3 Enhanced Feature Registers, EF0, EF1 and EF2.

1. Button Boxes — The OSD generator examines the character string being displayed and if the 'button box' attributes have been set in the Enhanced feature byte, then a box creator selectively substitutes the character pixels in either or both the top and left most pixel line or column with a button box pixel. The shade of the button box pixel depends upon whether a 'depressed' or 'raised' box is required, and can be programmed through the I^2C compatible interface. The raised pixel color ('highlight') is defined by the value in the color palette register, EF1 (normally white). The depressed pixel ('lowlight') color by the value in the color palette register EF2 (normally gray). See *Figure 16*.
2. Heavy Button Boxes — When heavy button boxes are selected, the color palette value stored in register EF3 is used for the depressed ('lowlight') pixel color instead of the value in register EF2.
3. Shadowing — Shadowing can be added to two-color characters by choosing the appropriate attribute value for the character. When a character is shadowed, a shadow pixel is added to the lower right edges of the color 2 image, as shown in *Figure 17*. The color of the shadow is determined by the value in the color palette register EF3 (normally black).
4. Bordering — A border can be added to the two-color characters. When a character is bordered, a border pixel is added at every horizontal, vertical or diagonal transition between color 1 and color 2. See *Figure 18*. The color of the border is determined by the value in the color palette register EF3 (normally black).
5. Blinking — If blinking is enabled as an attribute, all colors within the character except the button box pixels which have been overwritten will alternately switch to color 1 and then back to the correct color at a rate determined by the microcontroller through the I^2C compatible interface.





Effect on the screen:

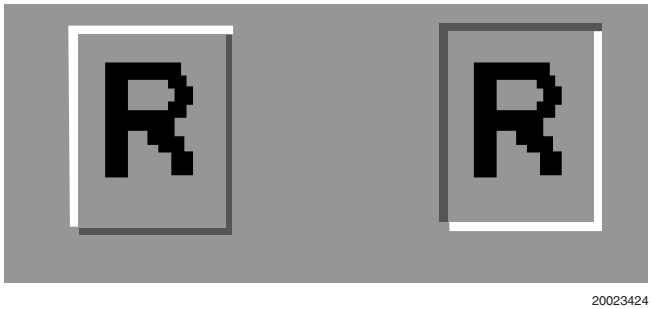


FIGURE 16. Button Boxes

OSD Generator Operation (Continued)

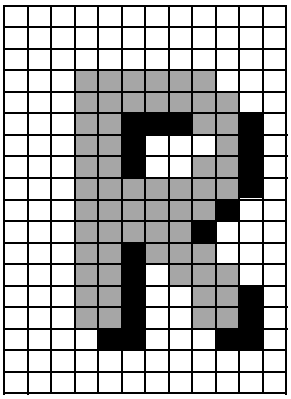


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FIGURE 17. Shadowing

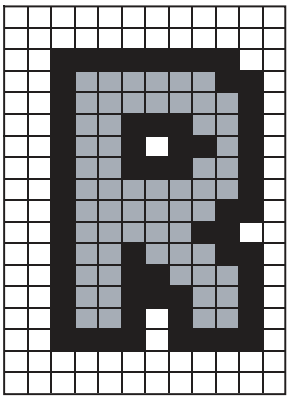

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FIGURE 18. Bordering

Microcontroller Interface

The microcontroller interfaces to the LM1237 preamp via the I^2C compatible interface. The protocol of the interface begins with a Start Pulse followed by a byte comprised of a seven bit Slave Device Address and a Read/Write bit. Since the first byte is composed of both the address and the read/write bit, the address of the LM1237 for writing is 0xBA (10111010b) and the address for reading is 0xBB (10111011b). The development software provided by National Semiconductor will automatically take care of the difference between the read and write addresses if the target address under the communications tab is set to 0xBA. *Figure 19* and *Figure 20* show a write and read sequence on the I^2C compatible interface.

WRITE SEQUENCE

The write sequence begins with a start condition which consists of the master pulling SDA low while SCL is held high. The slave device address is next sent. The address byte is made up of an address of seven bits (7-1) and the read/write bit (0). Bit 0 is low to indicate a write operation. Each byte that is sent is followed by an acknowledge. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The register to be written to is next sent in two bytes, the least significant byte being sent first. The master can then send the data, which consists of one or more bytes. Each data byte is followed by an acknowledge bit. If more than one data byte is sent the data will increment to the next address location. See *Figure 19*.

Microcontroller Interface (Continued)

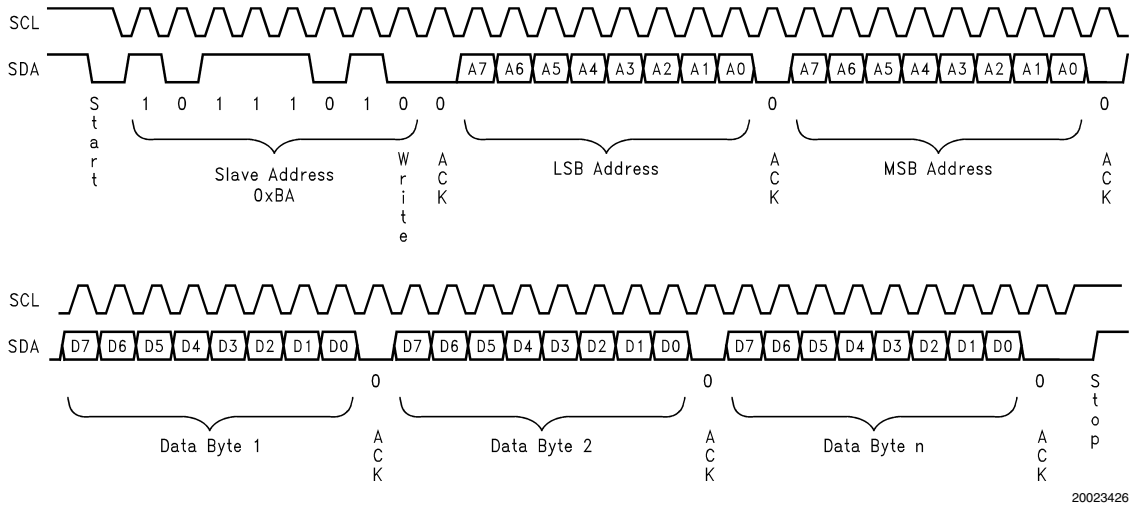


FIGURE 19. I²C Compatible Write Sequence

READ SEQUENCE

Read sequences are comprised of two I²C compatible transfer sequences: The first is a write sequence that only transfers the two byte address to be accessed. The second is a read sequence that starts at the address transferred in the previous address only write access and increments to the next address upon every data byte read. This is shown in *Figure 20*. The write sequence consists of the Start Pulse, the Slave Device Address, the Read/Write bit (a zero, indicating a write) and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access. Next the read data access will be performed beginning with the Start Pulse, the Slave Device Address, the Read/Write bit (a one, indicating a read) and the Acknowledge bit. The next 8 bits will be the read data driven out by the LM1237 preamp associated with the address indicated by the two address bytes. Subsequent read data bytes will correspond to the next increment address locations. Data should only be read from the LM1237 when both OSD windows are disabled.

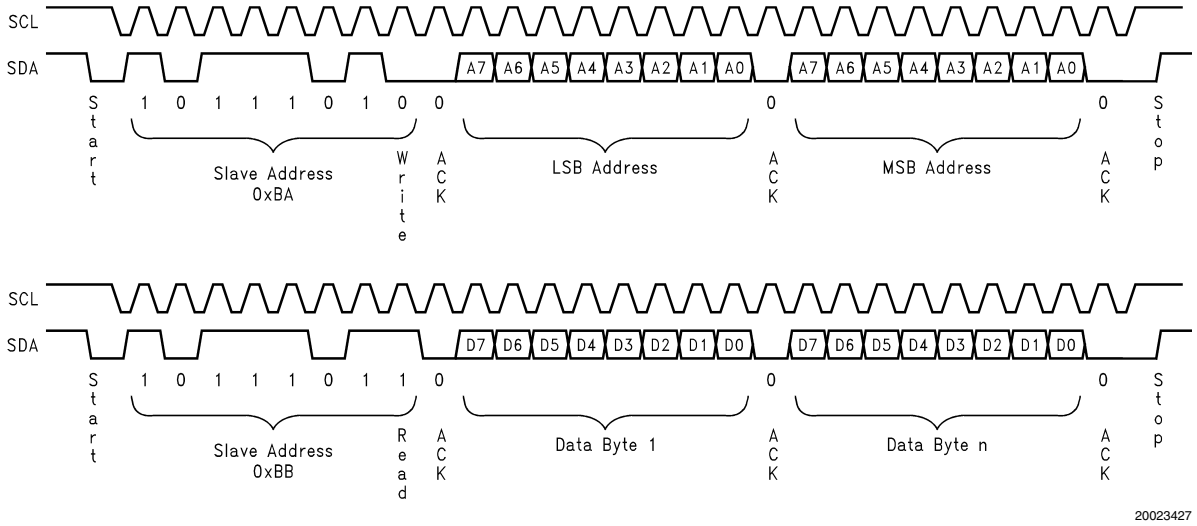


FIGURE 20. I²C Compatible Read Sequence

LM1237 Address Map

TABLE 4. Character ROM Address Map

Address Range	R/W	Description
0x0000–0x2FFF	R	ROM Character Fonts, 190 two-color Character Fonts that are read-only. The format of the address is as follows: A15–A14: Always zeros. A13–A6: Character value (0x00–0xBF are valid values) A5–A1: Row of the character (0x00–0x11 are valid values) A0: Low byte of line when a zero. High byte of line when a one. The low byte will contain the first eight pixels of the line with data Bit 0 corresponding to the left most bit in the Character Font line. The high byte will contain the last four pixels and data. Bits 7–4 are “don’t cares”. Data Bit 3 of the high byte corresponds to the right most pixel in the Character Font line.
0x3000–0x3FFF	R	ROM Character Fonts, 64 four-color Character Fonts that are read-only. The format of the address is as follows: A15–A14: Always zeros. A13–A6: Character value (0xC0–0xFF are valid values) A5–A1: Row of the character (0x00–0x11 are valid values) A0: Low byte of line when a zero. High byte of line when a one. The low byte will contain the first eight pixels of the line with data Bit 0 corresponding to the left most bit in the Character Font line. The high byte will contain the last four pixels and data Bits 7–4 are “don’t cares”. Data Bit 3 of the high byte corresponds to the right most pixel in the Character Font line. **NOTE:** The value of Bit 0 of the Character Font Access Control Register (Address 0x8402) is a zero, it indicates that the Bit 0 data value of the four-color pixels is being accessed via these addresses. When the value of Bit 0 of the Access Control Register is a one, it indicates that the Bit 1 data value of the four-color pixel is being accessed via these addresses.
0x4000–0x7FFF	—	Reserved.

TABLE 5. Display Page RAM Address Map

Address Range	R/W	Description
0x8000–0x81FF	R/W	Display Page RAM Characters. A total of 512 display characters, skipped line, end-of-row and end-of-window character codes may be supported via this range. To support skipped lines and character attributes a number of special case rules are used when writing to this range. (Refer to the Display Page RAM section of this document for more details.)

Preamp Interface Registers

TABLE 6. OSD Interface Registers

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
Fonts - 2 Color	0x0000–0x2FFE		PIXEL (7:0)							
	+1		X	X	X	X	PIXEL (11:8)			
Fonts - 4 Color	0x3000–0x3FFE		PIXEL (7:0)							
	+1		X	X	X	X	PIXEL (11:8)			
Display Page	0x8000–0x83FF		CHAR_CODE[7:4] or reserved				CHAR_CODE[3:0] or ATTR_CODE			
FRMCTRL1	0x8400	0x10	X	X	X	TD	CDPR	D2E	D1E	OSE
FRMCTRL2	0x8401	0x80	PIXELS_PER_LINE (2:0)			BLINK_PERIOD (4:0)				
CHARFONTACC	0x8402	0x00	X	X	X	X	X	X	ATTR	FONT4
VBLANKDUR	0x8403	0x10	X	VBLANK_DURATION (6:0)						

Preamp Interface Registers (Continued)

TABLE 6. OSD Interface Registers (Continued)

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
CHARHTCTRL	0x8404	0x51	CHAR_HEIGHT (7:0)							
BBHLCTRLB0	0x8405	0xFF	B[1:0]		G[2:0]			R[2:0]		
BBHLCTRLB1	0x8406	0x01	X	X	X	X	X	X	X	B[2]
BBLLCTRLB0	0x8407	0x00	B[1:0]		G[2:0]			R[2:0]		
BBLLCTRLB1	0x8408	0x00	X	X	X	X	X	X	X	B[2]
CHSDWCTRLB0	0x8409	0x00	B[1:0]		G[2:0]			R[2:0]		
CHSDWCTRLB1	0x840A	0x00	X	X	X	X	X	X	X	B[2]
ROMSIGCTRL	0x840D	0x00	X	X	X	X	X	X	X	CRS
ROMSIGDATAB0	0x840E	0x00	CRC (7:0)							
ROMSIGDATAB1	0x840F	0x00	CRC (15:8)							
HSTRT1	0x8410	0x13	HPOS (7:0)							
VSTRT1	0x8411	0x14	VPOS (7:0)							
COLWIDTH1B0	0x8414	0x00	COL (7:0)							
COLWIDTH1B1	0x8415	0x00	COL (15:8)							
COLWIDTH1B2	0x8416	0x00	COL (23:16)							
COLWIDTH1B3	0x8417	0x00	COL (31:24)							
HSTRT2	0x8418	0x56	HPOS (7:0)							
VSTRT2	0x8419	0x5B	VPOS (7:0)							
W2STRTADRL	0x841A	0x00	ADDR (7:0)							
W2STRTADRH	0x841B	0x01	X	X	X	X	X	X	X	ADDR(8)
COLWIDTH2B0	0x841C	0x00	COL (7:0)							
COLWIDTH2B1	0x841D	0x00	COL (15:8)							
COLWIDTH2B2	0x841E	0x00	COL (23:16)							
COLWIDTH2B3	0x841F	0x00	COL (31:24)							

Note: Set reserved bits to 0.

TABLE 7. LM1237 Preamplifier Interface Registers

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
BGAINCTRL	0x8430	0xE0	X	BGAIN[6:0]						
GGAINCTRL	0x8431	0xE0	X	GGAIN[6:0]						
RGAINCTRL	0x8432	0xE0	X	RGAIN[6:0]						
CONTRCTRL	0x8433	0xE0	X	CONTRAST[6:0]						
DAC1CTRL	0x8434	0x80	DAC1[7:0]							
DAC2CTRL	0x8435	0x80	DAC2[7:0]							
DAC3CTRL	0x8436	0x80	DAC3[7:0]							
DAC4CTRL	0x8437	0x80	DAC4[7:0]							
DACOSDDCOFF	0x8438	0x94	X	DCF[1:0]		OSD CONT[1:0]		DS OFFSET[1:0]		
GLOBALCTRL	0x8439	0x00	X	X	X	X	X	X	PS	BV
PLLFREQRNG	0x843E	0x16	X	X	CLMP	X	OOR	VBL	PFR[1:0]	
SRTSTCTRL	0x843F	0x00	X	A/D[0]	X	X	X	X	X	SRST[0]

Note: Set reserved bits to 0.

Two-Color Attribute Table

TABLE 8. LM1237 Two-Color Attribute Registers

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
ATT2C0n	0x8440 + 4n	C1B[1:0]		C1G[2:0]			C1R[2:0]		

Two-Color Attribute Table (Continued)

TABLE 8. LM1237 Two-Color Attribute Registers (Continued)

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
ATT2C1n	+1	C2B[0]	C2G[2:0]			C2R[2:0]			C1B[2]
ATT2C2n	+2	X	X	EF[3:0]				C2B[2:1]	
ATT2C3n	+3	X	X	X	X	X	X	X	X

Note: Set reserved bits to 0.

The attributes for two-color display characters may be written or read via the following address format:

A15–A6: Always a binary 1000010001.

A5–A2: Attribute code n (0x0–0xF are valid values).

A1–A0: Determines which of the 3 bytes is to be accessed.

Note: In the table, n indicates the attribute number $0 \le n \le 15$.

Note: When writing, bytes 0 through 2 must be written in order. Bytes 0 through 2 will take effect after byte 2 is written. Since byte 3 contains all reserved bits, this byte may be written, but will have no effect.

When reading, it is OK to read only one, two, or all three bytes.

If writing more than one 2-color attributes using the auto increment feature, all four bytes must be written.

Four-Color Attribute Table

TABLE 9. LM1237 Four-Color Attribute Registers

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
ATT4C0n	8500 + (n*8)	C1B[1:0]		C1G[2:0]			C1R[2:0]		
ATT4C1n	+1	C2B[0]	C2G[2:0]			C2R[2:0]			C1B[2]
ATT4C2n	+2	X	X	EF[3:0]				C2B[2:1]	
ATT4C3n	+3	X	X	X	X	X	X	X	X
ATT4C4n	+4	C3B[1:0]		C3G[2:0]			C3R[2:0]		
ATT4C5n	+5	C4B[0]	C4G[2:0]			C4R[2:0]			C3B[2]
ATT4C6n	+6	X	X	X	X	X	X	C4B[2:1]	
ATT4C7n	+7	X	X	X	X	X	X	X	X

Note: Set reserved bits to 0.

The attributes for four-color display characters may be written or read via the following address format:

A15–A7: Always a binary 100001010.

A6–A3: Attribute code n (0x0–0xF are valid values).

A2–A0: Determine which of the six bytes of the attribute is to be accessed.

Note: In the table, n indicates the attribute number $0 \le n \le 15$.

Note: When writing, bytes 0 through 2 must be written in order and bytes 4 to 6 must be written in order. Bytes 0 through 2 will take effect after byte 2 is written. Bytes 4 through 6 will take effect after byte 6 is written. Since bytes 5 and 7 contain all reserved bits, these bytes may be written, but no effect will result.

When reading, it is OK to read only one, two, or all three bytes.

If writing more than one 4-color attributes using the auto increment feature, all eight bytes must be written.

Display Page RAM

THE OSD WINDOW

The Display Page RAM contains all of the 8-bit display character codes and their associated 4-bit attribute codes, and the special 12-bit page control codes—the row-end, skip-line parameters and window-end characters.

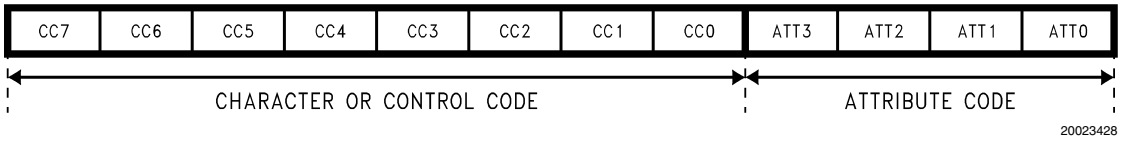
The LM1237 has a distinct advantage over many OSD generators that it allows variable size and format windows. The window size is not dictated by a fixed geometry area of RAM. Instead, 512 locations of 12-bit words are allocated in RAM for the definition of the windows, with special control codes to define the window size and shape.

Window width can be any length supported by the number of pixels per line that is selected divided by the number of pixels in a character line. It must be remembered that OSD characters displayed during the monitor blanking time will not be displayed on the screen, so the practical limit to the number of horizontal characters on a line is reduced by the number of characters within the horizontal blanking period.

CHARACTER CODE AND ATTRIBUTE CODE

Each of the 512 locations in the page RAM is comprised of a 12-bit code consisting of an 8-bit character or control code, and a 4-bit attribute code:

Display Page RAM (Continued)



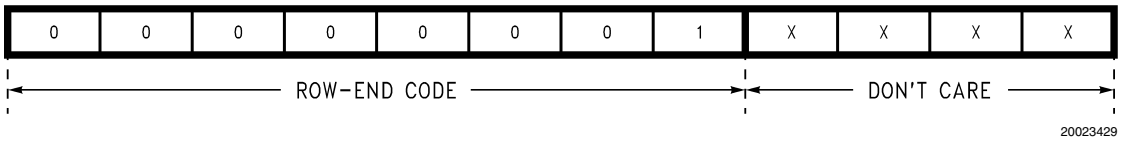
Bits 11–4 (Character Code): These 8 bits define which of the 254 characters is to be called from the character ROM. Valid character codes are 0x02–0xFF.

Bits 3–0 (Attribute Code): These 4 bits address the attribute table used to specify which of the 16 locations in RAM specify the colors and enhanced features to be used for this particular character. Two separate attribute tables are used, one for 2-color characters, the other for 4-color characters.

Each of the characters are stored in sequence in the page RAM. Special codes are used between lines to show where one line ends and the next begins, and also to allow blank (or 'skipped') single scan lines to be added between character rows.

ROW END CODE

To signify the end of a row of characters, a special Row-End (RE) code is used in place of a character code.



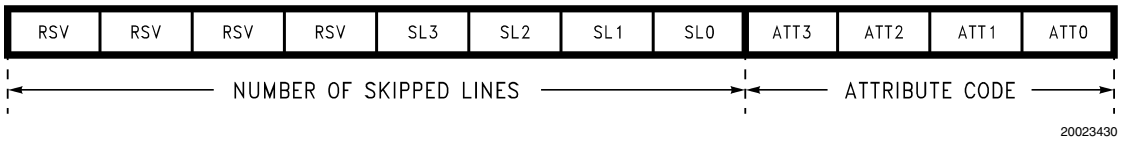
Bits 11–4 (Row-End Code): A special character code of 0x01

Bits 3–0 (Don't care)

The RE character tells the OSD generator that the character codes following must be placed on a new row in the displayed window.

SKIPPED LINE CODE

Each displayed row of characters may have up to 15 skipped (i.e., blank) lines beneath it in order to allow finer control of the vertical spacing of character rows. (Each skipped line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate size relative to the character cell—see section Constant Character Height Mechanism). To specify the number of skipped lines, the first character in each new row of characters to be displayed is interpreted differently than the other characters in the row. Instead of interpreting the data in the location as a character code, the 12 bits are defined as follows:



Bits 11–8 (Reserved): These should be set to zero.

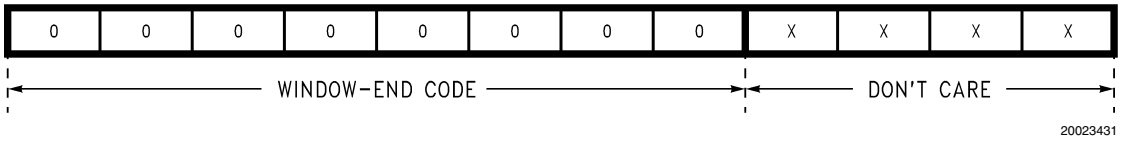
Bits 7–4 (Skipped Lines): These four bits determine how many blank pixel lines will be inserted between the present row of display characters and the next row of display characters. A range of 0–15 may be selected.

Bits 3–0 (Attribute Code): The pixels in the skipped lines will normally be Color 1 of the addressed 2-Color Attribute Table entry. Note that the pixels in the first line immediately below the character may be overwritten by the pixel override system that creates the button box. (Refer to the Box Formation Section for more information).

Each new line MUST start with an SL code, even if the number of skipped lines to follow is zero. An SL code MUST always follow an RE control code. An RE code may follow an SL code if several 'transparent' lines are required between sections of the window (see example 3 below). In this case, skipped lines of zero characters are displayed, causing a break in the window.

WINDOW END CODE

To signify the end of the window, a special Window-End (WE) code is used in place of a Row-End code.



Bits 11–4 (Row-End Code): A special character code of 0x00.

Bits 3–0 (Don't care)

Display Page RAM (Continued)

The WE control code tells the OSD generator that the character codes following belong to another displayed window at the next window location. A WE control code may follow normal characters or an SL parameter, but never an RE control code.

WRITING TO THE PAGE RAM

The Display Page RAM can contain up to 512 of the above listed characters and control codes. Each character, or control code will consume one of the possible 512 locations. For convenience, a single write instruction to bit 3 of the Frame Control Register (0x8400) can reset the page RAM value to all zero.

Display Window 1 will also start at the first location (corresponding to the I^2C address 0x8000). This location must always contain the Skip-Line (SL) code associated with the first row of Display Window 1. Subsequent locations should contain the characters to be displayed on row 1 of Display Window 1, until the RE character code or WE character code is written into the Display Page-RAM.

The skip-line parameters associated with the next row must always be written to the location immediately after the preceding row's row-end character. The only exception to this rule is when a window-end character (value 0x0000) is encountered. It is important to note that a row-end character should not precede a window-end character (otherwise the window-end character will be interpreted as the next row's skip-line code). Instead, the window-end character will both end the row and the window making it unnecessary to precede it with a row-end character.

The I^2C Format for writing a sequence of display characters is minimized by allowing sequential characters with the same attribute code to send in a string as follows:

Byte #1 — I^2C Slave Address

Byte #2 — LSB Register Address

Byte #3 — MSB Register Address

Byte #4 — Attribute Table Entry to use for the following characters

Byte #5 — First display character, SL parameter, RE or WE control code

Byte #6 — Second display character, SL parameter, RE or WE control code

Byte #7 — Third display character, SL parameter, RE or WE control code

Byte #n — Last display character in this color sequence, SL parameter, RE or WE control code to use the associated Attribute Table Entry.

The Attribute Table Entry (Byte #4, of the above) is automatically associated with each subsequent display character or SL code written. The following are examples of how the Display Page RAM associates to the actual On-Screen Display Window #1.

EXAMPLE 1:

A 3x3 character matrix of yellow characters on a black background is to be displayed on the screen of all the same color, using 2-color character codes:

The actual On-Screen Display of Window #1 is shown in *Figure 21*. Note the dotted white lines are not actually part of the OSD image to be displayed. They are shown here only to designate character boundaries.

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FIGURE 21. Example 1 OSD

Notes:

- Every row must begin with an attribute and an SL. Display Page RAM memory location 0x8000 will always be associated with the SL of row 0 of Display Window #1.
- Every row except the last row of a Display Window must end with an RE character. The character immediately after an RE character is always the SL value for the next row.
- The last row in a Display Window must be a WE character. The WE character must NOT be preceded by an RE character.
- The entire Display Window may be written in a single I^2C write sequence because the Attribute Table entry (i.e., the color palette) does not change for the entire Display Window.
- The Attribute Table Entry that is associated with RE and WE characters are "don't cares". So in general it is most efficient just to allow them to be the same value as the Attribute Table Entry associated with the previous display character.

Display Page RAM (Continued)

- The colors of the characters and background can be stored in a single location in the 2-color attribute table, in location ATT0.
- The data shown in *Table 10* is sent to the LM1237 in one I^2C transmission.

TABLE 10. Example 1 Data Transmission

Data Sent	Description	RAM Address
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x00	Address LSB	
0x80	Address MSB	
0x00	Use Attribute table 00 for the following characters	
0x00	Skip 0 lines Command	8000
0x02	Character “A”	8001
0x03	Character “B”	8002
0x04	Character “C”	8003
0x01	Row-End (RE) Command	8004
0x00	Skip 0 lines	8005
0x05	Character “D”	8006
0x06	Character “E”	8007
0x07	Character “F”	8008
0x01	Row-End (RE) Command	8009
0x00	Skip 0 lines Command	800A
0x08	Character “G”	800B
0x09	Character “H”	800C
0x0A	Character “I”	800D
0x00	Window-End (WE) Command	800E
	I^2C stop condition (See the Microcontroller Interface Section)	

EXAMPLE 2:

A 3x3 character matrix of characters on a black background is to be displayed on the screen, using 2-color character codes. 2 skipped lines are required below the first line of characters, 3 skipped lines are required below the second line of characters, and 4 skipped lines are required below the third line of characters. The first line of characters will use color attribute 0, the second line will use color attribute 1, the third line will use color attribute 0 for the first character, color attribute 1 for the second character, and color attribute 2 for the third character. This is shown in *Figure 22*.

Display Page RAM (Continued)

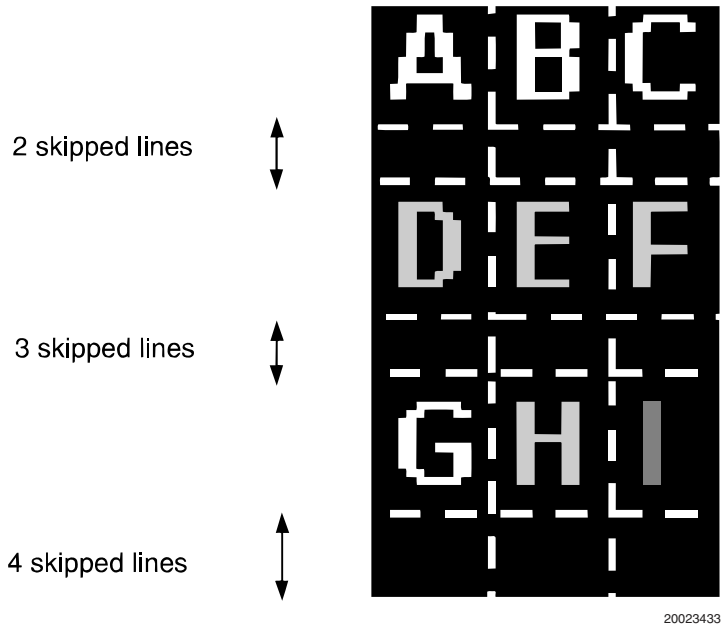


FIGURE 22. Example 2 OSD

Notes:

- Every row must begin with an attribute and an SL value. Display Page RAM memory location 0x8000 will always be associated with the SL of row 0 of Display Window #1.
- If an I^2C transmission finishes without an RE (in the middle of a row) the first byte sent in the next I^2C transmission is the attribute.
- Every row except the last row of a Display Window must end with an RE character. The character immediately after an RE character is always the SL value for the next row.
- The last row in a Display Window must be a WE character. The WE character must NOT follow an RE character.
- *Table 11* is the data sent to the LM1237 for the entire image, in five transmissions.

TABLE 11. Example 2 (Five Sequences)

Data Sent	Description	RAM Address
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x00	Address LSB	
0x80	Address MSB	
0x00	Use Attribute table 0x00 for the following characters	
0x02	Skip 2 lines Command	0x8000
0x02	Character “A”	0x8001
0x03	Character “B”	0x8002
0x04	Character “C”	0x8003
0x01	Row-End (RE) Command	0x8004
	I^2C stop condition (See the Microcontroller Interface Section)	
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x05	Address LSB	
0x80	Address MSB	
0x01	Use Attribute table 0x01 for the following characters	
0x03	Skip 3 lines Command	0x8005

Display Page RAM (Continued)

TABLE 11. Example 2 (Five Sequences) (Continued)

Data Sent	Description	RAM Address
0x05	Character “D”	0x8006
0x06	Character “E”	0x8007
0x07	Character “F”	0x8008
0x01	Row-End (RE) Command	0x8009
	I^2C stop condition (See the Microcontroller Interface Section)	
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x0A	Address LSB	
0x80	Address MSB	
0x00	Use Attribute table 0x00 for the following character	
0x04	Skip 4 lines Command	0x800A
0x08	Character “G”	0x800B
	I^2C stop condition (See the Microcontroller Interface Section)	
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x0C	Address LSB	
0x80	Address MSB	
0x01	Use Attribute table 0x01 for the following character	
0x09	Character “H”	0x800C
0x01	Row-End (RE) Command	
	I^2C stop condition (See the Microcontroller Interface Section)	
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x0D	Address LSB	
0x80	Address MSB	
0x02	Use Attribute table 0x02 for the following character	
0x0A	Character “I”	0x800D
0x00	Window-End (WE) Command	0x800E
	I^2C stop condition (See the Microcontroller Interface Section)	

EXAMPLE 3:

Two different length rows of characters a black background are to be displayed on the screen, using 2-color character codes. 3 transparent skipped lines are required between the character rows. This is shown in *Figure 23*.

Display Page RAM (Continued)

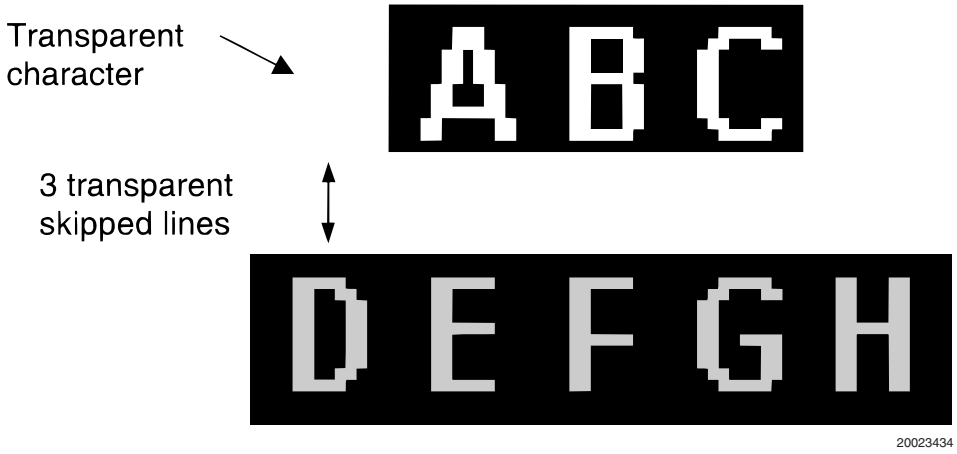


FIGURE 23. Example 3 OSD

Notes:

- In order to centralize the three characters above the five characters on the row below, a “transparent” blank character has been used as the first character on the row.
- In order to create the transparent skipped lines between the two character rows, a row of no characters has been used, resulting in a RE, SL, RE, SL control code sequence.
- In this example, the transparent character is defined by the 2-color attribute table entry ATT0. Bit 4 of Frame Control Register 1 must be set to indicate that the black color is to be translated as transparent (see section Control Register Definitions).
- The top row of characters are yellow on black; in this example, these are defined by the 2-color attribute table entry ATT9.
- The second row of characters are blue on black; in this example, these are defined by the 2-color attribute table entry ATT10.
- The black background of the characters are not transparent because ATT9 and ATT10 are used.
- The data shown in *Table 12* is sent to the LM1237 in four I^2C transmissions.

TABLE 12. Example 3 I^2C Sequences

Data Sent	Description	RAM Address
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x00	Address LSB	
0x80	Address MSB	
0x00	Use Attribute table 0x00 for the following characters	
0x00	Skip 2 lines Command	0x8000
0x80	Character “ ”	0x8001
	I^2C stop condition (See the Microcontroller Interface Section)	
	I^2C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x02	Address LSB	
0x80	Address MSB	
0x09	Use Attribute table 0x09 for the following characters	
0x02	Character “A”	0x8002
0x03	Character “B”	0x8003
0x04	Character “C”	0x8004
0x01	Row-End (RE) Command	0x8005
	I^2C stop condition (See the Microcontroller Interface Section)	
	I^2C start condition (See the Microcontroller Interface Section)	

Display Page RAM (Continued)

TABLE 12. Example 3 I²C Sequences (Continued)

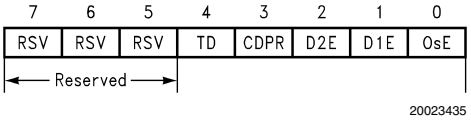
Data Sent	Description	RAM Address
0xBA	Chip address (See the Microcontroller Interface Section)	
0x06	Address LSB	
0x80	Address MSB	
0x00	Use Attribute table 0x00 for the following character	
0x03	Skip 3 lines Command	0x8006
0x01	Row-End (RE) Command	0x8007
	I²C stop condition (See the Microcontroller Interface Section)	
	I²C start condition (See the Microcontroller Interface Section)	
0xBA	Chip address (See the Microcontroller Interface Section)	
0x08	Address LSB	
0x80	Address MSB	
0x0A	Use Attribute table 0x0A for the following characters	
0x00	Skip 0 lines Command	0x8008
0x05	Character “D”	0x8009
0x06	Character “E”	0x800A
0x07	Character “F”	0x800B
0x08	Character “G”	0x800C
0x09	Character “H”	0x800D
0x00	Window-End (WE) Command	0x800E
	I²C stop condition (See the Microcontroller Interface Section)	

Control Register Definitions

OSD INTERFACE REGISTERS

Frame Control Register 1

Register Name (address): FRMCTRL1 (0x8400)

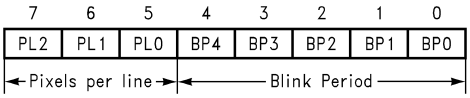


Bit 0	On-Screen Display Enable. The On-Screen Display will be disabled when this bit is a zero. When this bit is a one the On-Screen Display will be enabled and Display Window 1 will be enabled if Bit 1 of this register is a one; likewise Display Window 2 will be enabled if Bit 2 of this register is a one.
Bit 1	Display Window 1 Enable. When Bit 0 of this register and this bit are both ones, Display Window 1 is enabled. If either bit is a zero, then Display Window 1 will be disabled.
Bit 2	Display Window 2 Enable. When Bit 0 of this register and this bit are both ones, Display Window 2 is enabled. If either bit is a zero, then Display Window 2 will be disabled.
Bit 3	Clear Display Page RAM. Writing a one to this bit will result in setting all of the Display Page RAM values to zero. This bit is automatically cleared after the operation is complete.
Bit 4	Transparent Disable. When this bit is a zero, a palette color of black (i.e., color palette look-up table value of 0x00) in the first 8 palette look-up table address locations (i.e., ATT0–ATT7) will be interpreted as transparent. When this bit is a one, the color will be interpreted as black.
Bits 7–5	Reserved (Should be set to zero)

Control Register Definitions (Continued)

Frame Control Register 2

Register Name (address): FRMCTRL2 (0x8401)



20023436

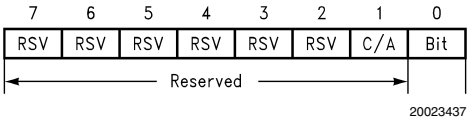
Bits 4–0	Blinking Period. These five bits set the blinking period of the blinking feature, which is determined by mulitiplying the value of these bits by 8, and then multiplying the result by the vertical field rate.
Bits 7–5	Pixels per Line. These three bits determine the number of pixels per line of OSD characters per the following table which also lists the maximum horizontal scan rate recommended for each setting.

Bits 7–5	Description	Max Horizontal Frequency (kHz)
0x0	512 pixels per line	125
0x1	576 pixels per line	119
0x2	640 pixels per line	112
0x3	704 pixels per line	106
0x4	768 pixels per line	100
0x5	832 pixels per line	93
0x6	896 pixels per line	87
0x7	960 pixels per line	81

Control Register Definitions (Continued)

Character Font Access Register

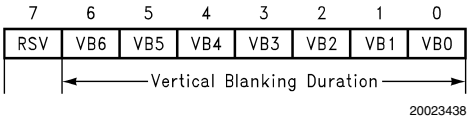
Register Name (address): CHARFONTACC (0x8402)



Bit 0	This is the Color Bit Plane Selector. This bit must be set to 0 to read or write a two-color attribute from the range 0x0000 to 0x2FFF. When reading or writing four-color attributes from the range 0x3000 to 0x3FFF, this bit is set to 0 for the least significant plane and to 1 for the most significant plane.
Bit 1	This is the Character/Attribute Selector. This applies to reads from the Display Page RAM (address range 0x8000–0x81FF). When a 0, the character code is returned and when a 1, the attribute code is returned.
Bits 7–2	Reserved. These should be set to zero.

Vertical Blank Duration Register

Register Name (address): VBLANKDUR (0x8403)

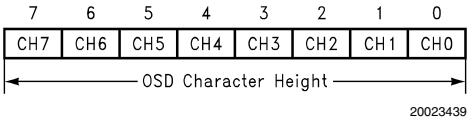


Bits 6–0	This register determines the duration of the vertical blanking signal in scan lines. When vertical blanking is enabled, it is recommended that this register be set to a number greater than 0x0A.
Bit 7	Reserved. This bit should be set to zero.

Control Register Definitions (Continued)

Character Height Register

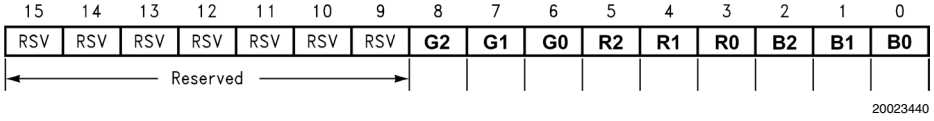
Register Name (address): CHARHTCTRL (0x8404)



Bits 7–0	This register determines the OSD character height as described in the section Constant Character Height Mechanism. The values of this register is equal to the approximate number of OSD height compensated lines required on the screen, divided by 4. This value is not exact due to the approximation used in scaling the character. Example: If approximately 324 OSD lines are required on the screen (regardless of the number of scan lines) then the Character Height Control Register is programmed with 81 (0x51).

Enhanced Feature Register 1 **Button Box Highlight Color**

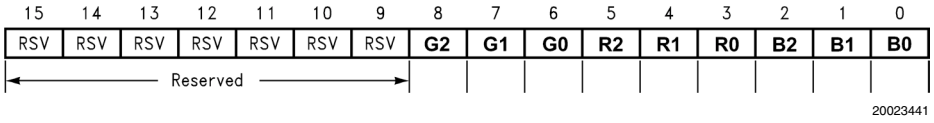
Register Name (addresses): BBHLCTRLB1 (0x8406) and BBHLCTRLB0 (0x8405)



Bits 8–0	These determine the button box highlight color.
Bits 15–9	Reserved. These bits should be set to zero.

Enhanced Feature Register 2 **Button Box Lowlight Color**

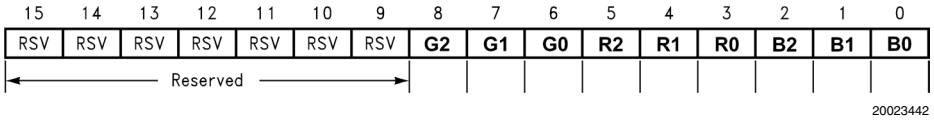
Register Names (addresses): BBLLCTRLB1 (0x8408) and BBLLCTRLB0 (0x8407)



Bits 8–0	These determine the button box lowlight color.
Bits 15–9	Reserved. These bits should be set to zero.

Enhanced Feature Register 3 **Heavy Button Box Lowlight/Shading/Shadow**

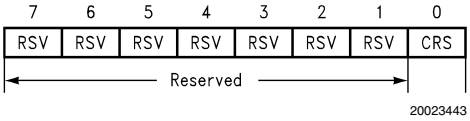
Register Names (addresses): CHSDWCTRLB1 (0x840A) and CHSDWCTRLB0 (0x8409)



Bits 8–0	These registers determine the heavy button box lowlight, shading or shadow color.
Bits 15–9	Reserved. These bits should be set to zero.

ROM Signature Control Register

Register Name (address): ROMSIGCTRL (0x840D)



Bit 0	This controls the calculation of the ROM signature. Setting this bit causes the ROM to be read sequentially and a 16-bit checksum calculated over the 256 characters. The sum, modulo 65535, is stored in the ROM Signature Data Register, and this bit is then automatically cleared.
Bits 7–1	Reserved. These should be set to zero.

ROM Signature Data Register

Control Register Definitions (Continued)

Register Names (addresses): ROMSIGDATAB1 (0x840F) and ROMSIGDATAB0 (0x840E)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0

Bits 15–0	This is the checksum of the 256 ROM characters truncated to 16 bits (modulo 65535). All devices with the same masked ROM will have the same checksum.

Display Window 1 Horizontal Start Location Register

Register Name (address): HSTRT1 (0x8410)

7	6	5	4	3	2	1	0
1H7	1H6	1H5	1H4	1H3	1H2	1H1	1H0

Bits 7–0	There are two possible OSD windows which can be displayed simultaneously or individually. This register determines the horizontal start position of Window 1 in OSD pixels (not video signal pixels). The actual position, to the right of the horizontal flyback pulse, is determined by multiplying this register value by 4 and adding 30. Due to pipeline delays, the first usable start location is approximately 42 OSD pixels following the horizontal flyback time. For this reason, we recommend this register be programmed with a number larger than 2, otherwise improper operation may result.

Display Window 1 Vertical Start Location Register

Register Name (address): VSTRT1 (0x8411)

7	6	5	4	3	2	1	0
1V7	1V6	1V5	1V4	1V3	1V2	1V1	1V0

Bits 7–0	This register determines the Vertical start position of the Window 1 in constant-height character lines (not video scan lines). The actual position is determined by multiplying this register value by 2. (Note: each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the OSD character cell size. See the Constant Character Height Mechanism section.) This register should be set so the entire OSD window is within the active video.

Control Register Definitions (Continued)

Display Window 1 Column Width Register

Register Names (addresses): COLWIDTH1B3 (0x8417), COLWIDTH1B2 (0x8416), COLWIDTH1B1 (0x8415), COLWIDTH1B0 (0x8414)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COL 31	COL 30	COL 29	COL 28	COL 27	COL 26	COL 25	COL 24	COL 23	COL 22	COL 21	COL 20	COL 19	COL 18	COL 17	COL 16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COL15	COL14	COL13	COL12	COL11	COL10	COL9	COL8	COL7	COL6	COL5	COL4	COL3	COL2	COL1	COL0

Bits 31–0	These are the Display Window 1 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31–0 of Display Window 1, respectively. A value of zero indicates the column will have normal width (12 pixels). A value of one indicates the column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations. The user should note that if more than 32 display characters are programmed to reside on a row, then all display characters after the first thirty-two will have normal width (12 pixels).

Display Window 2 Horizontal Start Location Register

Register Name (address): HSTRT2 (0x8418)

7	6	5	4	3	2	1	0
2H7	2H6	2H5	2H4	2H3	2H2	2H1	2H0

Bits 7–0	This register determines the horizontal start position of Window 2 in OSD pixels (not video signal pixels). The actual position, to the right of the horizontal flyback pulse, is determined by multiplying this register value by 4 and adding 30. Due to pipeline delays, the first usable start location is approximately 42 OSD pixels following the horizontal flyback time. For this reason, we recommend this register be programmed with a number larger than 2, otherwise improper operation may result.

Display Window 2 Vertical Start Location Register

Register Name (address): VSTRT2 (0x8419)

7	6	5	4	3	2	1	0
2V7	2V6	2V5	2V4	2V3	2V2	2V1	2V0

Bits 7–0	This register determines the Vertical start position of Window 2 in constant-height character lines (not video scan lines). The actual position is determined by multiplying this register value by 2. (Note: each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the OSD character cell size. See the Constant Character Height Mechanism section.) This register should be set so the entire OSD window is within the active video.

Display Window 2 Start Address

Register Names (addresses): W2STRTADRH (0x841B) W2STRTADRL (0x841A)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	RSV	RSV	2AD8	2AD7	2AD6	2AD5	2AD4	2AD3	2AD2	2AD1	2AD0

Bits 8–0	This register determines the starting address of Display Window 2 in the Display Page RAM. This first address location will always contain the SL code for the first row of Display Window 2.
Bits 15–9	These bits are reserved and should be set to zero.

Display Window 2 Column Width Register

Register Names (addresses): COLWIDTH2B3 (0x841F), COLWIDTH1B2 (0x841E), COLWIDTH2B1 (0x841D), COLWIDTH1B0 (0x841C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COL 31	COL 30	COL 29	COL 28	COL 27	COL 26	COL 25	COL 24	COL 23	COL 22	COL 21	COL 20	COL 19	COL 18	COL 17	COL 16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COL15	COL14	COL13	COL12	COL11	COL10	COL9	COL8	COL7	COL6	COL5	COL4	COL3	COL2	COL1	COL0

Control Register Definitions (Continued)

Bits 31–0	These are the Display Window 2 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31–0 of Display Window 2, respectively. A value of zero indicates the column will have normal width (12 OSD pixels). A value of one indicates the column will be twice as wide as normal (24 OSD pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations. The user should note that if more than 32 display characters are programmed to reside on a row, then all display characters after the first thirty-two will have normal width (12 pixels).

Pre-Amplifier Interface Registers

Blue Channel Gain Register

Register Name (address): BGAINCTRL (0x8430)

7	6	5	4	3	2	1	0
RSV	BG6	BG5	BG4	BG3	BG2	BG1	BG0

Bits 6–0	This register determines the gain of the blue video channel.
Bit 7	Reserved and should be set to zero.

Green Channel Gain Register

Register Name (address): GGAINCTRL (0x8431)

7	6	5	4	3	2	1	0
RSV	GG6	GG5	GG4	GG3	GG2	GG1	GG0

Bits 6–0	This register determines the gain of the green video channel.
Bit 7	Reserved and should be set to zero.

Red Channel Gain Register

Register Name (address): RGAINCTRL (0x8432)

7	6	5	4	3	2	1	0
RSV	RG6	RG5	RG4	RG3	RG2	RG1	RG0

Bits 6–0	This register determines the gain of the red video channel.
Bit 7	Reserved and should be set to zero.

Contrast Control Register

Register Name (address): CONTRCTRL (0x8433)

7	6	5	4	3	2	1	0
RSV	CG6	CG5	CG4	CG3	CG2	CG1	CG0

Bits 6–0	This register determines the contrast gain and affects all three channels, blue, red and green.
Bit 7	Reserved and should be set to zero.

DAC 1 Register

Register Name (address): DAC1CTRL (0x8434)

7	6	5	4	3	2	1	0
BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Bits 7–0	This register determines the output of DAC 1. The full-scale output is determined by bit 5 of the DAC Config, OSD Contrast & DC Offset Register.

DAC 2 Register

Register Name (address): DAC2CTRL (0x8435)

7	6	5	4	3	2	1	0
GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

Pre-Amplifier Interface Registers (Continued)

Bits 7–0	This register determines the output of DAC 2. The full-scale output is determined by bit 5 of the DAC Config, OSD Contrast & DC Offset Register.

DAC 3 Register

Register Name (address): DAC3CTRL (0x8436)

7	6	5	4	3	2	1	0
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0

Bits 7–0	This register determines the output of DAC 3. The full-scale output is determined by bit 5 of the DAC Config, OSD Contrast & DC Offset Register.

DAC 4 Register

Register Name (address): DAC4CTRL (0x8437)

7	6	5	4	3	2	1	0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

Bits 7–0	This register determines the output of DAC 4. The output of this DAC can be scaled and mixed with the outputs of DACs 1–3 as determined by bit 6 of the DAC Config, OSD Contrast & DC Offset Register.

DAC Config, OSD Contrast & DC Offset Register

Register Name (address): DACOSDDCOFF (0x8438)

7	6	5	4	3	2	1	0
RSV	DCF1	DCF0	OSD1	OSD0	DC2	DC1	DC0

Bits 2–0	These determine the DC offset of the three video outputs, blue, red and green.
Bits 4–3	These determine the contrast of the internally generated OSD.
Bit 5	When this bit is a 0, the full-scale outputs of DACs 1–3 are 4.5V. When it is a 1 the full-scale level is 2.5V.
Bit 6	When this bit is a 0, the DAC 4 output is independent. When it is a 1, the DAC 4 output is scaled by 50% and added to the outputs of DACs 1–3.
Bit 7	Reserved and should be set to zero.

Global Video Control Register

Register Name (address): GLOBALCTRL (0x8439)

7	6	5	4	3	2	1	0
RSV	RSV	RSV	RSV	RSV	RSV	PS	BV

Bit 0	When this bit is a 1, the video outputs are blanked (set to black level). When it is a 0, video is not blanked.
Bit 1	When this bit is a 1, the analog sections of the preamplifier are shut down for low power consumption. When it is a 0, the analog sections are enabled.

PLL Range Register

Register Name (address): PLLFREQRNG (0x843E)

7	6	5	4	3	2	1	0
RSV	RSV	CLMP	RSV	OOR	VBL	PFR1	PFR0

Bits 1–0	These determine the optimum frequency range of the Phase Locked Loop. Please see *Table 3* for recommended register values for various horizontal scan rates.
Bit 2	This is the Vertical Blanking register. When this bit is a 1, vertical blanking is gated to the video outputs. When set to a 0, the video outputs do not have vertical blanking.

Pre-Amplifier Interface Registers (Continued)

Bit 3	This is the OSD override bit. This should be set to 0 for normal operation. When set to a 1, the video outputs are disconnected and OSD only is displayed. This is useful for the OSD display of special conditions such as “No Signal” and “Input Signal Out of Range”, to avoid seeing unsynchronized video.
Bit 4	Reserved and should be set to zero.
Bit 5	This is the Clamp Polarity bit. When set to a 0, the LM1237 expects a positive going clamp pulse. When set to a 1, the expected pulse is negative going.
Bits 7–6	Reserved and should be set to zero.

Software Reset and Test Control Register

Register Name (address): SRTSTCTRL (0x843F)

7	6	5	4	3	2	1	0
RSV	AID	RSV	RSV	RSV	RSV	RSV	SRST

Bit 0	When this bit is a 1, all registers except this one are loaded with their default values. All operations are aborted, except data transfers in progress on the I^2C compatible bus. This bit clears itself when the reset is complete.
Bits 5–1	Reserved and should be set to zero.
Bit 6	This bit disables the register Auto-Increment feature of the I^2C compatible protocol. When set to a 1 Auto-Increment is disabled and when a 0, AI is enabled.
Bit 7	Reserved and should be set to zero.

Attribute Table and Enhanced Features

Each display character and SL in the Display Page RAM will have a 4-bit Attribute Table entry associated with it. The user should note that two-color display characters and four-color display characters use two different Attribute Tables, effectively providing 16 attributes for two-color display characters and 16 attributes for four-color display characters.

For two-color characters the attribute contains the code for the 9-bit foreground color (Color 2), the code for the 9-bit background color (Color 1), and the character’s enhanced features (Button Box, Blinking, Heavy Box, Shadowing, Bordering, etc.).

For four-color characters the attribute contains the code for the 9-bit Color 1, the code for the 9-bit Color 2, the code for the 9-bit Color 3, the code for the 9-bit Color 4 and the character’s enhanced features (Button Box, Blinking, Heavy Box, Shadowing, Bordering, etc.).

Two Color Attribute Format

Register Names (addresses):

ATT2C3n (0x8443+n*4), ATT2C2n (0x8442+n*4), ATT2C1n (0x8441+n*4), ATT2C0n (0x8440+n*4), where n is the attribute value as described in Table 100.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EFB3	EFB2	EFB1	EFB0	C2B2	C2B1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2B0	C2G2	C2G1	C2G0	C2R2	C2R1	C2R0	C1B2	C1B1	C1B0	C1G2	C1G1	C1G0	C1R2	C1R1	C1R0

Bits 8–0	These nine bits determine the background color (color1) which is displayed when the corresponding OSD pixel is a 0.
Bits 17–9	These nine bits determine the foreground color (color2) which is displayed when the corresponding OSD pixel is a 1.
Bits 21 –18	These are the enhanced feature (EF) bits which determine which feature is applied to the displayed character. The features and their corresponding codes are shown in *Table 13*.
Bits 31–22	Reserved and should be set to zero.

TABLE 13. Enhanced Feature Descriptions

Bits 21–18	Feature Description
0000b	Normal Display (color2/color1)
0001b	Blinking
0010b	Shadowing

Attribute Table and Enhanced Features (Continued)

TABLE 13. Enhanced Feature Descriptions (Continued)

Bits 21–18	Feature Description
0011b	Bordering
0100b	RESERVED
0101b	RESERVED
0110b	RESERVED
0111b	RESERVED
1000b	Raised Box
1001b	Blinking and Raised Box
1010b	Depressed Box
1011b	Blinking and Depressed Box
1100b	Heavy Raised Box
1101b	Blinking and Heavy Raised Box
1110b	Heavy Depressed Box
1111b	Blinking and Heavy Depressed Box

Four Color Attribute Format

Register Names (addresses):

ATT4C7n (0x8507+n*4), ATT4C6n (0x8507+n*4), ATT4C5n (0x8507+n*4), ATT4C4n (0x8507+n*4), ATT4C3n (0x8507+n*4), ATT4C2n (0x8507+n*4), ATT4C1n (0x8507+n*4), ATT4C0n (0x8507+n*4), where n is the attribute value (Table 100).

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	C4B2	C4B1
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
C4B0	C4G2	C4G1	C4G0	C4R2	C4R1	C4R0	C3B2	C3B1	C3B0	C3G2	C3G1	C3G0	C3R2	C3R1	C3R0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EFB3	EFB2	EFB1	EFB0	C2B2	C2B1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2B0	C2G2	C2G1	C2G0	C2R2	C2R1	C2R0	C1B2	C1B1	C1B0	C1G2	C1G1	C1G0	C1R2	C1R1	C1R0

Bits 8–0	These nine bits determine the color1 which is displayed when the corresponding OSD pixel code is 00b.
Bits 17–9	These nine bits determine the color2 which is displayed when the corresponding OSD pixel code is a 01b.
Bits 21–18	These are the enhanced feature (EF) bits which determine which feature is applied to the displayed character. The features and their corresponding codes are shown in *Table 14*.
Bits 31–22	Reserved and should be set to zero.
Bits 40–32	These nine bits determine the color3 which is displayed when the corresponding OSD pixel code is a 10b.
Bits 49–41	These nine bits determine the color4 which is displayed when the corresponding OSD pixel code is an 11b.
Bits 63–50	Reserved and should be set to zero.

TABLE 14. Attribute Tables and Corresponding Addresses

Attribute Value (n)	Two-Color Attribute Table Address	Four-Color Attribute Table Address
0000b	0x8440–0x8443	0x8500–0x8507
0001b	0x8444–0x8447	0x8508–0x850F
0010b	0x8448–0x844B	0x8510–0x8517
0011b	0x844C–0x844F	0x8518–0x851F
0100b	0x8450–0x8453	0x8520–0x8527
0101b	0x8454–0x8457	0x8528–0x852F
0110b	0x8458–0x845B	0x8530–0x8537
0111b	0x845C–0x845F	0x8538–0x853F
1000b	0x8460–0x8463	0x8540–0x8547
1001b	0x8464–0x8467	0x8548–0x854F

Attribute Table and Enhanced Features (Continued)

TABLE 14. Attribute Tables and Corresponding Addresses (Continued)

Attribute Value (n)	Two-Color Attribute Table Address	Four-Color Attribute Table Address
1010b	0x8468–0x846B	0x8550–0x8557
1011b	0x846C–0x846F	0x8558–0x855F
1100b	0x8470–0x8473	0x8560–0x8567
1101b	0x8474–0x8477	0x8568–0x856F
1110b	0x8478–0x847B	0x8570–0x8577
1111b	0x847C–0x847F	0x8578–0x857F

BUTTON BOX FORMATION

The value of the most significant Enhanced Feature Bit (EFB3) determines when to draw the left, right, bottom and top sides of a Box. EFB1 denotes whether a box is raised or depressed, and EFB2 denotes whether the box is normal or 'heavy'. For normal boxes, the lowlight color is determined by the color code stored in the register EF2. For the heavy box feature, the lowlight is determined by the color code stored in register EF3.

Boxes are created by a 'pixel override' system that overwrites character cell pixel information with either the highlight color (EF1) or low light shadow (EF2 or EF3) of the box. Only the top pixel line of the character and the right edge of the character can be overwritten by the pixel override system.

To form a complete box, the left hand edge of a box is created by overwriting the pixels in the right most column of the preceding character to one being enclosed by the box. The bottom edge of a box is created by either—

- overwriting the pixels in the top line of the character below the character being enclosed by the box, or
- overwriting the pixels in the top line of the skipped lines below, in the case where skip lines are present below a boxed character.

Characters should be designed so that button boxes will not interfere with the character.

Some minor limitations result from the above box formation methodology:

- No box may use the left most display character in the Display Window, or it will have no left side of the Box. To create a box around the left most displayed character, a transparent 'blank' character must be used in the first character position. This character will not be visible on the screen, but allows the formation of the box.
- At least one skip line must be used beneath characters on the bottom row, if a box is required around any characters on this row in order to accommodate the bottom edge of the box.
- Skipped lines cannot be used within a box covering several rows.
- Irregular shaped boxes, (i.e., other than rectangular), may have some missing edges.

Operation of the Shadow Feature

The shadow feature is created as follows: As each 12-bit line in the character is called from ROM, the line immediately preceding it is also called and used to create a 'pixel override' mask. Bits 11 through 1 of the preceding line are compared to bits 10 through 0 of the current character line. Each bit X in the current line is compared to bit X+1 in the preceding line (i.e., the pixel above and to the left of the current pixel). Note that bit 11 of the current line cannot be shadowed. A pixel override output mask is then created. When a pixel override output is 1 for a given pixel position, the color of that pixel must be substituted with the color code stored in the register EF3. Please see *Figure 24* for an example.

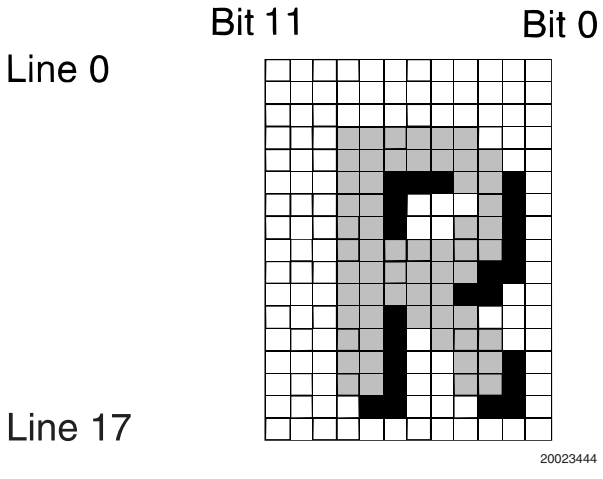


FIGURE 24. Operation of the Shadow Feature

Attribute Table and Enhanced Features (Continued)

Operation of the Bordering Feature

Borders are created in a similar manner to the shadows, using the pixel override system to overwrite pixel data with a pixel color set by EF3. However, instead of comparing just the previous line to the current line, all pixels surrounding a given pixel are examined.

The pixel override is created as follows: As each 12-bit line in the character is called from ROM, the character line immediately above and the line immediately below are also called. A 'Pixel Override' output mask is then created by looking at all pixels surrounding the pixel:

When a black override output is 1 for a given pixel position, X, the color of that pixel must be substituted with the color code stored in the register EF3.

Because the shadowing relies upon information about the pixels surrounding any given pixel, the bordering system may not operate correctly for pixels in the perimeter of the character (line 0, line 17, column 0 and column 11).

Constant Character Height Mechanism

The CRT monitor scan circuits ensure that the height of the displayed image remains constant so the physical height of a single displayed pixel row will decrease as the total number of image scan lines increases. As the OSD character matrix has a fixed number of lines, C, (where C = 18), then the character height will reduce as the number of scan lines increase, assuming a constant image height. To prevent this, the OSD generator repeats some of the lines in the OSD character in order to maintain a constant height percentage of the vertical image size.

In the LM1237, an approximation method is used to determine which lines are repeated, and how many times each line is repeated. The constant character height mechanism will not decrease the OSD character matrix to less than 18 lines. Each character will be at least 18 lines high.

Display Window 1 to Display Window 2 Spacing

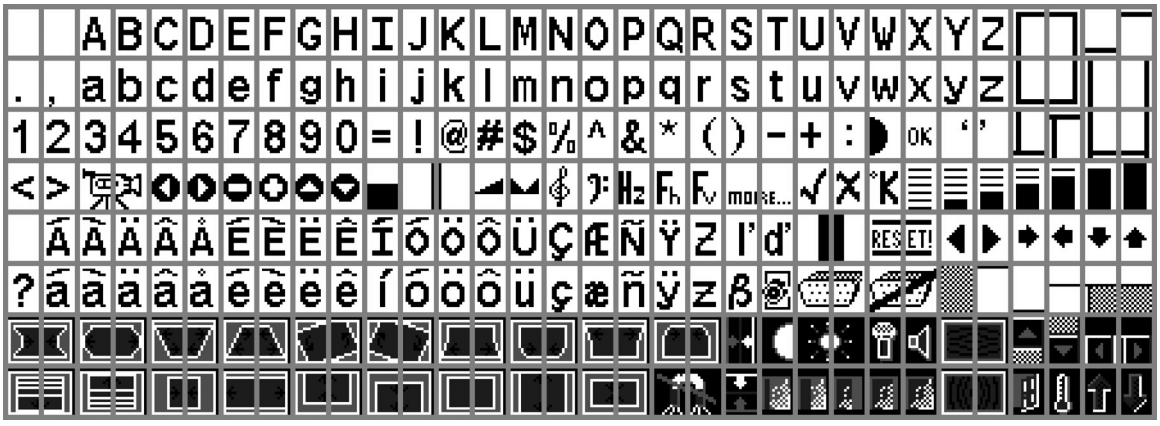
There is no required vertical spacing between Display Window 1 and Display Window 2, but they should not overlap.

There must be a two-character horizontal space between Display Window 1 and Display Window 2 for proper operation of both windows or undefined results may occur.

Evaluation Character Fonts

The character font for evaluation of the LM1237 is shown in *Figure 25*. The actual font will depend on customer customization requirements.

Note that the first two character codes of the two-color font (0x00 and 0x01) are reserved for the Window End (WE) and Row End (RE) codes respectively.

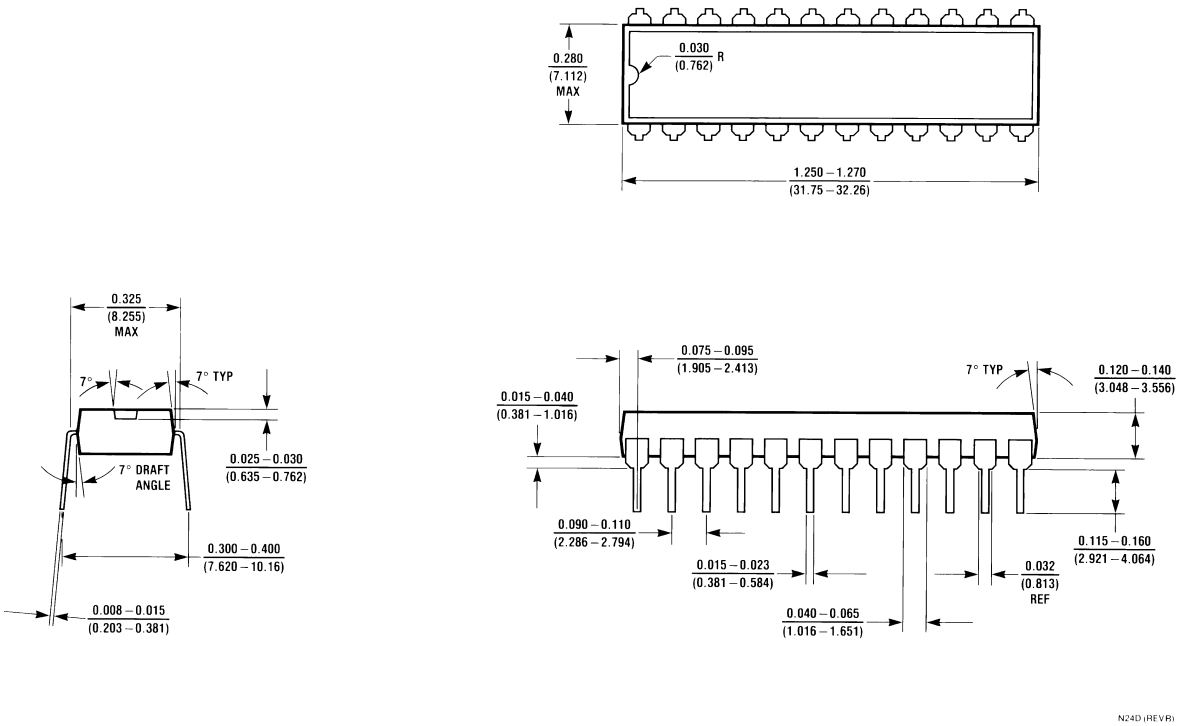


20023445

FIGURE 25. Character Font

Physical Dimensions inches (millimeters)

unless otherwise noted



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