National Semiconductor

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54F/74F2620 • 54F/74F2623 Inverting Octal Bus Transceiver with 25Ω Series Resistors in the Outputs

54F/74F2620 • 54F/74F2623 Inverting Octal Bus Transceiver with 25Ω Series Resistors in the Outputs

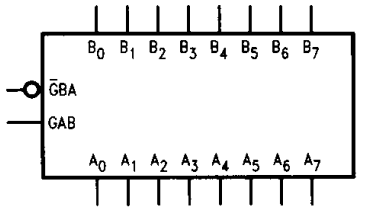
General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. These devices are functionally equivalent to the 'F620 and 'F623. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors. Both busses are capable of sinking 12 mA, sourcing 15 mA, and have TRI-STATE outputs. Dual enable pins (GAB, $\overline{G}$BA) allow data transmission from the A bus to the B bus or from the B bus to the A bus. The 'F2620 is an inverting option of the 'F2623.

Features

- 25Ω series resistors in the outputs eliminate the need for external resistors.
- Designed for asynchronous two-way data flow between busses
- Outputs sink 12 mA and source 15 mA
- Dual enable inputs control direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F2620 is an inverting option of the 'F2623

Logic Symbol



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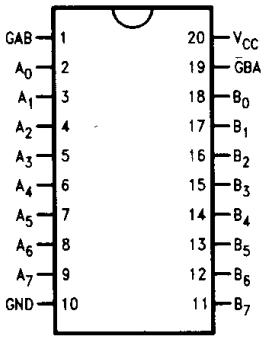
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{G}$BA, GAB	Enable Inputs	1.0/1.0	20 μA/−0.6 mA
A_0–A_7	A Inputs or	3.5/0.667	70 μA/−0.4 mA
	TRI-STATE Outputs	750/20	−15 mA/12 mA
B_0–B_7	B Inputs or	3.5/0.667	70 μA/−0.4 mA
	TRI-STATE Outputs	750/20	−15 mA/12 mA

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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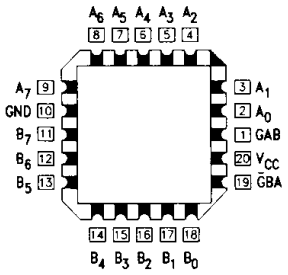
Pin Assignment for LCC



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Functional Description

The enable inputs GAB and $\overline{G}$BA control whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. If both $\overline{G}$BA and GAB are disabled ($\overline{G}$BA HIGH and GAB low), the outputs are in the high impedance state and data is stored at the A and B busses. When $\overline{G}$BA is active (LOW), B data is sent to the A bus. When GAB is active (HIGH), data from the A bus is sent to the B bus. If both enable inputs are active ($\overline{G}$BA LOW and GAB HIGH) B data is sent to the A bus while A data is sent to the B bus.

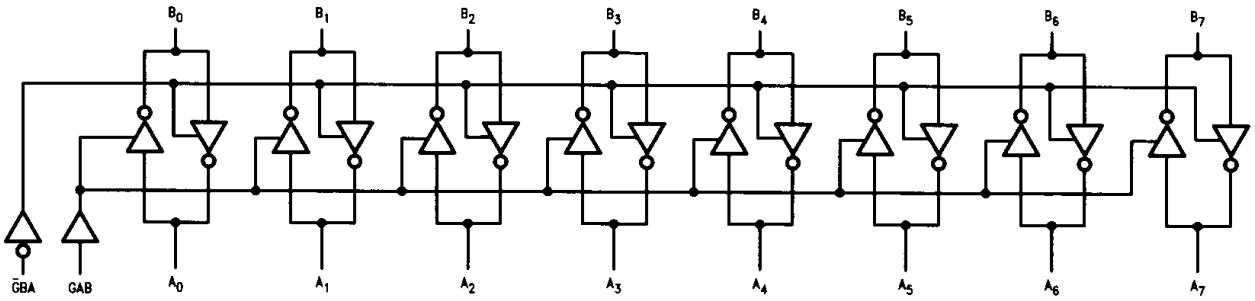
Function Table

Enable Inputs		Operation	
$\overline{G}$BA	GAB	'F2620	'F2623
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus
H	H	$\overline{A}$ Data to B Bus	A Data to B Bus
H	L	Z	Z
L	H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

Logic Diagram

'F2620



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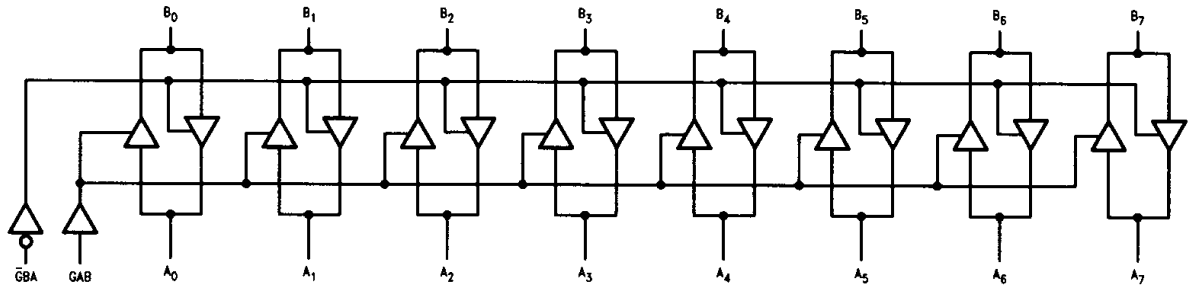
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'F2623



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

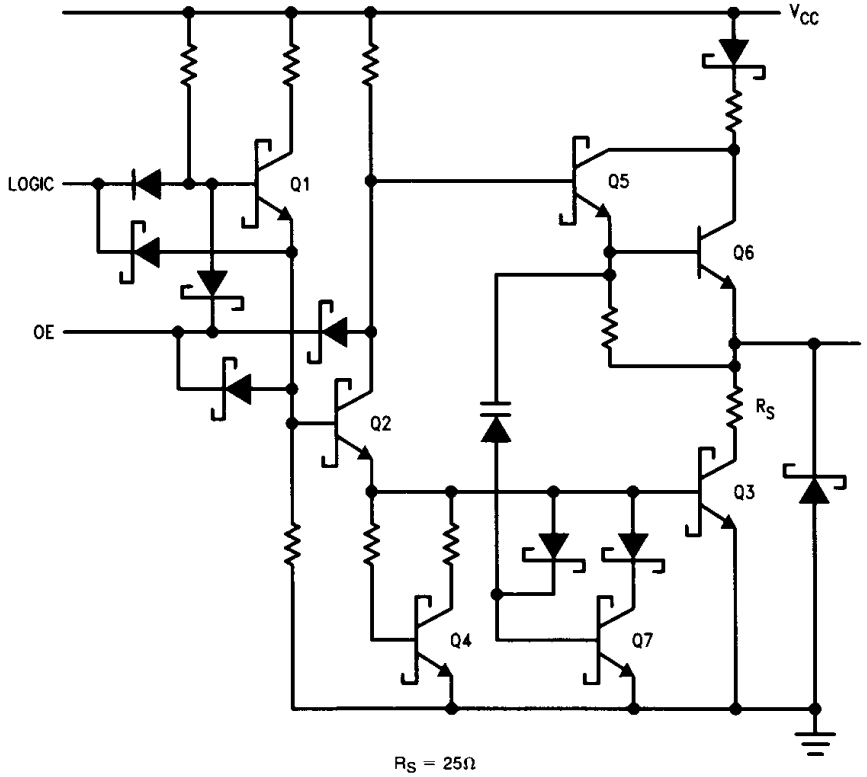
DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.0			V	Min	I_{OH} = −12 mA (A_n, B_n)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage				0.5	V	Min	I_{OL} = 1.0 mA (A_n, B_n)
					0.75			I_{OL} = 12 mA (A_n, B_n)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current ('F2620)				82	mA	Max	V_O = HIGH, V_{IN} = 0.2V
I_{CCL}	Power Supply Current ('F2620)				82	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F2620)				95	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current ('F2623)				82	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F2623)				82	mA	Max	V_O = LOW, V_{IN} = 0.2V
I_{CCZ}	Power Supply Current ('F2623)				95	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output ('F2620)	2.5 3.0		7.5 8.0			2.0 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output ('F2620)	2.5 3.0		7.5 8.0			2.0 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output ('F2623)	1.5 2.5		6.5 7.5			1.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output ('F2623)	1.5 2.5		6.5 7.5			1.5 2.5	7.5 8.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{G}$BA Input to A Output	2.0 2.5		7.0 8.0			2.0 2.0	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{G}$BA Input to A Output	1.5 1.0		6.5 5.5			1.5 1.0	7.5 5.5	
t_{PZH} t_{PZL}	Enable Time GAB Input to B Output ('F2620)	2.0 3.0		7.5 8.0			2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time GAB Input to B Output ('F2620)	2.5 2.0		8.0 7.5			2.0 2.0	9.0 8.0	
t_{PZH} t_{PZL}	Enable Time GAB Input to B Output ('F2623)	2.0 2.5		7.5 8.0			2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time GAB Input to B Output ('F2623)	2.0 2.0		8.0 8.0			2.0 2.0	9.0 8.0	

Basic FAST Circuit Showing Series Resistor Placement



$R_S = 25\Omega$

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Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

74F 2620/2623 P C QR

Temperature Range Family
74F = Commercial FAST
54F = Military FAST

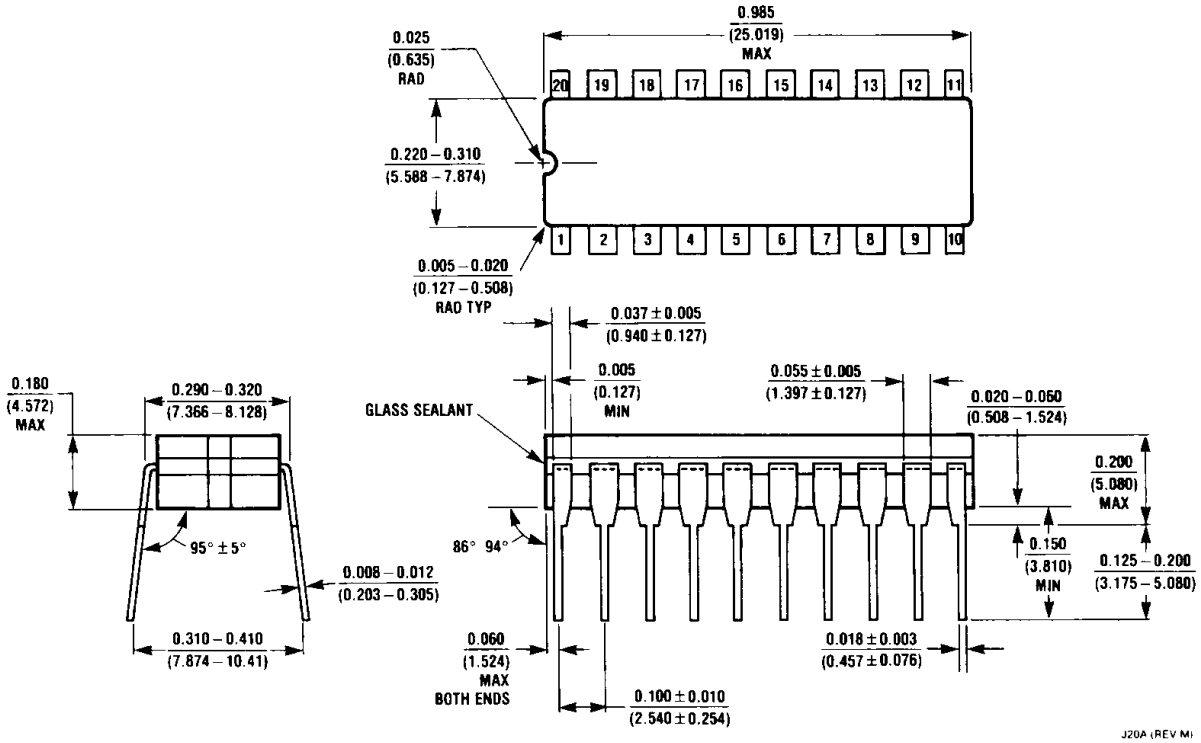
Device Type

Package Code
P = Plastic DIP
D = Ceramic DIP
S = Small Outline (SOIC)

Special Variations
X = Devices shipped in 13" reels
QR = Commercial grade device with burn-in
QB = Military grade device with environmental and burn-in processing shipped in tubes

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

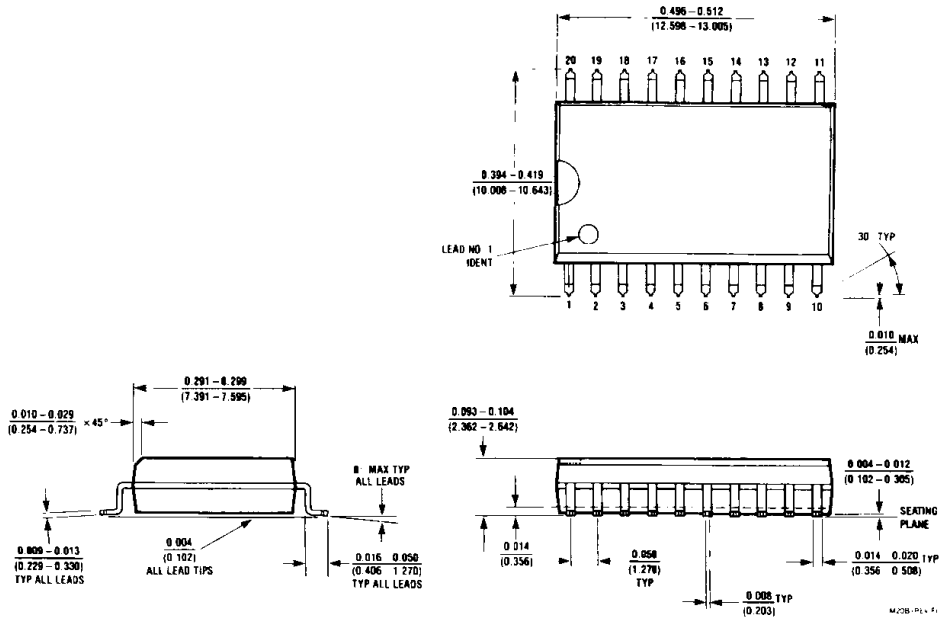
Physical Dimensions inches (millimeters)



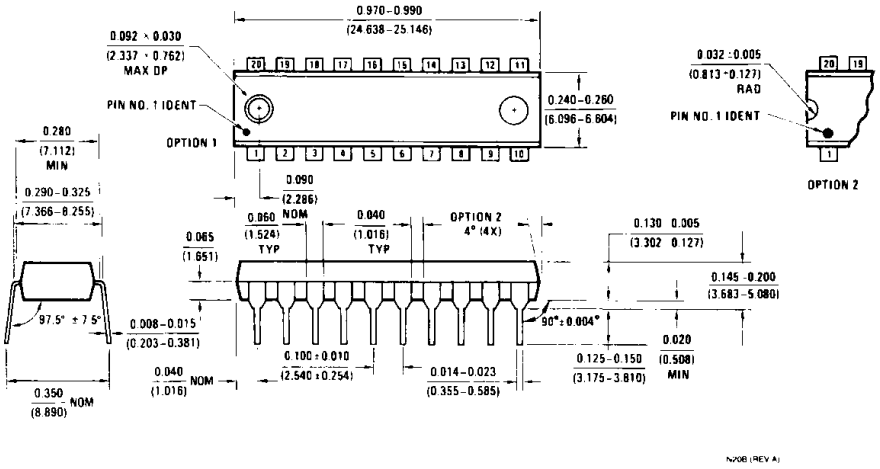
20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114658



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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