National Semiconductor

September 1990

54ACQ/74ACQ244 • 54ACTQ/74ACTQ244
Quiet Series Octal Buffer/Line Driver
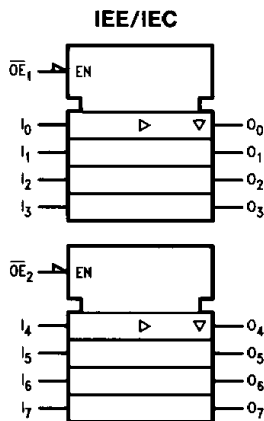# with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT244
- 4 kV minimum ESD immunity
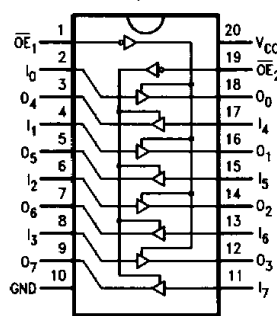- Standard Military Drawing (SMD)
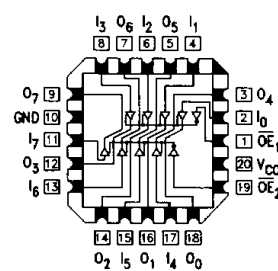 — 'ACTQ244: 5962-8776003

Logic Symbol

IEE/IEC

TL/F/10235–1

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC

TL/F/10235–2

Pin Assignment for LCC and PCC

TL/F/10235–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

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FACT™, FACT Quiet Series™, and GTO™ are trademarks of National Semiconductor Corporation.

RRD-B20M120/Printed in U. S. A.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	$+20$ mA
DC Input Voltage (V_I)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	$+20$ mA
DC Output Voltage (V_O)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	$-65°C$ to $+150°C$
DC Latch-Up Source or Sink Current	± 300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	$-40°C$ to $+85°C$
54ACQ/ACTQ	$-55°C$ to $+125°C$
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$	54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.1 2.25 3.15 2.75 3.85	2.1 3.15 3.85	2.1 3.15 3.85	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 0.9 2.25 1.35 2.75 1.65	0.9 1.35 1.65	0.9 1.35 1.65	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 2.9 4.49 4.4 5.49 5.4	2.9 4.4 5.4	2.9 4.4 5.4	V	$I_{OUT} = -50 \mu A$
		3.0 4.5 5.5	2.56 3.86 4.86	2.4 3.7 4.7	2.46 3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} -12 mA -24 mA -24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.1 0.001 0.1 0.001 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V	$I_{OUT} = 50 \mu A$
		3.0 4.5 5.5	0.36 0.36 0.36	0.50 0.50 0.50	0.44 0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 12 mA 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	± 0.1	± 1.0	± 1.0	μA	$V_I = V_{CC}$, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5		50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5		-50	-75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5	8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)

*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	Vcc (V)	74ACQ TA = +25°C Typ	74ACQ TA = +25°C	54ACQ TA = −55°C to +125°C	74ACQ TA = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	µA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	Figures 1, 2 (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	Figures 1, 2 (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	Vcc (V)	74ACTQ TA = +25°C Typ	74ACTQ TA = +25°C	54ACTQ TA = −55°C to +125°C	74ACTQ TA = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} \quad -24$ mA
		5.5		4.86	4.70	4.76		-24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} \quad 24$ mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	µA	$V_I = V_{CC}, GND$
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−50	−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5	8.0		160.0	80.0	µA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	Figures 1, 2 (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	Figures 1, 2 (Notes 2, 3)

*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	Vcc (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	Vcc* (V)	74ACQ $T_A = +25°C$ $C_L = 50$ pF Min	74ACQ $T_A = +25°C$ $C_L = 50$ pF Typ	74ACQ $T_A = +25°C$ $C_L = 50$ pF Max	54ACQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Min	54ACQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Max	74ACQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	74ACQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3	2.0	7.0	9.0			2.0	9.5	ns
		5.0	1.5	5.0	6.0			1.5	6.5	
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.0	12.0			2.5	12.5	ns
		5.0	1.5	6.5	8.0			1.5	8.5	
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	13.5			1.0	14.0	ns
		5.0	1.0	7.5	9.0			1.0	9.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns
		5.0		0.5	1.0				1.0	

*Voltage Range 5.0 is 5.0V ±0.5V.

Voltage Range 3.3 is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	Vcc* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF Min	74ACTQ $T_A = +25°C$ $C_L = 50$ pF Typ	74ACTQ $T_A = +25°C$ $C_L = 50$ pF Max	54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Min	54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Max	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	5.0	1.5	5.5	6.5	1.5	9.0	1.5	7.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.5	10.5	1.5	9.0	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	9.5	1.5	10.5	1.0	10.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	5.0		0.5	1.0				1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	70	pF	$V_{CC} = 5.0V$

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.

2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.

3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.

4. Set V_{CC} to 5.0V.

5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

• Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

• Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.

• Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

• Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

• First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.

• Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.

• Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.
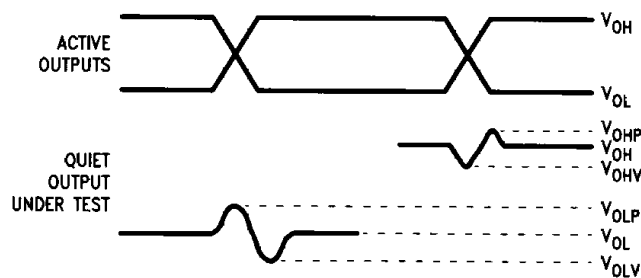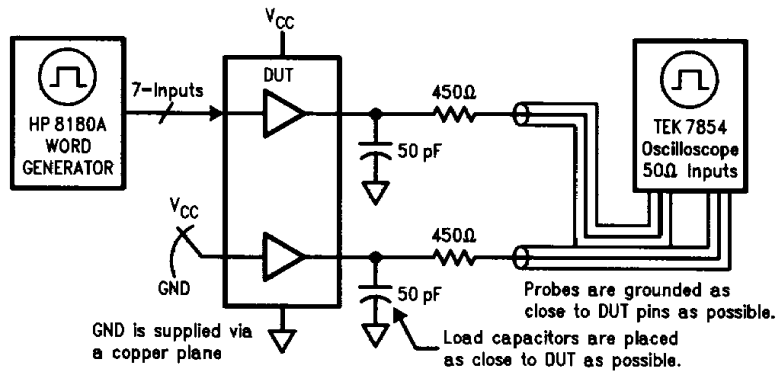

FIGURE 1. Quiet Output Noise Voltage Waveforms

TL/F/10235-4

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: $f = 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.
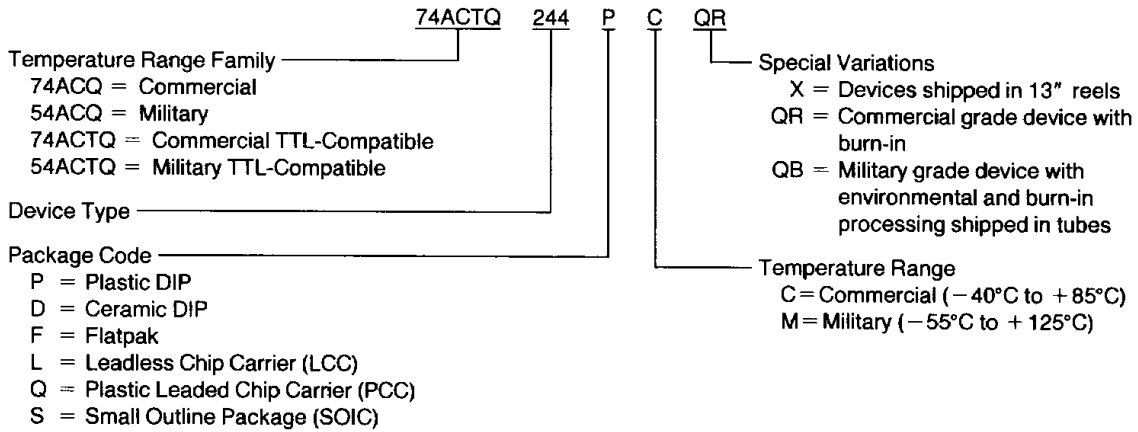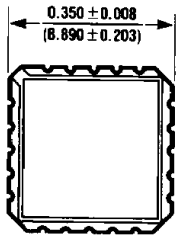
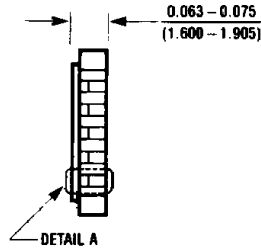FIGURE 2. Simultaneous Switching Test Circuit

TL/F/10235-5

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:
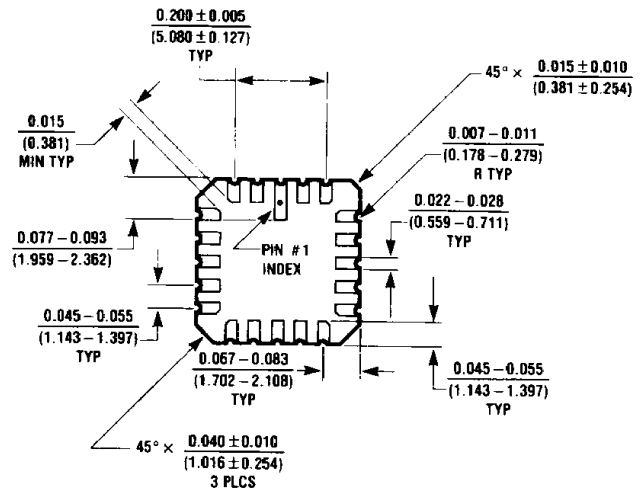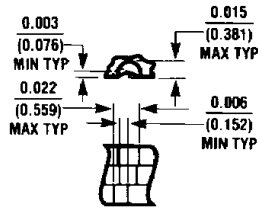
74ACTQ 244 P C QR

Temperature Range Family
  74ACQ = Commercial
  54ACQ = Military
  74ACTQ = Commercial TTL-Compatible
  54ACTQ = Military TTL-Compatible

Device Type

Package Code
  P = Plastic DIP
  D = Ceramic DIP
  F = Flatpak
  L = Leadless Chip Carrier (LCC)
  Q = Plastic Leaded Chip Carrier (PCC)
  S = Small Outline Package (SOIC)

Special Variations
  X = Devices shipped in 13" reels
  QR = Commercial grade device with burn-in
  QB = Military grade device with environmental and burn-in processing shipped in tubes

Temperature Range
  C = Commercial (−40°C to +85°C)
  M = Military (−55°C to +125°C)

6

Physical Dimensions inches (millimeters)

Top View

Side View

DETAIL A

0.350 ± 0.008
(8.890 ± 0.203)

0.063 – 0.075
(1.600 – 1.905)

0.200 ± 0.005
(5.080 ± 0.127)
TYP

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.015
(0.381)
MIN TYP

0.077 – 0.093
(1.959 – 2.362)

PIN #1
INDEX

0.007 – 0.011
(0.178 – 0.279)
R TYP

0.022 – 0.028
(0.559 – 0.711)
TYP

0.045 – 0.055
(1.143 – 1.397)
TYP

0.067 – 0.083
(1.702 – 2.108)
TYP

0.045 – 0.055
(1.143 – 1.397)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

Bottom View

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

Detail A

E20A (REV D)
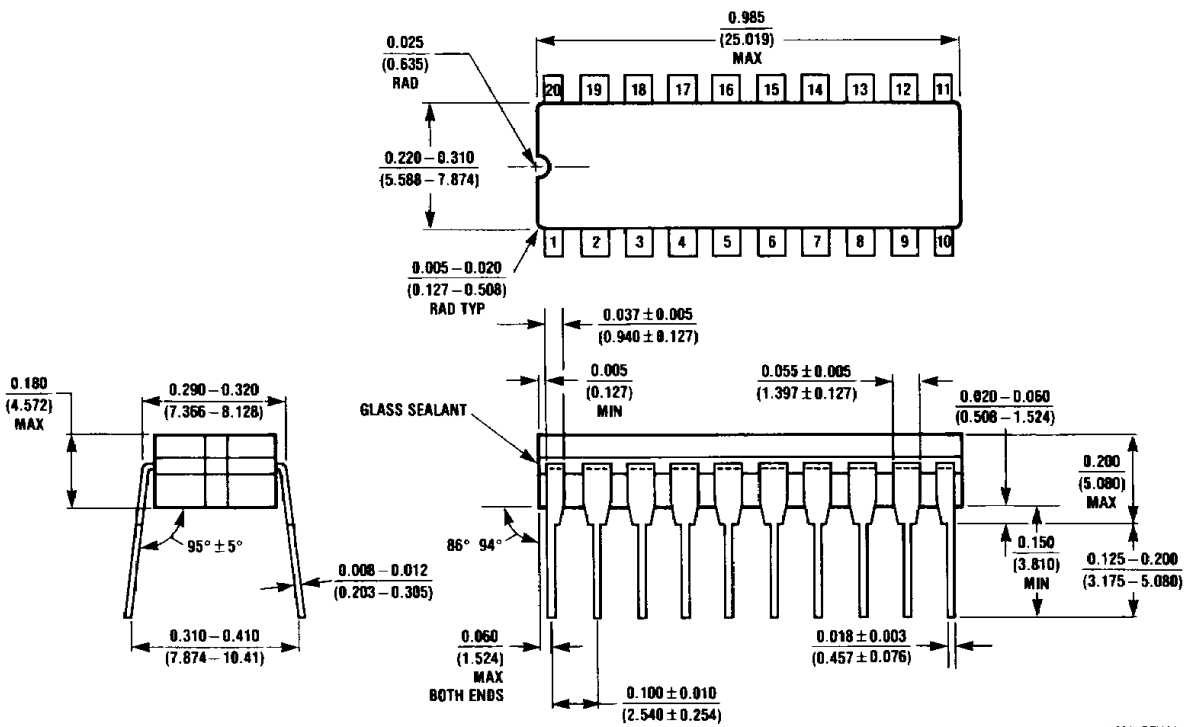
20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A
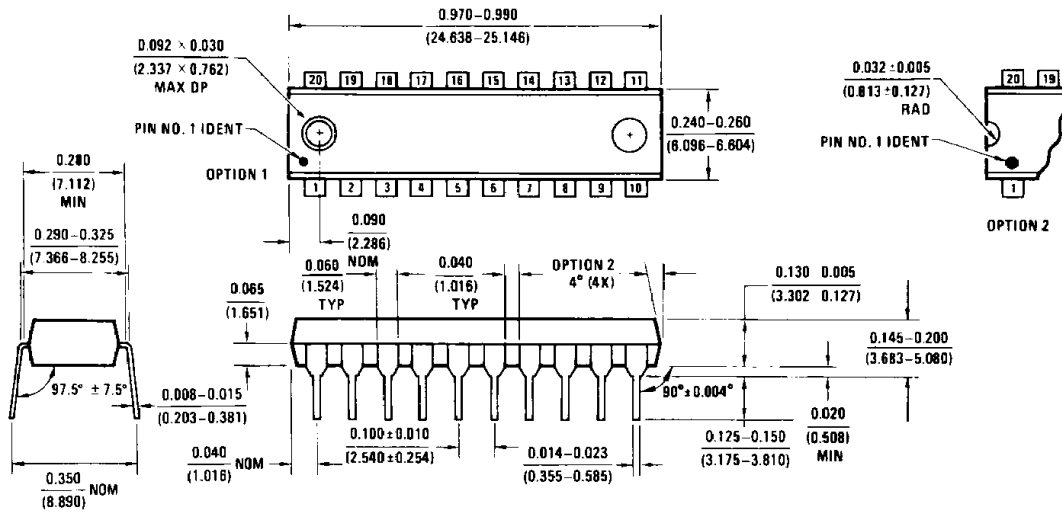
Physical Dimensions inches (millimeters) (Continued)

0.985
(25.019)
MAX

0.025
(0.635)
RAD

0.220 − 0.310
(5.588 − 7.874)

0.005 − 0.020
(0.127 − 0.508)
RAD TYP

0.037 ± 0.005
(0.940 ± 0.127)

0.005
(0.127)
MIN

0.055 ± 0.005
(1.397 ± 0.127)

0.020 − 0.060
(0.508 − 1.524)

GLASS SEALANT

0.180
(4.572)
MAX

0.290 − 0.320
(7.366 − 8.128)

0.200
(5.080)
MAX

95° ± 5°

0.008 − 0.012
(0.203 − 0.305)

86° 94°

0.150
(3.810)
MIN

0.125 − 0.200
(3.175 − 5.080)

0.310 − 0.410
(7.874 − 10.41)

0.060
(1.524)
MAX
BOTH ENDS

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

0.496 − 0.512
(12.598 − 13.005)

0.394 − 0.419
(10.008 − 10.643)

LEAD NO 1
IDENT

30° TYP

0.010 MAX
(0.254)

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

8° MAX TYP
ALL LEADS

SEATING
PLANE

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.014
(0.356)

0.050
(1.270)
TYP

0.014 − 0.020 TYP
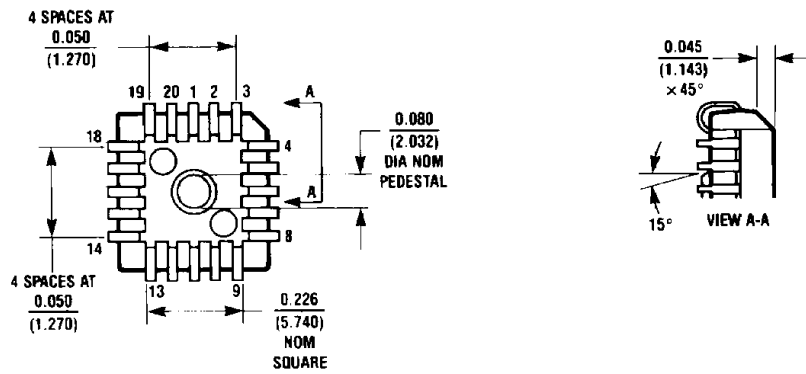(0.356 − 0.508)

0.008 TYP
(0.203)
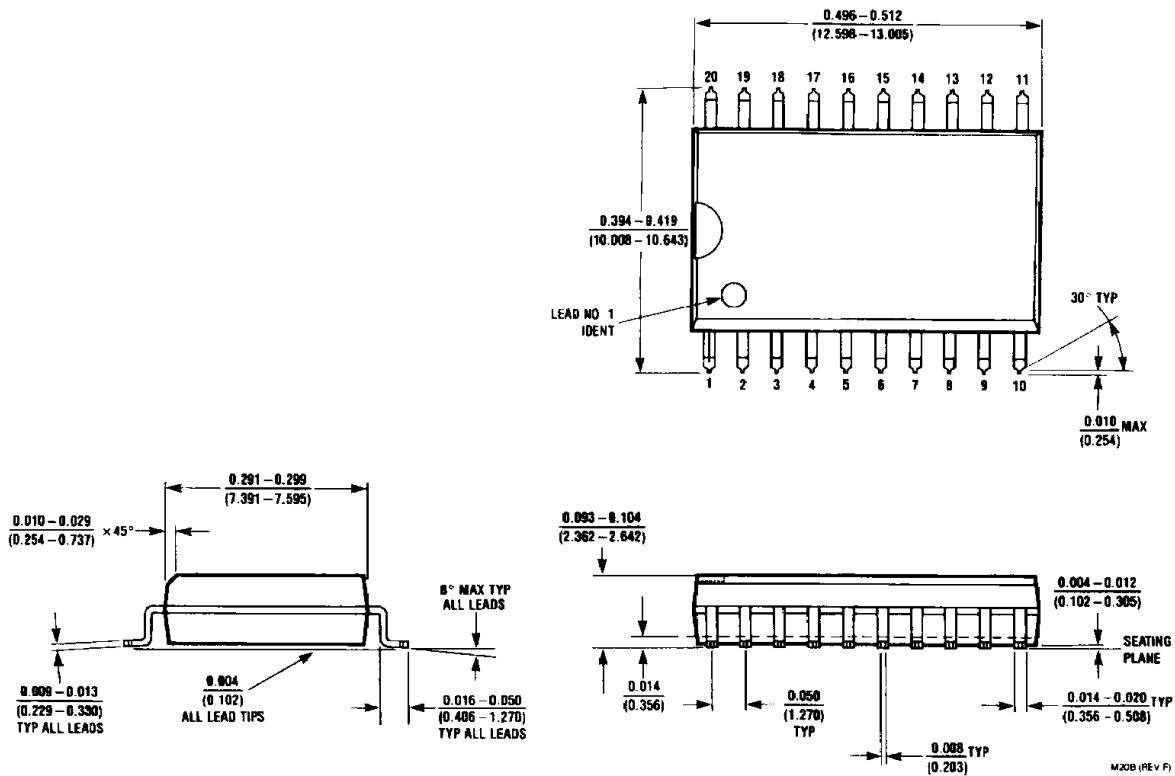
M20B (REV F)

20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

8

Physical Dimensions inches (millimeters) (Continued)

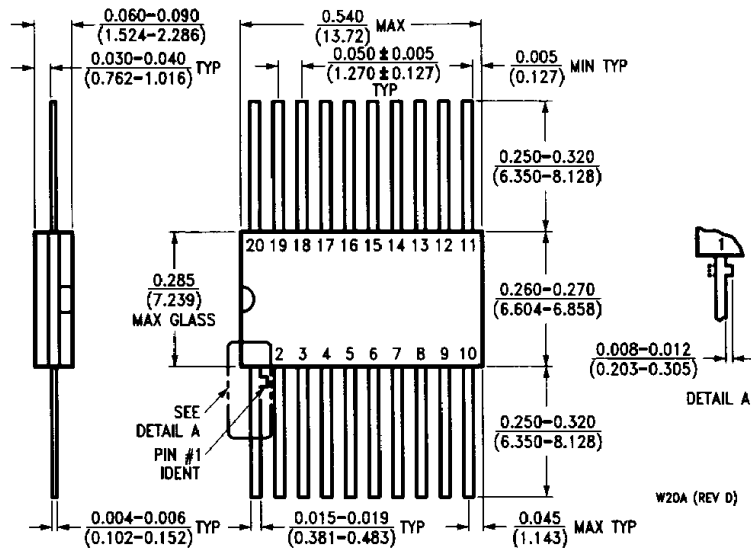20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

20-Lead Plastic Chip Carrier (Q)
NS Package Number V20A

9

Physical Dimensions inches (millimeters) (Continued)

0.060–0.090
(1.524–2.286)

0.030–0.040
(0.762–1.016) TYP

0.540 (13.72) MAX

0.050 ± 0.005
(1.270 ± 0.127) TYP

0.005 (0.127) MIN TYP

0.250–0.320
(6.350–8.128)

20 19 18 17 16 15 14 13 12 11

0.285
(7.239)
MAX GLASS

0.260–0.270
(6.604–6.858)

2 3 4 5 6 7 8 9 10

0.008–0.012
(0.203–0.305)

DETAIL A

SEE DETAIL A
PIN #1 IDENT

0.250–0.320
(6.350–8.128)

W20A (REV D)

0.004–0.006
(0.102–0.152) TYP

0.015–0.019
(0.381–0.483) TYP

0.045
(1.143) MAX TYP

20-Lead Ceramic Flatpak (F)
NS Package Number W20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.