



December 1990

F100331 Low Power Triple D Flip-Flop

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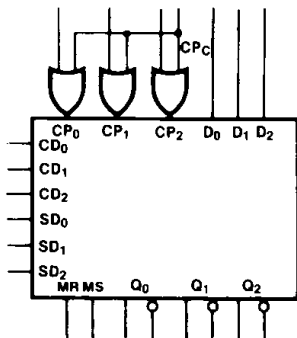
General Description

The F100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the F100131
- 2000V ESD protection
- Pin/function compatible with F100131
- Voltage compensated operating range = -4.2V to -5.7V

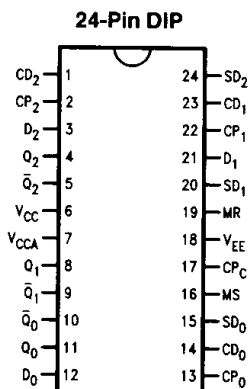
Logic Symbol



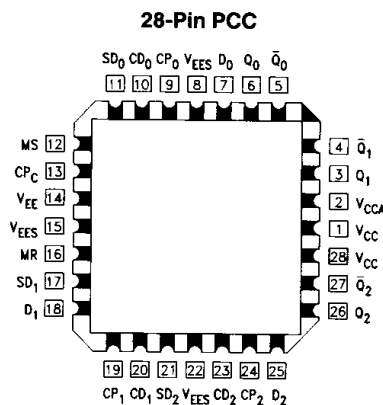
Pin Names	Description
CP ₀ -CP ₂	Individual Clock Inputs
CP _C	Common Clock Input
D ₀ -D ₂	Data Inputs
CD ₀ -CD ₂	Individual Direct Clear Inputs
SD _n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q ₀ -Q ₂	Data Outputs
Q̄ ₀ -Q̄ ₂	Complementary Data Outputs

TL/F/10262-1

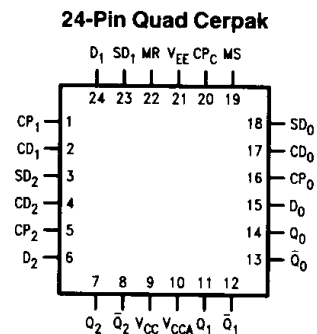
Connection Diagrams



TL/F/10262-2

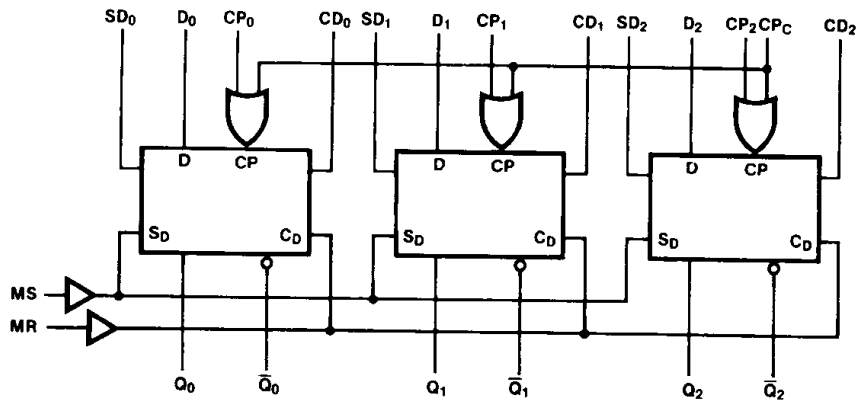


TL/F/10262-4



TL/F/10262-3

Logic Diagram



TL/F/10262-5

Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t + 1)$
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	$Q_n(t)$
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$

Asynchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t + 1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 U = Undefined
 t = Time before CP Positive Transition
 t + 1 = Time after CP Positive Transition
 ↗ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V_{EE})	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V

Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≤ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	-55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	-5.7V to -4.2V
Military	-5.7V to -4.2V

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV	
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)
V_{OLC}	Output LOW Voltage			-1610	mV	
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL}$ (Min)
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH}$ (Max)
I_{EE}	Power Supply Current	-122		-65	mA	Inputs Open

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operate under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	Figures 2 and 3	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns	Figures 1 and 3	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.75	2.00	0.75	2.00	0.75	2.00	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.70	0.70	1.70	0.70	1.80	ns	$CP_n, CP_C = L$	Figures 1 and 4
t_{PLH} t_{PHL}		0.70	2.00	0.70	2.00	0.70	2.00		$CP_n, CP_C = H$	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.60	1.10	2.60	1.10	2.60	ns	$CP_n, CP_C = L$	
t_{PLH} t_{PHL}		1.10	2.80	1.10	2.80	1.10	2.80		$CP_n, CP_C = H$	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	Figures 1, 3 and 4	
t_s	Setup Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	0.40		0.40		0.40		ns	Figure 5	
		1.30		1.30		1.30			Figure 4	
		2.30		2.30		2.30				
t_h	Hold Time D_n	1.00		1.00		1.00		ns	Figure 5	
$t_{pw(H)}$	Pulse Width HIGH $CP_n, CP_C, CD_n,$ SD_n, MR, MS	2.00		2.00		2.00		ns	Figures 3 and 4	

PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	Figures 2 and 3	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns	Figures 1 and 3	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.75	1.80	0.75	1.80	0.75	1.80	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.50	0.70	1.50	0.70	1.60	ns	$CP_n, CP_C = L$	Figures 1 and 4
t_{PLH} t_{PHL}		0.70	1.80	0.70	1.80	0.70	1.80		$CP_n, CP_C = H$	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.40	1.10	2.40	1.10	2.40	ns	$CP_n, CP_C = L$	
t_{PLH} t_{PHL}		1.10	2.60	1.10	2.60	1.10	2.60		$CP_n, CP_C = H$	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	Figures 1, 3 and 4	
t_s	Setup Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	0.30		0.30		0.30		ns	Figure 5	
		1.20		1.20		1.20			Figure 4	
		2.20		2.20		2.20				
t_h	Hold Time D_n	0.90		0.90		0.90		ns	Figure 5	
$t_{pw(H)}$	Pulse Width HIGH $CP_n, CP_C, CD_n,$ SD_n, MR, MS	2.00		2.00		2.00		ns	Figures 3 and 4	
$t_{s\ G-G}$	Skew, Gate to Gate	TBD		TBD		TBD		ps	PCC Only (Note 1)	

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1085	-870	mV	$-55^{\circ}C$			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^{\circ}C$ to $+125^{\circ}C$			
		-1830	-1555	mV	$-55^{\circ}C$			
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to $-2.0V$	1, 2, 3
		-1085		mV	$-55^{\circ}C$			
V_{OLC}	Output LOW Voltage		-1610	mV	$0^{\circ}C$ to $+125^{\circ}C$			
			-1555	mV	$-55^{\circ}C$			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Guaranteed HIGH Signal for all Inputs	1, 2, 3, 4	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Guaranteed LOW Signal for all Inputs	1, 2, 3, 4	
I_{IL}	Input LOW Current	0.50		μA	$-55^{\circ}C$ to $+125^{\circ}C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	1, 2, 3	
I_{IH}	Input HIGH Current		240	μA	$0^{\circ}C$ to $+125^{\circ}C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	1, 2, 3	
			340	μA	$-55^{\circ}C$			
I_{EE}	Power Supply Current	-130	-50	mA	$-55^{\circ}C$ to $+125^{\circ}C$	Inputs Open	1, 2, 3	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^{\circ}C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups, 1, 2, 3, 7 and 8.

Note 3: Sampled tested (Method 5005, Table I) on each manufactured lot at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups A1, 2, 3, 7 and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	350		350		350		MHz	Figures 2 and 3	4
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	Figures 1 and 3	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		0.50	2.40	0.60	2.10	0.50	2.50			
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	0.70	2.70	0.80	2.60	0.80	2.90	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		0.70	2.90	0.80	2.80	0.80	3.10		CP _n , CP _C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20	1.40	ns	Figures 1, 3 and 4	
t_s	Setup Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	1.00		0.80		0.90		ns	Figure 5	
		1.50		1.30		1.60			Figure 4	
		2.50		2.30		2.50				
t_h	Hold Time D_n	1.50		1.30		1.60		ns	Figure 5	
$t_{pw(H)}$	Pulse Width HIGH $CP_n, CP_C, CD_n,$ SD_n, MR, MS	2.00		2.00		2.00		ns	Figures 3 and 4	

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	375		375		375		MHz	Figures 2 and 3	4
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.50	2.00	0.60	1.80	0.50	2.20	ns	Figures 1 and 3	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.50	2.00	0.60	1.80	0.50	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.50	2.00	0.60	1.80	0.50	2.20	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		0.50	2.20	0.60	1.90	0.50	2.30			
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	0.70	2.50	0.80	2.40	0.80	2.70	ns	CP _n , CP _C = L	
t_{PLH} t_{PHL}		0.70	2.70	0.80	2.60	0.80	2.90		CP _n , CP _C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.20	0.20	1.20	0.20	1.20	ns	Figures 1, 3 and 4	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$. Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$, and $-55^\circ C$ Temp., Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ Temperature (design characterization data).

Cerpak AC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_s	Setup Time									4
	D_n	0.90		0.70		0.80		ns	Figures 4 and 5	
	CD_n, SD_n (Release Time)	1.40		1.20		1.50				
	MS, MR (Release Time)	2.40		2.20		2.40				
t_h	Hold Time D_n	1.40		1.20		1.50		ns	Figure 5	
$t_{pw(H)}$	Pulse Width HIGH									
	$CP_n, CPC, CD_n,$ SD_n, MR, MS	2.00		2.00		2.00		ns	Figures 3 and 4	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$. Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$, and $-55^\circ C$ Temp., Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ Temperature (design characterization data).

Test Circuits

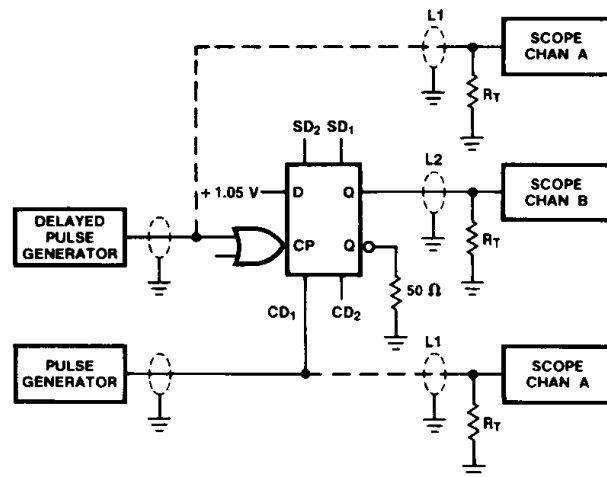


FIGURE 1. AC Test Circuit

TL/F/10262-6

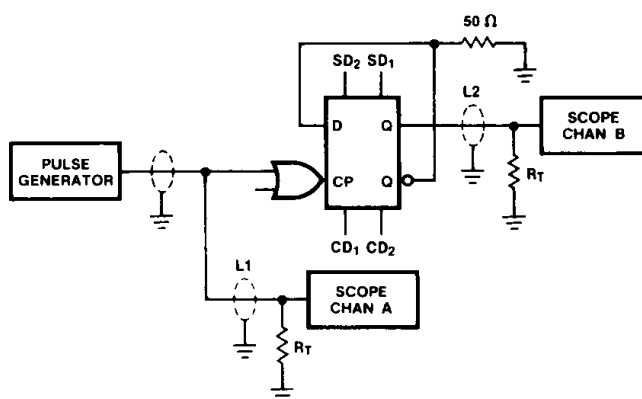


FIGURE 2. Toggle Frequency Test Circuit

TL/F/10262-7

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = Equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

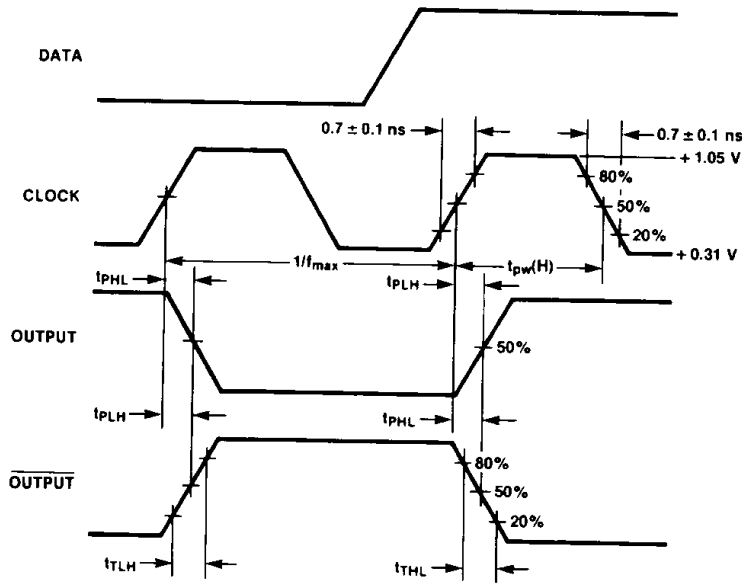


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/10262-8

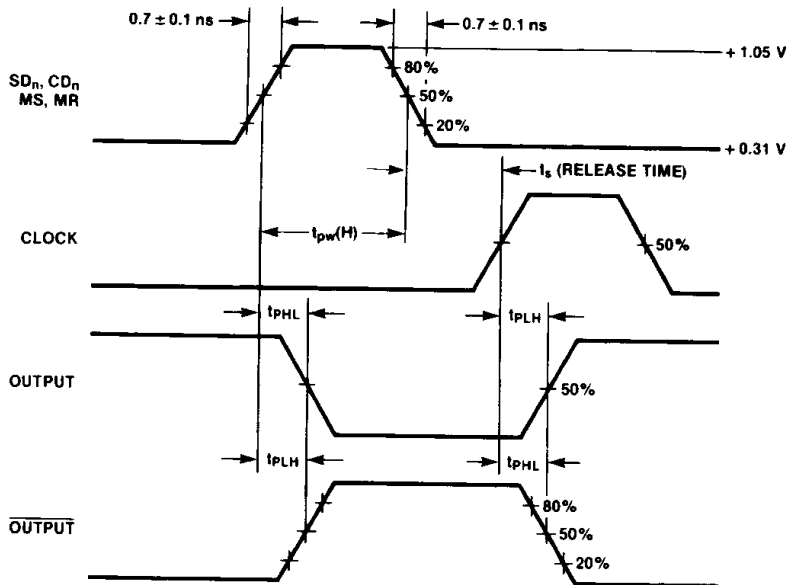


FIGURE 4. Propagation Delay (Resets)

TL/F/10262-9

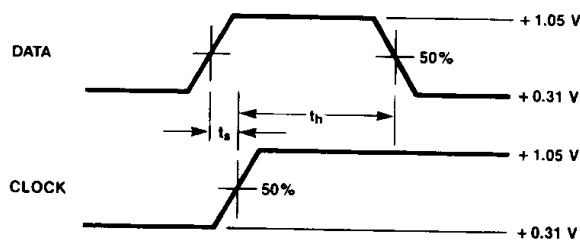


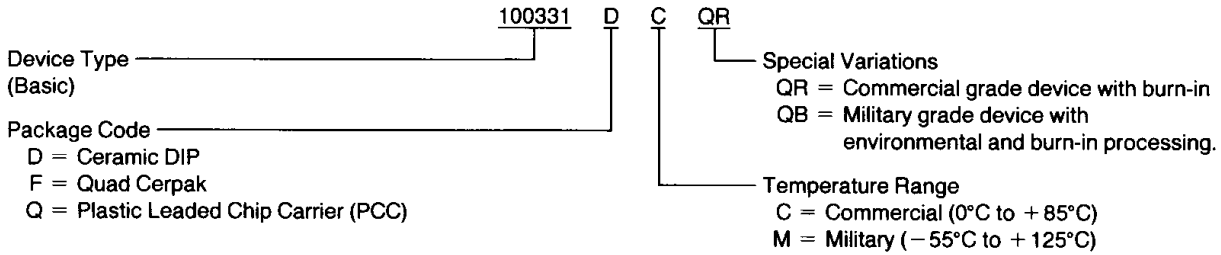
FIGURE 5. Data Setup and Hold Time

TL/F/10262-10

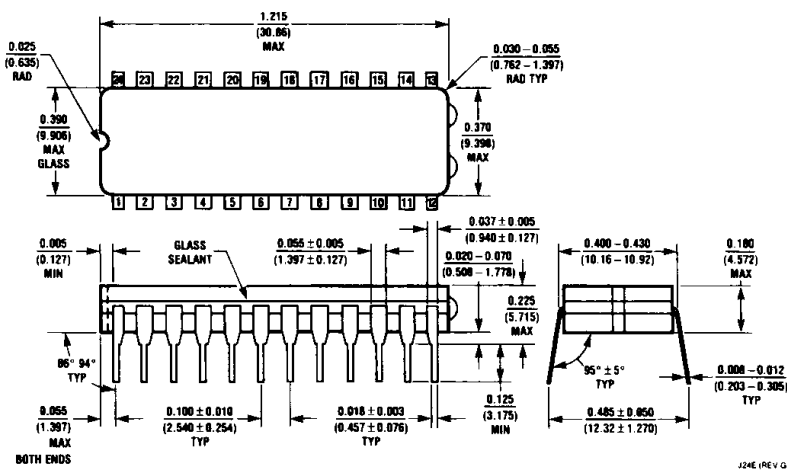
Note: t_s is the minimum time before the transition of the clock that information must be present at the data input.
Note: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

Ordering Information

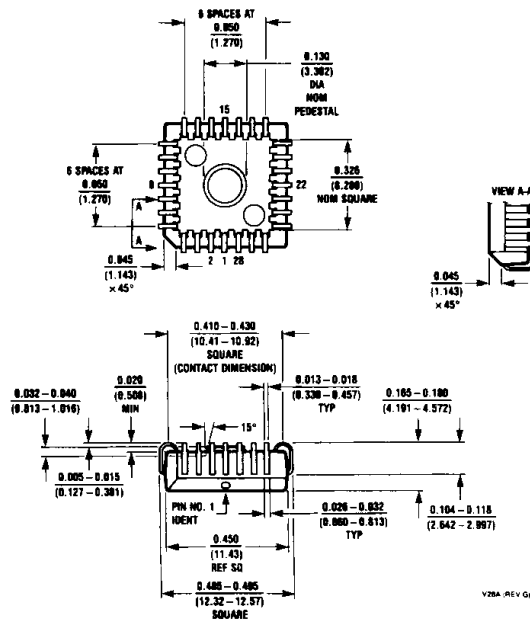
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)



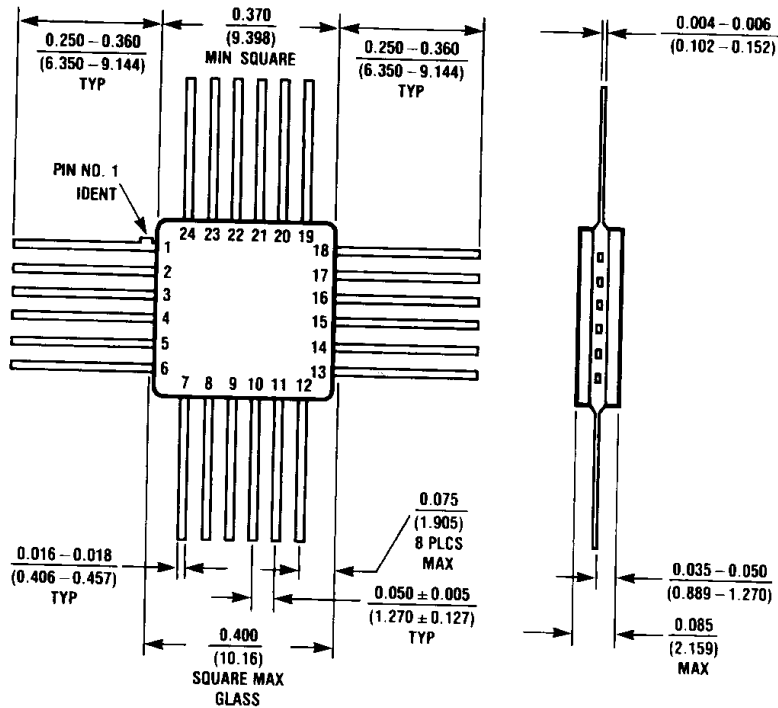
24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



28-Lead Plastic Chip Carrier (Q)
NS Package Number V28A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114912



**24-Lead Quad Cerpak (F)
NS Package Number W24B**

W24B (REV C)

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-6090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanso Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
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National Semicondutores Do Brasil Ltda.
Av. Bng. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
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National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victoria, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458