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NTE5480 thru NTE5487
Silicon Controlled Rectifier (SCR)
8 Amp

Description:

The NTE5480 through NTE5487 are multi–purpose PNPN silicon controlled rectifiers in a TO64 type package suited for industrial and consumer applications. These 8 amp devices are available in voltages ranging from 25V to 600V.

Features:

- Uniform Low–Level Noise–Immune Gate Triggering: I_{GT} = 10mA Typ @ T_C = +25°C
- Low Forward "ON" Voltage: v_T = 1V Typ @ 5A @ +25°C
- High Surge–Current Capability: I_{TSM} = 100A Peak
- Shorted Emitter Construction

Absolute Maximum Ratings: (T_J = –40° to +100°C unless otherwise specified)

Peak Repetitive Forward and Reverse Blocking Voltage (Note 1), V_{DRM} or V_{RRM}
- NTE5480 . . . . . 25V
- NTE5481 . . . . . 50V
- NTE5482 . . . . . 100V
- NTE5483 . . . . . 200V
- NTE5484 . . . . . 300V
- NTE5485 . . . . . 400V
- NTE5486 . . . . . 500V
- NTE5487 **(This device is discontinued)** 600V

Forward Current RMS, $I_{T(RMS)}$ 8A
Peak Forward Surge Current (One Cycle, 60Hz, T_J = –40° to +100°C, I_{TSM} 100A
Circuit Fusing ($t \le 8.3$ms, T_J = –40° to +100°C), I^2t . . . . . $40A^2s$
Peak Gate Power, P_{GM} 5W
Average Gate Power, $P_{G(AV)}$ 0.5W
Peak Gate Current, I_{GM} 2A
Peak Gate Voltage (Note 2), V_{GM} 10V
Operating Temperature Range, T_J . . . . . –40° to +100°C
Storage Temperature Range, T_{stg} . . . . . –40° to +150°C
Typical Thermal Resistance, Junction–to–Case, R_{thJC} . . . . . 1.5°C/W
Typical Thermal Resistance, Case–to–Ambient, R_{thJA} . . . . . 50°C/W

Note 1. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

Note 2. Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.

Electrical Characteristics: (T_C = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current	I_{DRM}, I_{RRM}	Rated V_{DRM} or V_{RRM}, Gate Open	T_J = +25°C	–	–	10	µA
			T_J = +100°C	–	–	2	mA
Gate Trigger Current (Continuous DC)	I_{GT}	V_D = 7V, R_L = 100Ω, Note 3		–	10	30	mA
			T_C = –40°C	–	–	60	mA
Gate Trigger Voltage (Continuous DC)	V_{GT}	V_D = 7V, R_L = 100Ω		–	0.75	1.5	V
			T_C = –40°C	–	–	2.5	V
			T_J = +100°C	0.2	–	–	V
Forward "ON" Voltage	v_{TM}	I_{TM} = 15.7A, Note 4		–	1.4	2.0	V
Holding Current	I_H	V_D = 7V, Gate Open		–	10	30	mA
			T_C = –40°C	–	–	60	mA
Turn–On Time (t_d + t_r)	t_{on}	I_G = 20mA, I_F = 5A, V_D = Rated V_{DRM}		–	1	–	µs
Turn–Off Time	t_{off}	I_F = 5A, I_R = 5A, dv/dt = 30V/µs		–	15	–	µs
			T_J = +100°C, V_D = Rated V_{DRM}	–	25	–	µs
Forward Voltage Application Rate (Exponential)	dv/dt	Gate Open, T_J = +100°C, V_D = Rated V_{DRM}		–	50	–	V/µs

Note 3. For optimum operation, i.e. faster turn–on, lower switching losses, best di/dt capability, recommended I_{GT} = 200mA minimum.

Note 4. Pulsed, 1ms max., Duty Cycle ≤ 1%.