NT7501

33 X 100 RAM-Map LCD Controller/Driver

Features

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (In normal display mode)
- RAM capacity: 65 X 132 = 8580 bits
- Many command functions: Read/Write Display Data, Display ON/OFF, Normal/Reverse Display, Page Address Set, Set Display Start Line, Set LCD Bias, Electronic contrast Controls, Read Modify Write, Select Segment Driver Direction and Power Save
- High-speed 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800
- Serial interface
- Single supply operation, 2.4 - 3.5V
- Maximum 9V LCD driving output voltage
- 2X / 3X / 4X on chip DC-DC converter
- Voltage regulator
- Voltage follower (LCD bias: 1/5 or 1/6)
- On chip oscillator

General Description

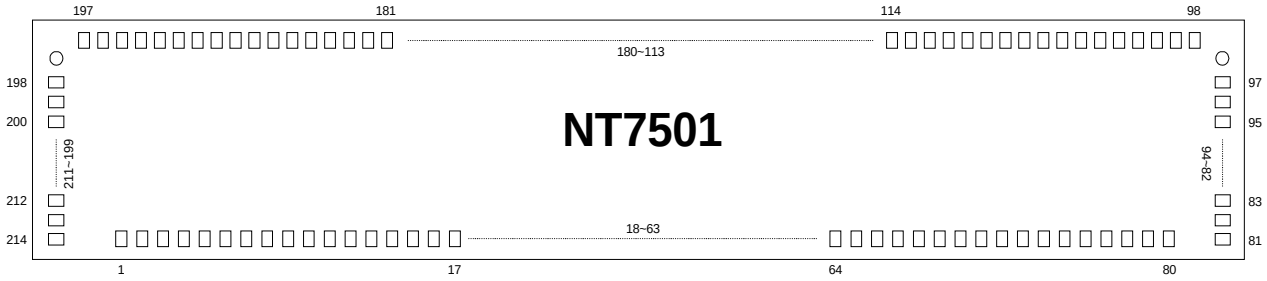
The NT7501 is a single-chip LCD driver for dot-matrix liquid crystal displays, which is directly connectable to a microcomputer bus. It accepts 8-bit serial or parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates a LCD drive signal independent of the microprocessor clock.

The set of the on-chip display RAM of 65 X 132 bits, and a one-to-one correspondence between the LCD panel pixel dots and the on-chip RAM bits, permits implementation of displays with a high degree of freedom.

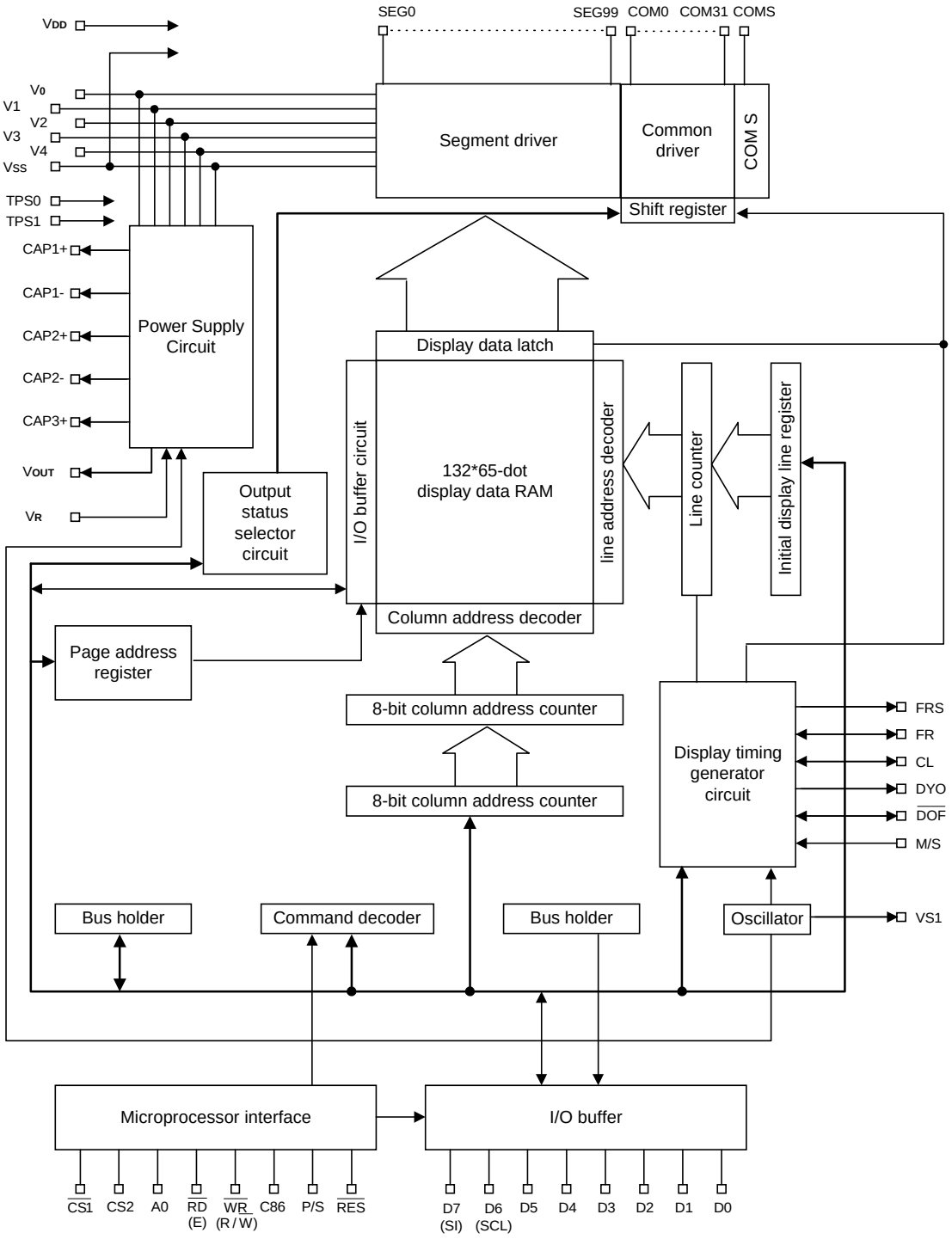
As a total of 133 circuits of common and segment outputs are incorporated, a single chip of NT7501 can make 33 X 100 dots displays.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with minimal current consumption and a minute LSI configuration.

Pad Configuration



Block Diagram



Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
20 - 26	V_{DD}	Supply	2.4 - 3.5V power supply input. These pads must be connected to each other
35 - 42	V_{SS}	Supply	Ground input. These pads must be connected to each other
63 - 64 65 - 66 67 - 68 69 - 70 71 - 72	V_0 V_1 V_2 V_3 V_4	Supply	LCD driver supply voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should have the following relationship: $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ When the on-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command

V1	V2	V3	V4
4/5V0, 5/6V0	3/5V0, 4/6V0	2/5V0, 2/6V0	1/5V0, 1/6V0

LCD Driver Supplies

Pad No.	Symbol	I/O	Description
47 - 48	CAP1-	O	Capacitor 1- pad for internal DC/DC voltage converter
49 - 50	CAP1+	O	Capacitor 1+ pad for internal DC/DC voltage converter
51 - 52	CAP2-	O	Capacitor 2- pad for internal DC/DC voltage converter
53 - 54	CAP2+	O	Capacitor 2+ pad for internal DC/DC voltage converter
45 - 46	CAP3+	O	Capacitor 3+ pad for internal DC/DC voltage converter
12, 61 - 62, 77	V_{DD}	Supply	Used for pad option or to connect to power filter capacitor
9, 15, 59 - 60, 73 - 74	V_{SS}	Supply	Used for pad option or to connect to power filter capacitor
43 - 44	V_{OUT}	O	DC/DC voltage converter output
55 - 56	V_0	O	Connect to Rb
57 - 58	V_R	I	Voltage adjustment pad. Applies voltage between V_0 and V_{SS} using a resistive divider
75 - 76	TPS0, TPS1	I	Selects the temperature coefficient of the reference voltage

System Bus Connection Terminals

Pad No.	Symbol	I/O	Description
27 - 34	D0 - D7 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
16	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicate that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
8	$\overline{RES}$	I	When $\overline{RES}$ is set to "L", the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.
11 - 13	$\overline{CS1}$ CS2	I	This is the chip select signal. When $\overline{CS1}$ = "L" and CS2 = "H", then the chip select becomes active and data/command I/O are enabled
18	$\overline{RD}$ (E)	I	When connected to an 8080 MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080MPU, and the NT7501 data bus is in an output statue when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
17	$\overline{WR}$ (R/$\overline{W}$)	I	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{WR}$ signal . The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ = "H": Read. When R/$\overline{W}$ = "L": Write.
14	C86	I	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.
10	P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input. The following applies depending on the P/S status: <table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$ $\overline{WR}$</td><td></td></tr><tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table> When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.
7	M/S	I	This terminal selects the master/slave operation for the NT7501 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
4	CL	I/O	This is the display clock input terminal. When the NT7501 chips are used in master/slave mode, the various CL terminals must be connected.

System Bus Connection Terminals (continue)

Pad No.	Symbol	I/O	Description
2	FR	I/O	This is the liquid crystal alternating current signal I/O terminal. M/S = "H": Output M/S = "L": Input When the NT7501 chip is used in master/slave mode, the various FR terminals must be connected.
3	DYO	O	Common drive signal output. This output is enabled for only in master operation and connects to the common driver DIO pad. It becomes HZ in slave operation.
6	VS1	O	Internal power supply voltage monitor output.
5	$\overline{DOF}$	I/O	This is the liquid crystal display blanking control terminal. M/S = "H": Output M/S = "L": Input When the NT7501 chip is used in master/slave mode, the various $\overline{DOF}$ terminals must be connected
1	FRS	O	This is the output terminal for the static drive. This terminal is only enabled when the static indicator is ON when in master operation mode, and is used in conjunction with the FR terminal.

Liquid Crystal Drive Pads

Pad No.	Symbol	I/O	Description
98 - 197	SEG0 - 99	O	Segment signal output for LCD display
81 - 96, 198 - 213	COM15 - 0 COM16 - 31	O	Common signal output for LCD display
97, 214	COMS	O	These are the COM output terminals for the indicator. Both terminals output the same signal. Do not connect these terminals if they are not used. When in master/slave mode, the same signal is output by both master and slave.

Option Pads

Pad No.	Symbol	I/O	Description
78 - 80	OP1 - OP3	I	Internal pull high, no connection for user

Functional Description

Microprocessor Interface

Interface type selection

The NT7501 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of the P/S pad, either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table 1.

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
H	Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
L	Serial Input	$\overline{CS1}$	CS2	A0	-	-	-	SI	SCL	(HZ)

"-" must always be high or low

Parallel Input

When the NT7501 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low as shown in Table 2.

Table 2.

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 to D7
H	6800 microprocessor bus	$\overline{CS1}$	CS2	A0	E	$R/\overline{W}$	D0 to D7
L	8080 microprocessor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{RW}$	D0 to D7

Data Bus Signals

The NT7501 identifies the data bus signal according to A0, E, $R/\overline{W}$ ($\overline{RD}$, $\overline{WR}$) signals.

Table 3.

Common	6800 processor	8080 processor		Function
A0	($R/\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Reads status
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (P/S is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When the chip is not selected, the shift register and counter are reset. The serial data of D7, D6, ···D0 are read at D7 in this sequence when the serial clock (SCL) goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.

The serial data input (SI) is determined to be the display data when A0 is high, and the control data when A0 is low. A0 is read on the rising edge of every eighth clock signal.

Figure1 shows a timing chart of serial interface signals. The serial clock sign must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

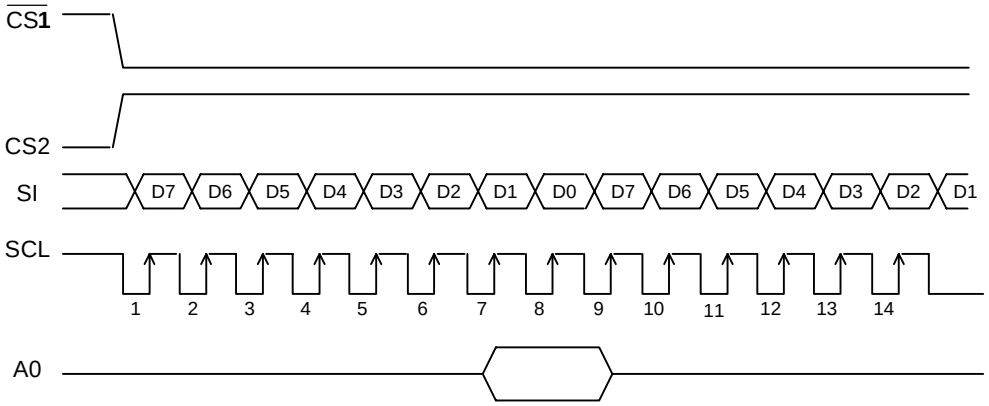


Figure 1.

Chip Select Inputs

The NT7501 has two chip select pads, $\overline{CS1}$ and CS2 can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high.

When these pads are set to any other combination, D0 to D7 are high impedance and A0, E and $R/\overline{W}$ inputs are disabled. When the serial input interface is selected. the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The NT7501 can perform a series of pipeline processes between the LSI's using the bus holder of the internal data bus in order to match the operating frequency of the display RAM and the internal registers with that of the microprocessor. For example, the microprocessor reads data from the display RAM in the first read (dummy) cycle, stores it in the bus holder and outputs it onto the system bus in the next data read cycle.
Also, the microprocessor temporarily stores display data in the bus holder, and stores it in the display RAM until the next data write cycle starts.
When viewed from the microprocessor, the NT7501 access speed greatly depends on the cycle time rather than the access time to the display RAM (t_{ACC}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the read instruction immediately following. Instead, the address data is output only during second data read. A single dummy read must be inserted after the address setup and after write cycle (refer to Figure2).

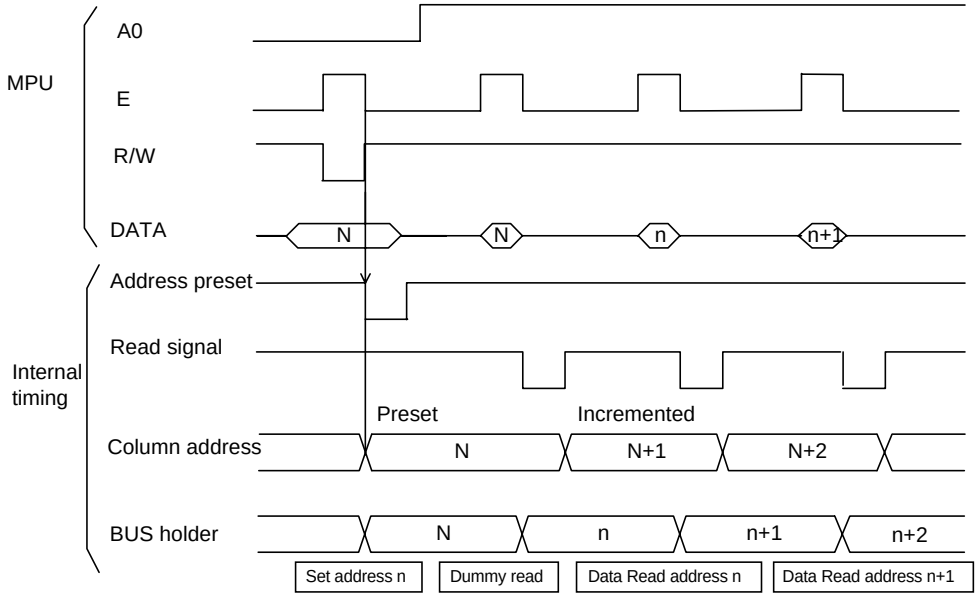


Figure 2.

Busy Flag

The Busy flag is set when the NT7501 starts to operate. During operation, it accepts Read Status instruction only. The busy flag signal is output at pad D7 when Read Status is issued. If the cycle time (t**CYC**) is correct, the microprocessor need not check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line, according to COM0 (usually, the top line of screen), is determined using register data. The register is also used for screen scrolling and page switching.

The set Display Start Line command sets the 6-bit display start address in this register. The register data is preset on the line counter each time the FR signal status changes. The line counter is incremented by CL signal and it generates a line address to allow 132 bit.

Column Address Counter

This is a 8 bit presettable counter that provides the column address to the display RAM (refer to Figure4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of the Page Address register.

When the ADC Select command is issued to display an inverse display, the column address decoder inverts the relationship between the RAM column address and the display segment output.

Page Address Register

This is a 4-bit page address register that provides a page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 8 (D3 is high, but D2,D1 and D0 are low) is RAM area dedicated to the indicator, and only display data D0 is valid.

Display Data RAM

The display data RAM stores pixel data for the LCD. It is a 65-column by 132-row (8-page by 8 bit + 1) addressable array. Each pixel can be selected when the page and column addresses are specified.

The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to the LCD common lines as shown in Figure 3. Therefore, multiple NT7501's can easily configure a large display having high flexibility with very little data transmission restriction.

The microprocessor writes and reads data to/from the RAM through the I/O buffer. As the LCD controller operates independently, data can be written into the RAM at the same time as the data is being displayed, without causing the LCD to flicker.

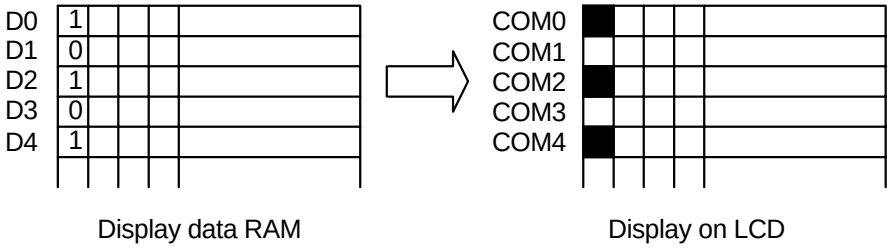


Figure 3.

Relationship between display data RAM and address (if initial display line is 21H)

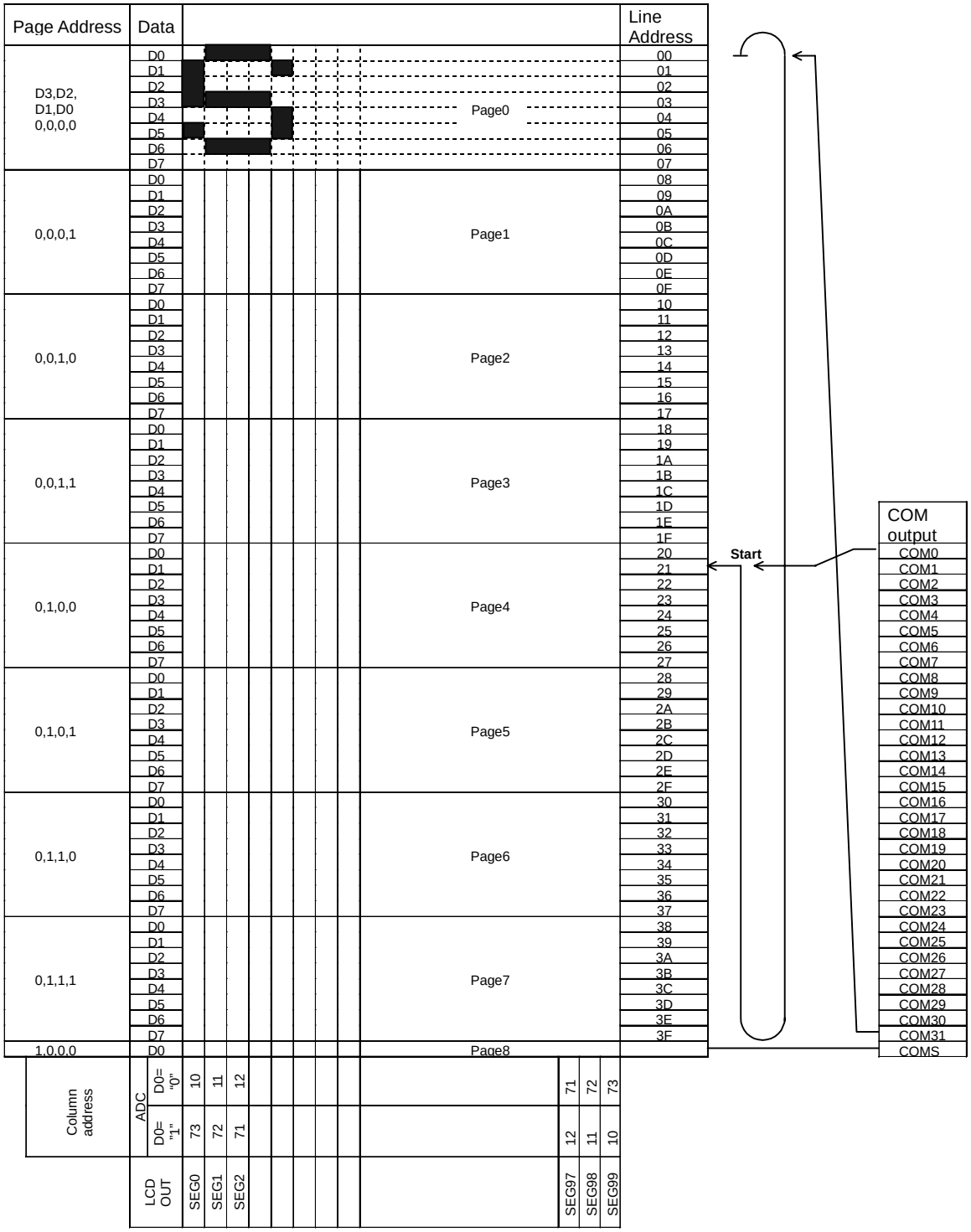


Figure 4.

Display Timing Generator

This section explains how the display timing generator circuit operates.

Signal Generation to Line Counter and Display Data Latch Circuit

The display clock (CL) generates a clock to the line counter and a latch signal to the display data latch circuit.
The line address of the display RAM is generated in synchronization with the display clock. 100-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pad.
The display data is read to the LCD drive circuit completely independent of access to the display data RAM from the microprocessor.

LCD AC Signal (FR) Generation

The display clock generates an LCD AC signal (FR). The FR causes the LCD drive circuit to generate a AC drive waveform.
It generates a 2-frame AC drive waveform.
When the NT7501 is operated in slave mode on the assumption of multi-chip, the FR pad and CL pad become input pads.

Common Timing Signal Generation

The display clock generates an internal common timing signal and a start signal (DYO) to the common driver. A display clock resulting from frequency division of an oscillation clock is output from the CL pad.
When an AC signal (FR) is switched, a high pulse is output as a DYO output at the turning edge of the previous display clock.
Refer to Figure 5. The DYO output is output only in master mode.

When the NT7501 is used for multi-chip, the slave requires to receive the FR, CL, $\overline{DOF}$ signals from the master.

Table 4 shows the FR, CL, DYO and $\overline{DOF}$ status.

Table 4.

Model	Operation mode	FR	CL	DYO	$\overline{DOF}$
NT7501	Master	Output	Output	Output	Output
	Slave	Input	Input	HZ	Input

HZ denotes a high-impedance status

Example of NT7501 1/33 duty (Dual-frame AC driver waveforms)

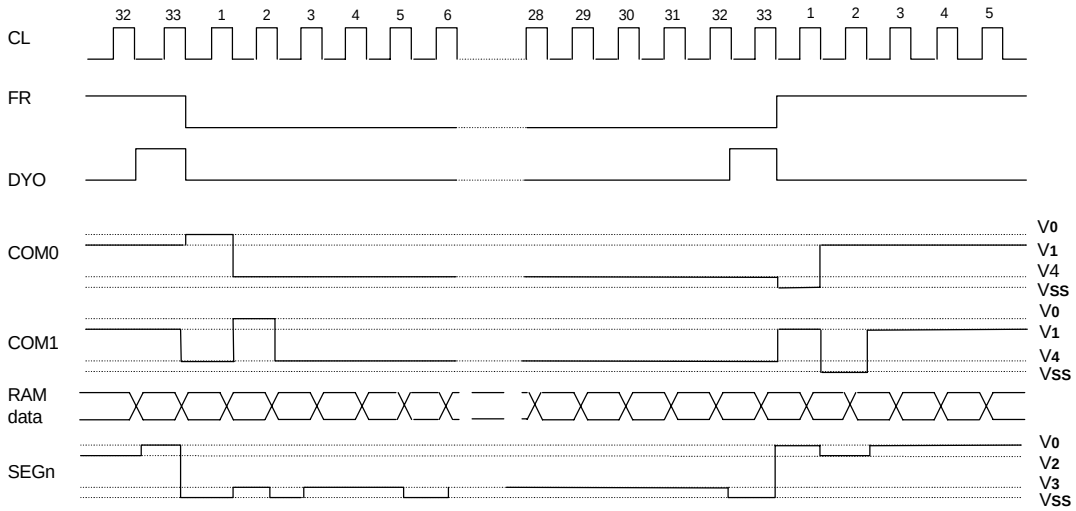


Figure 5.

Display Data Latch Circuit

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display in normal/reverse Display ON/OFF and Entire display on commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 100 segment outputs to generate four-level LCD panel drive signals. The LCD panel drive voltage is generated by a specific combination of display data, a COM scan signal, and a FR signal. Figure 5 gives an example of SEG and COM output waveform.

Oscillator Circuit

This is an oscillator having a complete built-in type CR, and its output is used as the display timing signal source or as the clock for the voltage booster circuit of the LCD power supply.

The oscillator circuit is available in master mode only.

The oscillator signal is divided and output as a display clock at the CL pad.

Power Supply Circuit

The power supply circuit generates voltage to drive the LCD panel at low power consumption, and is available in NT7501 master mode only. The power supply circuit consists of a voltage booster, a voltage regulator and a LCD drive voltage follower.

The power supply circuit built into the NT7501 is set for a small-scale LCD panel and is inappropriate for a large-pixel panel and a large-display-capacity LCD panel using multiple chips. As the large LCD panel has the dropped display quality due to a large load capacity, it must use an external power source.

The power circuit is controlled by the Set Power Control command. This command sets a three-bit data in the Power Control register to select one of eight power circuit functions. The external power supply and part of the internal power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when the voltage booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when the voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when the voltage follower control bit goes high, and D0 turns off when this bit goes low.

[Practical combination examples]

Status 1: To use only the internal power supply

Status 2: To use only the voltage regulator and voltage follower

Status 3: To use only the voltage follower, input the external voltage V_0

Status 4: To use only an external power supply because the internal power supply does not operate

	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
1	1	1	1	ON	ON	ON	-	Used	Used
2	0	1	1	OFF	ON	ON	VOUT	OPEN	Used
3	0	0	1	OFF	OFF	ON	V0	OPEN	OPEN
4	0	0	0	OFF	OFF	OFF	V0 to V4	OPEN	OPEN

* The voltage booster terminals are CAP1+, CAP1-, CAP2+, CAP2- and CAP3+
* Combinations other than those shown in the above table are possible but impractical.

Booster Circuit

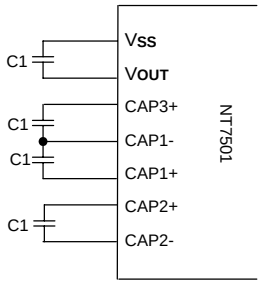
If capacitors C1 are connected between CAP1+ and CAP1-, CAP2+ and CAP2-, or between CAP1- and CAP3+ and between V_{SS} and V_{OUT}, the potential between V_{DD} and V_{SS} is boosted by four times toward the positive side and it is output at V_{OUT}.

For triple boosting, remove only the capacitor between CAP1- and CAP3+ from the connection of the quadruple boosting operation and then short between CAP3- and V_{OUT}. The triple boosted voltage appears at V_{OUT} (CAP3+).

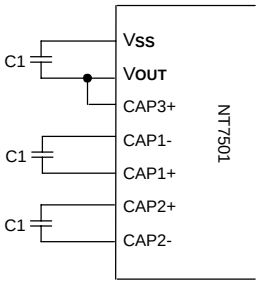
For double boosting, remove only capacitor C1 between CAP2+ and CAP2- from the connection of triple boosting operation, open CAP2- and short between CAP2+, CAP3+ and VOUT. The double boosted voltage is output at VOUT (CAP3+, CAP2+).

For quadruple boosting, set a V_{DD} voltage range so that the voltage at V_{OUT} may not exceed the absolute maximum rating.

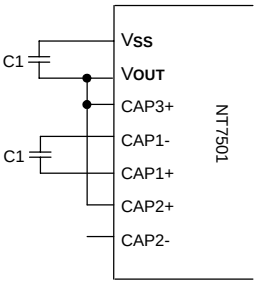
As the booster circuit uses signals from the oscillator circuit, the oscillator circuit must be operative.



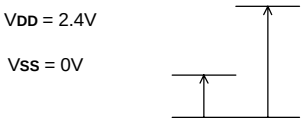
4x step-up voltage circuit



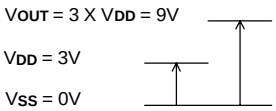
3x step-up voltage circuit



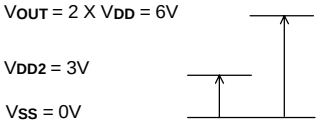
2x step-up voltage circuit



4x step-up voltage relationships



3x step-up voltage relationships



2x step-up voltage relationships

Voltage Regulator Circuit

The function of the internal voltage regulator circuits is to determine the liquid crystal operating voltage V_0, by adjusting resistors R_a and R_b, within the range $V_0 < V_{OUT}$. VOUT is the operating voltage of the operational amplifier circuits shown in Figure 6.

Feedback gain control for initial LCD voltage. External resistors are connected between V_0 and V_R, and between V_R and V_{SS} and these resistors are chosen to give the desired V_0 according to the following equation:

$V_0 = (1 + R_b/R_a) \times V_{REG} + R_b \times I_{ref}$

TPS1	TPS0	Thermal Gradient (% / °C)	VREG (V)
0	0	-0.05 (Internal V_{REG} used)	2.2
0	1	-0.2 (Internal V_{REG} used)	2.45
1	0	0	V_{DD}
1	1	0	V_{DD}

Voltage Regulator Using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of the LCD screen by electronic control command.

Software controls the 32 voltage levels of V_0. This yields the following equation:

$V_0 = (1+ R_b/R_a) \times V_{REG} + R_b \times I_{ref}$

Where I_{ref} = 0 to 6.5μA ± 40% depending on the 5-bit data set by the electronic control command.

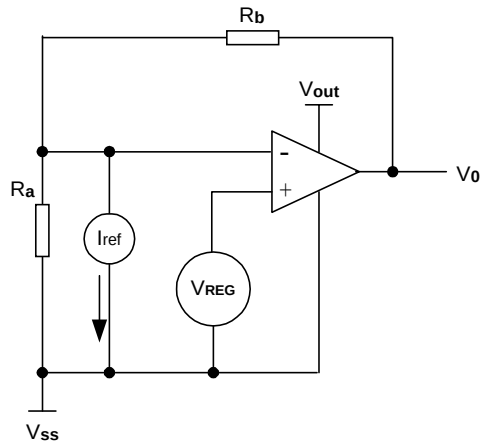


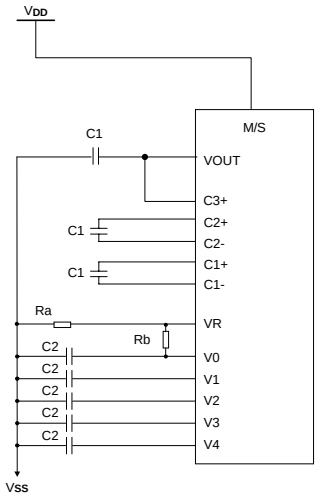
Figure 6.

Reference Power Supply Circuit for Driving LCD Panel

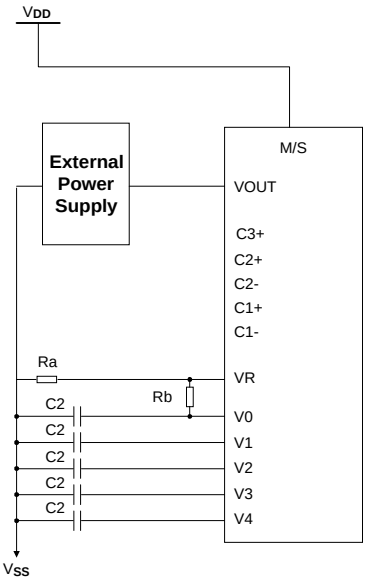
-When using all LCD power circuits

(Voltage converter regulator and follower)

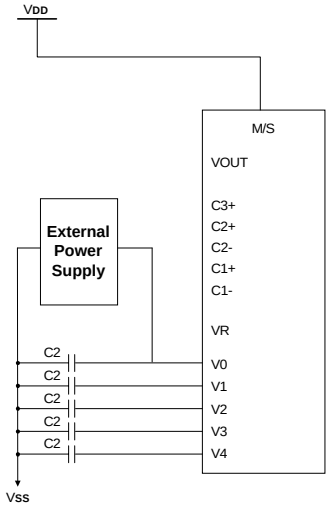
(In case of 3X boosting circuit)



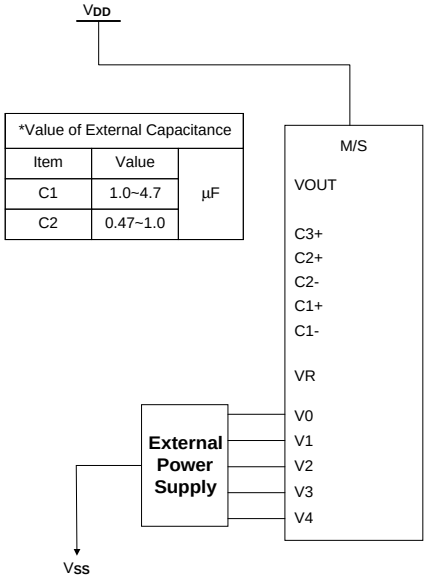
-When not using voltage booster circuits



When only using voltage follower



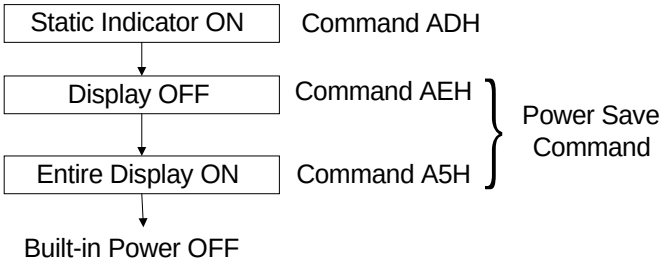
When not using the internal LCD power supply circuits



*Value of External Capacitance		
Item	Value	
C1	1.0~4.7	µF
C2	0.47~1.0	

Command Sequence when Built-in Power Supply is Turned OFF

To turn off the built-in power supply, follow the command sequence as shown below after setting the system to standby mode.



Reset Circuit

When the $\overline{RES}$ input goes low, this LSI is initialized.

Initialized status

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = low)
4. Read modify write OFF
5. Power control register (D2, D1, D0) = (0, 0, 0,)
6. Register data clear in serial interface
7. LCD power supply bias ratio 1/6
8. Static indicator: OFF
9. Display start line register set at line 1
10. Column address counter set at address0
11. Page address register set at page 0
12. Output status register (D3) = (0)
13. Electronic control register set at 0
14. Test command OFF

As seen in Figure 8 Microprocessor Interface (Reference Example). Connect the $\overline{RES}$ pad to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the NT7501 does not use the internal LCD power supply circuit, the $\overline{RES}$ must be low when the external LCD power supply is turned on.

When $\overline{RES}$ goes low, each register is cleared and set to the above initialized status. However, it has no effect on the oscillator circuit and output pads (FR, CL, DYO, D0 to D7)

The initialization by $\overline{RES}$ pad signal is always required during power-on. If the control signal from the MPU is HZ, an overcurrent may flow through the IC. A protection is required to prevent the HZ signal at the input pads during power-on.

Be sure to initialize it by $\overline{RES}$ pad when turning on the power supply. When the reset command is used, only parameters 8 to 14 in the above initialization are executed.

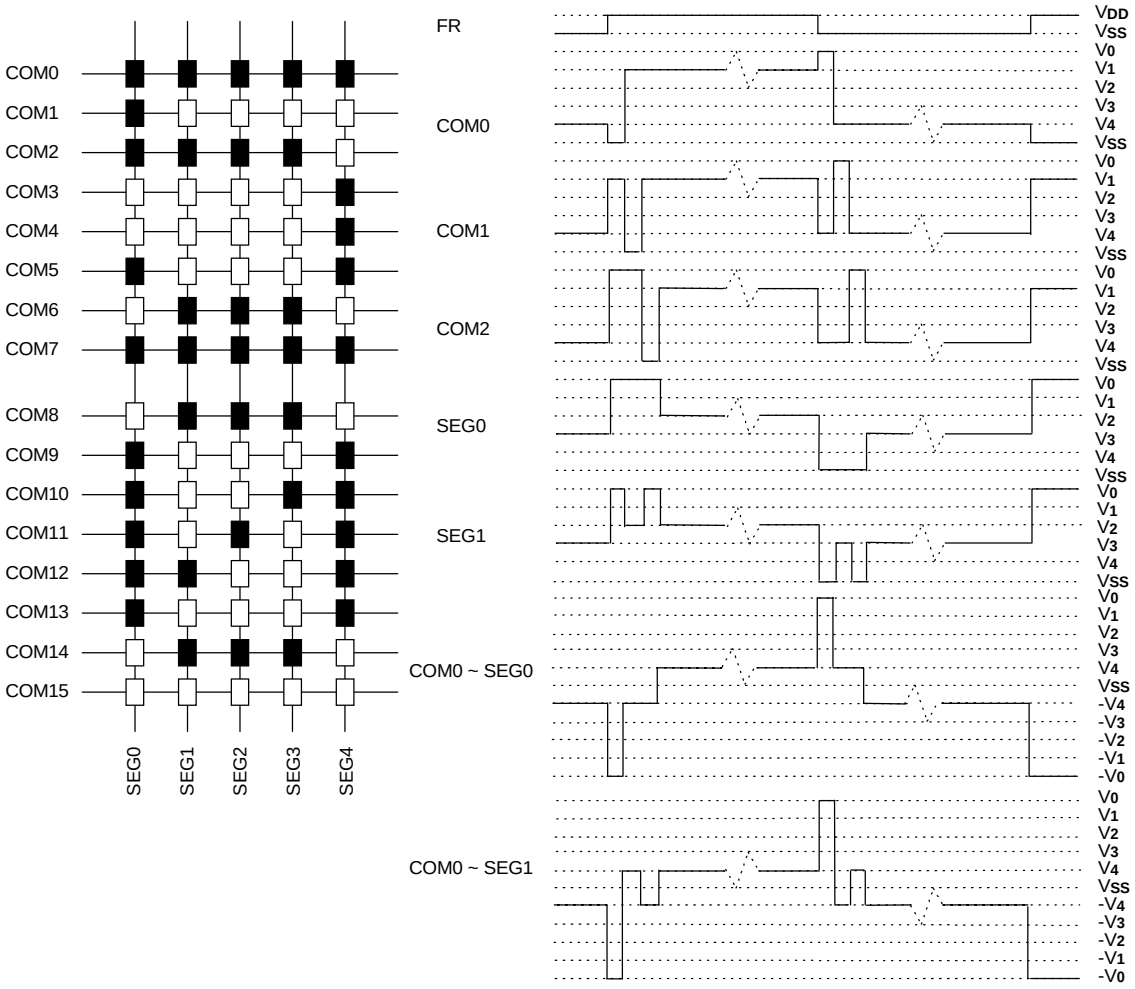

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
SEG0
SEG1
SEG2
SEG3
SEG4
FR
COM0
COM1
COM2
SEG0
SEG1
COM0 ~ SEG0
COM0 ~ SEG1
VDD
VSS
V0
V1
V2
V3
V4
-V4
-V3
-V2
-V1
-V0

Figure 7.

COMMANDS

The NT7501 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ ($R/\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using the internal timing clock only, (regardless of external clock) its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters read status when a low pulse is input to the $\overline{RD}$ pad and write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters read status when a high pulse is input to the $R/\overline{W}$ pad and write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(high) when the 6800 series microprocessor interface reads the status of display data. This is an only different point from the 8080 series microprocessor interface.

Looking at the 8080 series, microprocessor interface example commands are explained below.

When the serial interface is selected, input data in sequence starting from D7.

Command Set

1. Display ON/OFF

   Alternatively turns the display on and off.

A0	E / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

   The display turns off when D goes low and it turns on when D goes high.

2. Set Display Start Line

   Specifies the line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

Specifies the page address where to load display RAM data in the page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator and only D0 is valid for data change.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

4. Set Column Address

Specifies the column address of the display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them in succession. When the microprocessor repeatedly access the display RAM, the column address counter is incremented during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7501 is busy due to either internal operation or being reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and the column address “100-n” corresponds to segment driver n. When high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When it goes low the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates that initialization is in progress due to $\overline{RES}$ signal or by reset command. When low, the display is on. When high, the chip is being reset.

6. Write Display Data

Write 8-bit data in the display RAM. As the column address is incremented by 1 automatically after each writing, the microprocessor can continue to write data of multiple words.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7. Read Display Data

Reads 8-bit data from the display RAM area specified by the column address and page address. As the column address is incremented by 1 automatically after each reading, the microprocessor can continue to read data of multiple words. A single dummy reading is required immediately after the column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8. ADC Select

Changes the relationship between the RAM column address and the segment driver. The order of the segment driver output pads can be reversed by the software. This allows flexible IC layout during the LCD module assembly. For details, refer to the column address section of Figure4. When display data is written or read, the column address is incremented by 1 as shown in Figure4.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction)
When D is high, the left rotation (reverse direction)

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)
When D is high, the RAM data is low, being LCD ON potential (reverse display)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the Entire display ON status is provided. If the Entire Display ON command is executed during the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

11. Set LCD Bias

Selects a bias ratio for the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

The potential V0 is resistively divided inside the IC to produce potentials V1, V2, V3 and V4 which are necessary to drive the LCD. The bias ratio can be selected using the LCD bias setting command.
Moreover, the potentials V1, V2, V3 and V4 are converted in the impedance and supplied to the LCD drive circuit.

Duty	Bias ratio of LCD power supply
1/33	1/5 bias or 1/6 bias

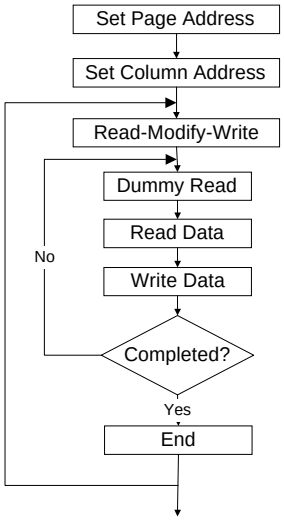
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once a Read-Modify-Write is issued, the column address is not incremental by the Read Display Data command but incremented by the Write Display Data command only. It continues until the End command is issued. When the End command is issued, the column address returns to the address before the Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

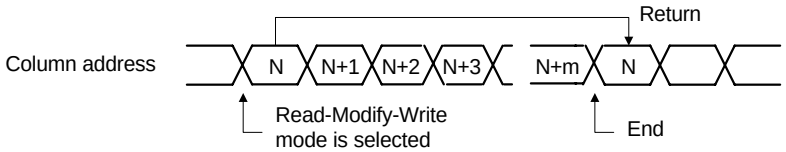
Cursor display sequence



13. End

Cancels the Read-Modify-Write mode and returns the column address to the original address (when Read-Modify-Write was issued.)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



14. Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect the contents of the display RAM. Refer to the Reset circuit section of FUNCTION DESCRIPTION.

A0	E / $\overline{RD}$	R/W / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize the LCD power supply. Only the Reset signal to the $\overline{RES}$ pad can initialize the supply.

15. Output Status Select Register

Applicable to the NT7501. When D is high or low, the scan direction of the COM output pad is selectable. Refer to the Output Status Selector Circuit in the FUNCTION DESCRIPTION for details.

A0	E / $\overline{RD}$	R/W / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D : Selects the scan direction of COM output pad
D = 0: Normal (COM0 → COM31) D = 1: Reverse (COM31 → COM0)
*: Invalid bit

16. Set Power Control

Selects one of eight power circuit functions using a 3-bit register. An external power supply and part of the on-chip power circuit can be used simultaneously. Refer to the Power Supply Circuit section of the FUNCTION DESCRIPTION for details.

A0	E / $\overline{RD}$	R/W / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, the voltage follower turns off. When A0 goes high, it turns on
When A1 goes low, the voltage regulator turns off. When A1 goes high, it turns on
When A2 goes low, the voltage booster turns off. When A2 goes high, it turns on

17. Set Electronic Control

Adjusts the contrast of the LCD panel display by changing the V0 LCD drive voltage that is output by the voltage regulator of the on-board power supply.
This command selects one of the 32 V0 LCD drive voltages by storing data in the 5-bit register. The V0 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator section of the FUNCTION DESCRIPTION for details.

A0	E / $\overline{RD}$	R/W / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	I V0 I
0	0	0	0	0	LOW
0	0	0	0	1	
0	0	0	1	0	
		:			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4, D3, D2, D1, D1, D0) = (0, 0, 0, 0, 0) to suppress the electronic control function.

18. Static Indicator

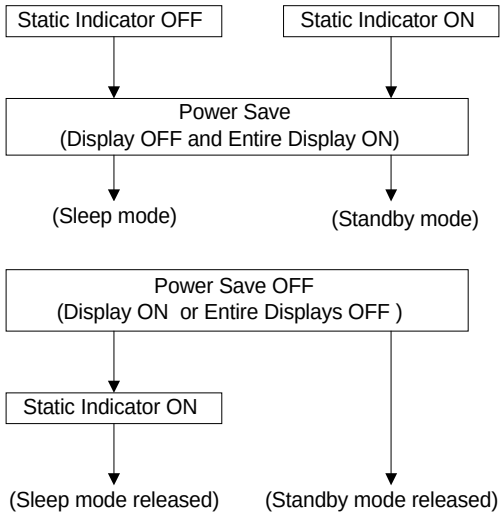
This command turns on or off the static drive indicators. The indicator display is controlled by this command only, and it is not affected by the other display control commands.
Either the FR or FRS terminal is connected to either of the static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on, the static drive operates and the indicator blinks at an interval of approximately one second. This pattern separation between indicator electrodes and dynamic drive electrodes is recommended. A closer pattern may cause a LCD and electrode deterioration.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D 0: Static indicator OFF
1: Static indicator ON

19. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.
Release the Sleep mode using the Power Save OFF command (Display ON command or Entire Display OFF command).



Sleep mode
This mode stops every operation of the LCD display system, and can reduce current consumption to a nearly static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:
(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the V**ss** level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access the built-in display RAM.

Standby mode
Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.
The ON operation of the static drive system indicates that the NT7501 is in the standby mode. The internal status in the standby mode is as follows:
(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the V**ss** level as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.
When the RESET command is issued in the standby mode, the sleep mode is set.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to the floating or Vss level, prior to, or concurrently with causing the NT7501 to go into the sleep mode or standby mode.
When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to the floating or Vss level, prior to, or concurrently with causing the NT7501 series to go into the sleep mode or standby mode.

20. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued unconsciously, set the $\overline{RES}$ input to low or issue the Reset command to release the test mode.

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

Cautions: The NT7501 holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. Consideration must be given to suppressing the noise on the package and system and to preventing ambient noise. To prevent spike noise, built-in software for periodical status refreshment is recommended.

The test command can be inserted in an unexpected place. Therefore it is recommended the user enter the test mode reset command F0h during the refresh sequence.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	D	Turns on the LCD panel when goes high, and turns it off when goes low
(2) Set Display Start Line	0	1	0	0	1	Display start address						Specifies the RAM display line for COM0
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in the Page Address register
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets the 4 higher bits of column address of the display RAM in register
(5) Set column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets the 4 lower bits of column address of the display RAM in register
(6) Read Status	0	0	1	Status				0	0	0	0	Reads the status information
(7) Write Display Data	1	1	0	Write data								Writes data in the display RAM
(8) Read Display Data	1	0	1	Read data								Reads data from the display RAM
(9) ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets the normal relationship between the RAM column address and the segment driver when low, but reverses the relationship when high
(10) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal display when low, but reverse display when high
(11) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1)
(12) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	D	Sets the LCD drive voltage bias ratio
(13) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments the Column Address counter during each writing when high and during each reading when low
(14) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write
(15) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets the internal functions
(16) Set Output Status Register	0	1	0	1	1	0	0	D	*	*	*	Selects the COM output scan direction. * Invalid data
(17) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode
(18) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets the V0 output voltage to Electronic Control register
(19) Set static indicator On/Off	0	1	0	1	0	1	0	1	1	0	D	Set the static indicator On/Off 0: OFF 1: ON
(20) Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(21) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(22) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

Absolute Maximum Rating*

DC Supply Voltage (V_{DD}) . . . . -0.3V to + 6.0V

DC Supply Voltage (V_{OUT}, V_0) . . . . . -0.3V to + 10.5V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . -40°C to + 85°C

Storage Temperature . . . . -55°C to + 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{SS} = 0V, V_{DD} = 2.4 - 3.5V T_A = -40 to 85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating Voltage	2.4		3.5	V	
		2.4		3.0	V	Triple boosting
		2.4		2.4	V	Quadruple boosting
V_{OUT}	Booster output voltage	6.0		9.0	V	
V_0	Voltage regulator operation voltage	5.0		8.0	V	
V_{REG1}	Reference voltage 1	2.0	2.2	2.4	V	T_A = 25°C, TPS1, TPS0 = 0, 0
V_{REG2}	Reference voltage 2	2.25	2.45	2.65	V	T_A = 25°C, TPS1, TPS0 = 0, 1
I_{DD1}	Dynamic current consumption 1	-	22	35	μA	V_{DD} = 3V, V_0 = 8V, built-in power supply off, display on, display data = checker and no access, T_A = 25°C
I_{DD2}	Dynamic current consumption 2	-	48	80	μA	3X boosting, V_{DD} = 3V, V_0 = 8V, built-in power supply on, display on, display data = checker and no access, T_A = 25°C
I_{SP}	Sleep mode current consumption		0.01	1	μA	During sleep, T_A = 25°C
I_{SB}	Standby mode current consumption		10	20	μA	During standby, T_A = 25°C
V_{IHC}	High-level input voltage	0.8 X V_{DD}		V_{DD}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CSI}$, CS2, FR, M/S, C86, P/S and $\overline{DOF}$
V_{ILC}	Low-level input voltage	V_{SS}		0.2 X V_{DD}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CSI}$, CS2, FR, M/S, C86, P/S and $\overline{DOF}$
V_{OHC}	High-level output voltage	0.8 X V_{DD}		V_{DD}	V	I_{OH} = -0.5mA (D0 – D7, FR, FRS, DYO, $\overline{DOF}$ and CL)
V_{OLC}	Low -level output voltage	V_{SS}		0.2 X V_{DD}		I_{OL} = 0.5mA (D0 – D7, FR, FRS, DYO, $\overline{DOF}$ and CL)
V_{IHS}	High-level input voltage	0.85 X V_{DD}		V_{DD}	V	Schmitt trigger input (CL, SCL(D6), TPS0, TPS1 and $\overline{RES}$)
V_{ILS}	Low-level input voltage	V_{SS}		0.15 X V_{DD}	V	Schmitt trigger input (CL, SCL(D6), TPS0, TPS1 and $\overline{RES}$)

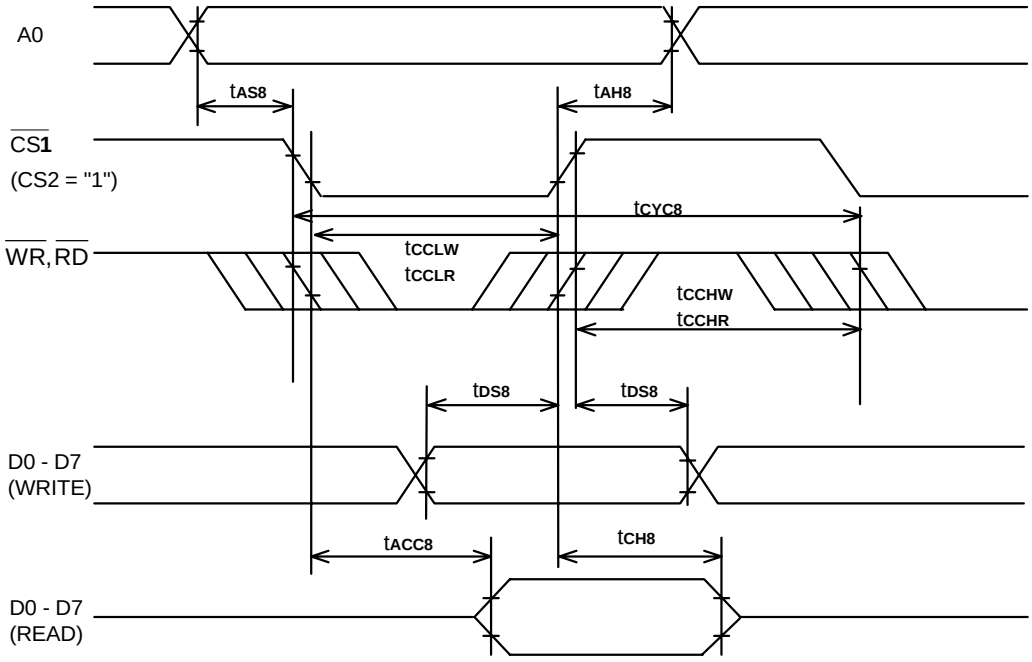
DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
I_{LI}	Input leakage current	-1.0		1.0	μA	V_{IN}=V_{DD} or V_{SS} (A0, $\overline{RD}$ (E), $\overline{WR}$ (R / $\overline{W}$), $\overline{CSI}$, CS2, M/S, C86, P/S, TPS0, TPS1 and $\overline{RES}$)	
I_{HZ}	HZ leakage current	-3.0		3.0	μA	When the D0 - D7, FR, CL, DYO and $\overline{DOF}$ are in high impedance	
R_{ON}	LCD driver ON resistance		3.0	4.5	kΩ	V_0 = 8.0V	T_A = 25°C, These are the resistance values for when 0.1V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, V4)
C_{IN}	Input pad capacity		5.0	8.0	pF	T_A = 25°C, f = 1MHz	
f_{OSC}	Oscillation frequency	18	22	26	kHZ	T_A = 25°C, V_{DD} = 3.0V	

Notes: 1. Voltages $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{ss}$ must always be satisfied.

AC Characteristics

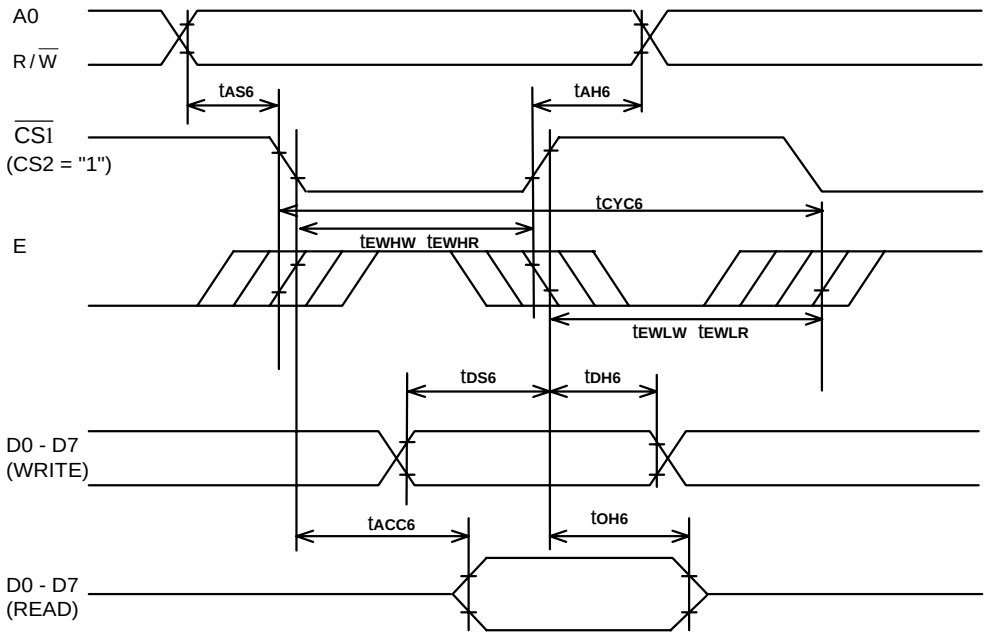
(1) System Buses



(V_{DD} = 2.4 - 3.5V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0			ns	
T_{AS8}	Address setup time	0			ns	
T_{CYC8}	System cycle time	400			ns	
T_{CCLW}	Control L pulse width (WR)	55			ns	
T_{CCLR}	Control L pulse width (RD)	125			ns	
T_{CCHW}	Control H pulse width (WR)	180			ns	
T_{CCHR}	Control H pulse width (RD)	130			ns	
T_{DS8}	Data setup time	35			ns	
T_{DH8}	Data hold time	13			ns	
T_{ACC8}	$\overline{RD}$ access time			125	ns	C_L = 100pF
T_{CH8}	Output disable time	10		90	ns	C_L = 100pF

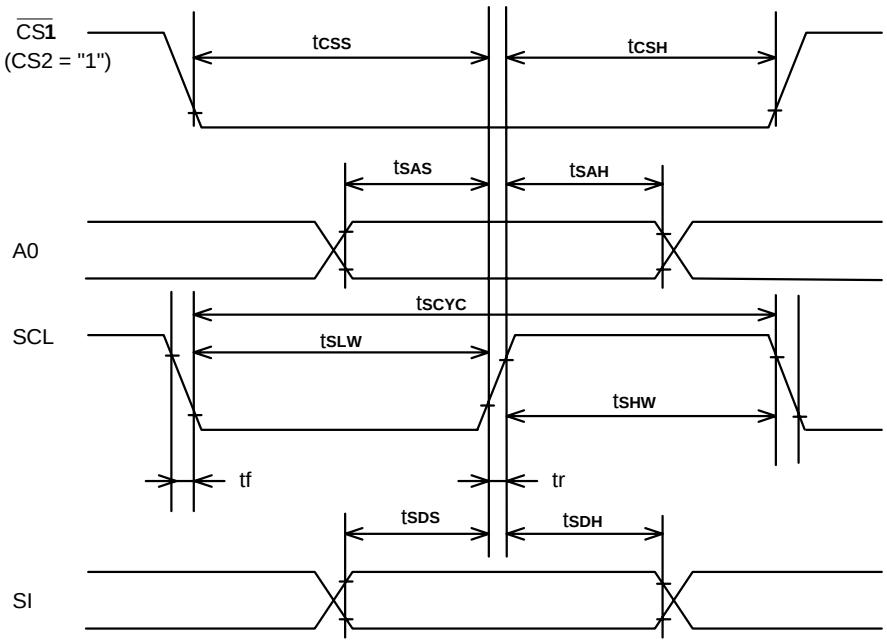
(2) System Buses



(V_{DD} = 2.4 - 3.5V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC6}	System cycle time	400			nS	
T_{AS6}	Address setup time	0			nS	
T_{AH6}	Address hold time	0			nS	
T_{DS6}	Data setup time	35			nS	
T_{DH6}	Data hold time	13			nS	
T_{OH6}	Output disable time	10		90	nS	C_L = 100pF
T_{ACC6}	Access time			125	nS	C_L = 100pF
T_{EWLR}	Enable Low pulse width	125			nS	
T_{EWLW}		55			nS	
T_{EWHR}	Enable high pulse width	125			nS	
T_{EWHW}		180			nS	

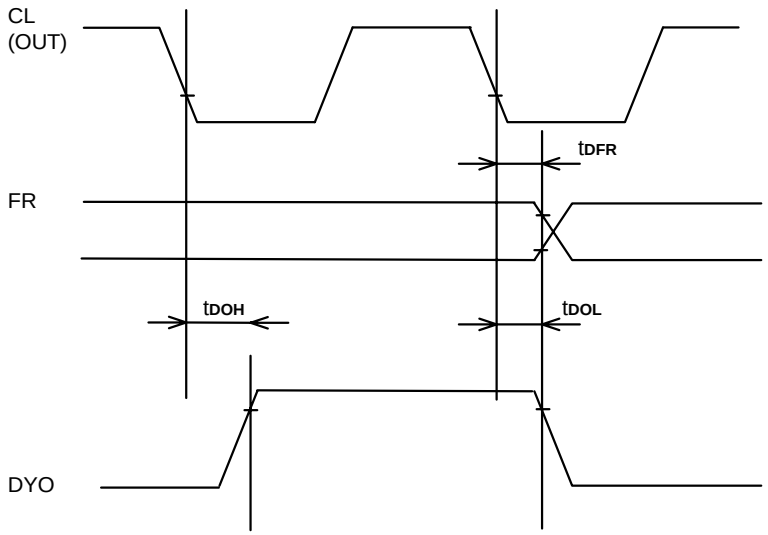
(3) Serial Interface



(V_{DD} = 2.4 - 3.5V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{SCYC}	Serial clock cycle	450			nS	
T_{SHW}	Serial clock H pulse width	180			nS	
T_{SLW}	Serial clock L pulse width	135			nS	
T_{SAS}	Address setup time	90			nS	
T_{SAH}	Address hold time	360			nS	
T_{SDS}	Data setup time	90			nS	
T_{SDH}	Data hold time	90			nS	
T_{CSS}	$\overline{CS1}$ serial clock time	55			nS	
T_{CSH}	$\overline{CS1}$ serial clock time	180			nS	

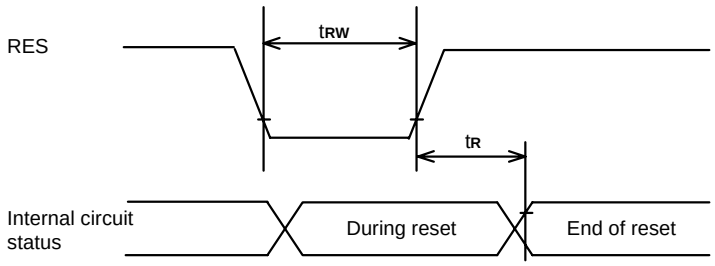
(4) Display Control Timing



(V_{DD} = 2.4 - 3.5V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{DFR}	FR delay time		13	70	nS	C_L = 50pF
T_{DOH}	DYO “H” delay time		55	180	nS	
T_{DOL}	DYO “L” delay time		55	180	nS	

(5) Reset Timing

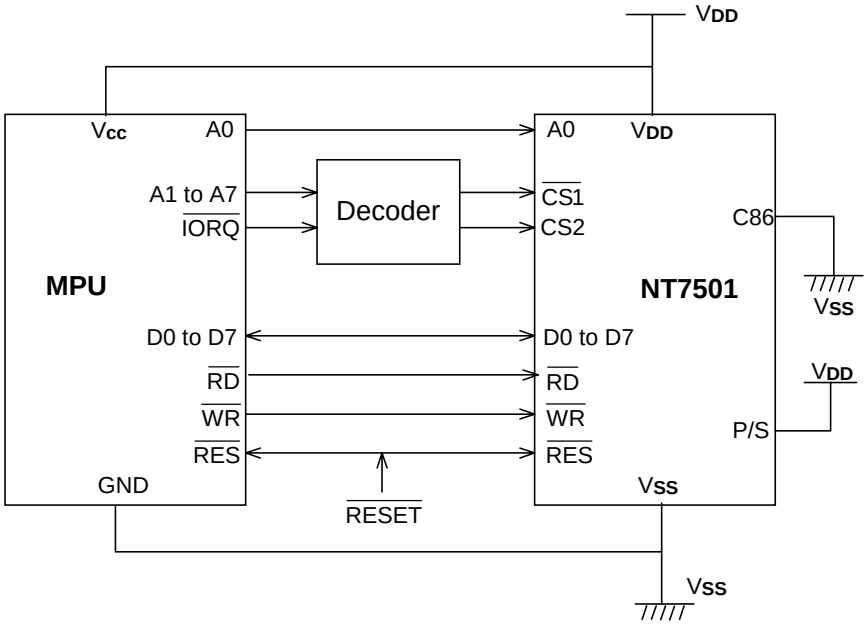


(V_{DD} = 2.4 - 3.5V, T_A = -40 - 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_R	Reset time	1.0			µS	
T_W	Reset low pulse width	1.0			µS	

MICROPROCESSOR INTERFACE (for reference only)

8080-series Microprocessors



6800-series Microprocessors

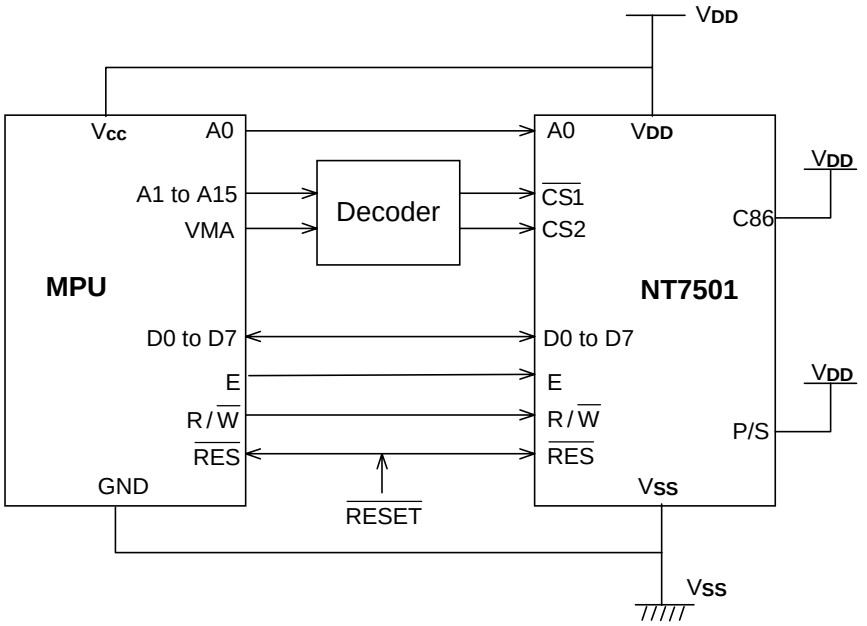
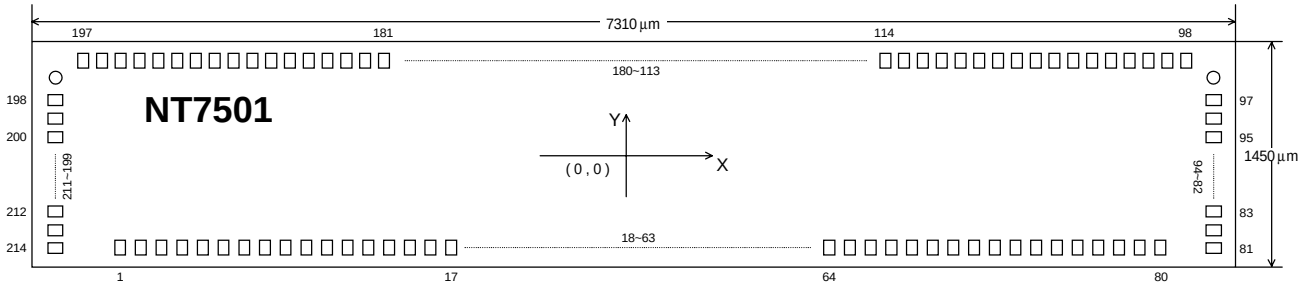


Figure 8

Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	FRS	-3357.5	-655	31	D4	-807.5	-655
2	FR	-3272.5	-655	32	D5	-722.5	-655
3	DYO	-3187.5	-655	33	D6	-637.5	-655
4	CL	-3102.5	-655	34	D7	-552.5	-655
5	$\overline{DOF}$	-3017.5	-655	35	V_{SS}	-467.5	-655
6	V_{S1}	-2932.5	-655	36	V_{SS}	-382.5	-655
7	M/S	-2847.5	-655	37	V_{SS}	-297.5	-655
8	$\overline{RES}$	-2762.5	-655	38	V_{SS}	-212.5	-655
9	V_{SS}	-2677.5	-655	39	V_{SS}	-127.5	-655
10	P/S	-2592.5	-655	40	V_{SS}	-42.5	-655
11	$\overline{CS1}$	-2507.5	-655	41	V_{SS}	42.5	-655
12	V_{DD}	-2422.5	-655	42	V_{SS}	127.5	-655
13	CS2	-2337.5	-655	43	V_{OUT}	212.5	-655
14	C86	-2252.5	-655	44	V_{OUT}	297.5	-655
15	V_{SS}	-2167.5	-655	45	CAP3+	382.5	-655
16	A0	-2082.5	-655	46	CAP3+	467.5	-655
17	$\overline{WR}$	-1997.5	-655	47	CAP1-	552.5	-655
18	$\overline{RD}$	-1912.5	-655	48	CAP1-	637.5	-655
19	V_{DD}	-1827.5	-655	49	CAP1+	722.5	-655
20	V_{DD}	-1742.5	-655	50	CAP1+	807.5	-655
21	V_{DD}	-1657.5	-655	51	CAP2-	892.5	-655
22	V_{DD}	-1572.5	-655	52	CAP2-	977.5	-655
23	V_{DD}	-1487.5	-655	53	CAP2+	1062.5	-655
24	V_{DD}	-1402.5	-655	54	CAP2+	1147.5	-655
25	V_{DD}	-1317.5	-655	55	V_0	1232.5	-655
26	V_{DD}	-1232.5	-655	56	V_0	1317.5	-655
27	D0	-1147.5	-655	57	V_R	1402.5	-655
28	D1	-1062.5	-655	58	V_R	1487.5	-655
29	D2	-977.5	-655	59	V_{SS}	1572.5	-655
30	D3	-892.5	-655	60	V_{SS}	1657.5	-655

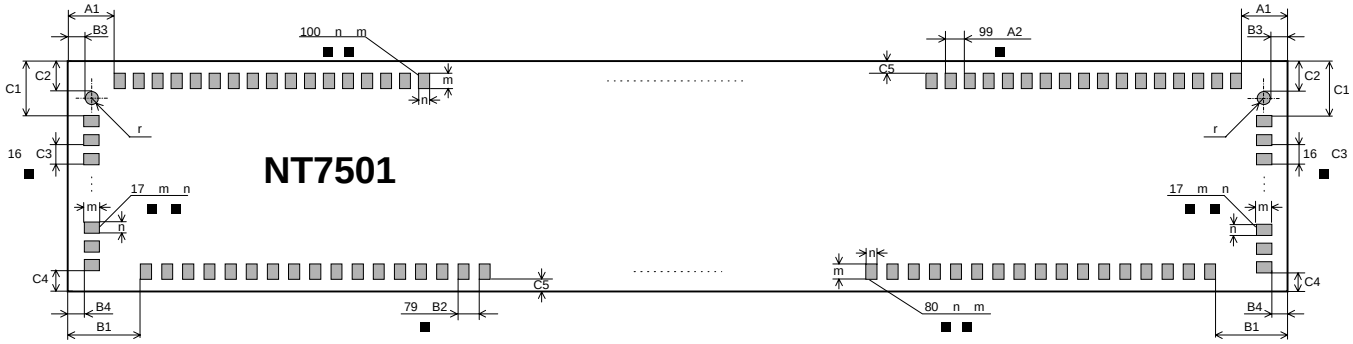
Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	V_{DD}	1742.5	-655	101	SEG3	3255	655
62	V_{DD}	1827.5	-655	102	SEG4	3185	655
63	V_0	1912.5	-655	103	SEG5	3115	655
64	V_0	1997.5	-655	104	SEG6	3045	655
65	V_1	2082.5	-655	105	SEG7	2975	655
66	V_1	2167.5	-655	106	SEG8	2905	655
67	V_2	2252.5	-655	107	SEG9	2835	655
68	V_2	2337.5	-655	108	SEG10	2765	655
69	V_3	2422.5	-655	109	SEG11	2695	655
70	V_3	2507.5	-655	110	SEG12	2625	655
71	V_4	2592.5	-655	111	SEG13	2555	655
72	V_4	2677.5	-655	112	SEG14	2485	655
73	V_{SS}	2762.5	-655	113	SEG15	2415	655
74	V_{SS}	2847.5	-655	114	SEG16	2345	655
75	TPS0	2932.5	-655	115	SEG17	2275	655
76	TPS1	3017.5	-655	116	SEG18	2205	655
77	V_{DD}	3102.5	-655	117	SEG19	2135	655
78	OP1	3187.5	-655	118	SEG20	2065	655
79	OP2	3272.5	-655	119	SEG21	1995	655
80	OP3	3357.5	-655	120	SEG22	1925	655
81	COM15	3590	-648.1	121	SEG23	1855	655
82	COM14	3590	-578.1	122	SEG24	1785	655
83	COM13	3590	-508.1	123	SEG25	1715	655
84	COM12	3590	-438.1	124	SEG26	1645	655
85	COM11	3590	-368.1	125	SEG27	1575	655
86	COM10	3590	-298.1	126	SEG28	1505	655
87	COM9	3590	-228.1	127	SEG29	1435	655
88	COM8	3590	-158.1	128	SEG30	1365	655
89	COM7	3590	-88.1	129	SEG31	1295	655
90	COM6	3590	-18.1	130	SEG32	1225	655
91	COM5	3590	51.9	131	SEG33	1155	655
92	COM4	3590	121.9	132	SEG34	1085	655
93	COM3	3590	191.9	133	SEG35	1015	655
94	COM2	3590	261.9	134	SEG36	945	655
95	COM1	3590	331.9	135	SEG37	875	655
96	COM0	3590	401.9	136	SEG38	805	655
97	COMS	3590	471.9	137	SEG39	735	655
98	SEG0	3465	655	139	SEG40	665	655
99	SEG1	3395	655	139	SEG41	595	655
100	SEG2	3325	655	140	SEG42	525	655

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	SEG43	455	655	179	SEG81	-2205	655
142	SEG44	385	655	180	SEG82	-2275	655
143	SEG45	315	655	181	SEG83	-2345	655
144	SEG46	245	655	182	SEG84	-2415	655
145	SEG47	175	655	183	SEG85	-2485	655
146	SEG48	105	655	184	SEG86	-2555	655
147	SEG49	35	655	185	SEG87	-2625	655
148	SEG50	-35	655	186	SEG88	-2695	655
149	SEG51	-105	655	187	SEG89	-2765	655
150	SEG52	-175	655	188	SEG90	-2835	655
151	SEG53	-245	655	189	SEG91	-2905	655
152	SEG54	-315	655	190	SEG92	-2975	655
153	SEG55	-385	655	191	SEG93	-3045	655
154	SEG56	-455	655	192	SEG94	-3115	655
155	SEG57	-525	655	193	SEG95	-3185	655
156	SEG58	-595	655	194	SEG96	-3255	655
157	SEG59	-665	655	195	SEG97	-3325	655
158	SEG60	-735	655	196	SEG98	-3395	655
159	SEG61	-805	655	197	SEG99	-3465	655
160	SEG62	-875	655	198	COM16	-3590	471.9
161	SEG63	-945	655	199	COM17	-3590	401.9
162	SEG64	-1015	655	200	COM18	-3590	331.9
163	SEG65	-1085	655	201	COM19	-3590	261.9
164	SEG66	-1155	655	202	COM20	-3590	191.9
165	SEG67	-1225	655	203	COM21	-3590	121.9
166	SEG68	-1295	655	204	COM22	-3590	51.9
167	SEG69	-1365	655	205	COM23	-3590	-18.1
168	SEG70	-1435	655	206	COM24	-3590	-88.1
169	SEG71	-1505	655	207	COM25	-3590	-158.1
170	SEG72	-1575	655	208	COM26	-3590	-228.1
171	SEG73	-1645	655	209	COM27	-3590	-298.1
172	SEG74	-1715	655	210	COM28	-3590	-368.1
173	SEG75	-1785	655	211	COM29	-3590	-438.1
174	SEG76	-1855	655	212	COM30	-3590	-508.1
175	SEG77	-1925	655	213	COM31	-3590	-578.1
176	SEG78	-1995	655	214	COMS	-3590	-648.1
177	SEG79	-2065	655				
178	SEG80	-2135	655				

Package Information



Chip Outline Dimensions

unit:µm

Symbol	Dimensions in µm	Symbol	Dimensions in µm
A1	169	B1	276.5
A2	70	B2	85
C1	232.1	B3	30
C2	120	B4	20
C3	70	m	90
C4	55.9	n	42
C5	25	r	35

Ordering Information

Part No.	Package
NT7501H-BDT	Au bump on chip tray