



# DATA SHEET

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O K I G a A s P R O D U C T S

## **KGL4217/KGL4221/KGL4222** **10-Gbps GaAs Optical Communications Family**

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**November 1999**



**Oki Semiconductor**

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## KGL4217/KGL4221/KGL4222

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### 10-Gbps GaAs Optical Communications Family Products

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#### INTRODUCTION

Oki Semiconductor's 10-Gbps GaAs Optical Communications Family Products include the KGL4217 Limiting Amplifier, KGL4221 16:1 Multiplexer IC, and KGL4222 1:16 Demultiplexer IC. These 10-Gbps optical devices are manufactured using Oki Semiconductor's 0.2- $\mu\text{m}$  gate length GaAs MESFET process.

The KGL4217 Limiting Amplifier provides high-speed operation, high-sensitivity, low power dissipation, and is mounted in a 24-pin ceramic package. The KGL4217 is used in high-speed optical communication environments operating with a maximum clock frequency of over 10 GHz.

The KGL4221 Mux and KGL4222 Demux feature high-speed operation and low power dissipation, and they are mounted in a 48-pin package. These ICs that provide high-speed conversion of parallel-to-serial (demux) or serial-to-parallel (mux) data streams operating with a maximum clock frequency of over 10 GHz.

#### GENERAL FEATURES

- High-speed operation: 10-Gbps data rate (min)
- Low-power dissipation
- 0.2- $\mu\text{m}$  gate length GaAs MESFET process
- KGL4217 Limiting Amplifier: 24-pin ceramic package
- KGL4221 Mux and KGL4222 Demux: 48-pin ceramic package  
Compatible with low-speed interfaces  
Oki's unique MCFF and CBFF technology

#### APPLICATION

- High-speed optical communication systems: 10 Gbps
- High-speed test equipment: KGL4221 16:1 (Mux) and KGL4222 16:1 (Demux)



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## KGL4217

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### 10-Gbps GaAs Limiting Amplifier

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#### Introduction

Oki Semiconductor's KGL4217 Limiting Amplifier IC is designed for 10-Gbps digital communications systems. This high speed, low-power Limiting Amplifier IC uses 0.2- $\mu\text{m}$  gate length GaAs MESFET and DCFL (Direct Coupled FET Logic) technologies. The KGL4217 is available as a 24-pin ceramic packaged device. The high sensitivity of the KGL4217 requires capacitive coupling for input and output signal interfaces.

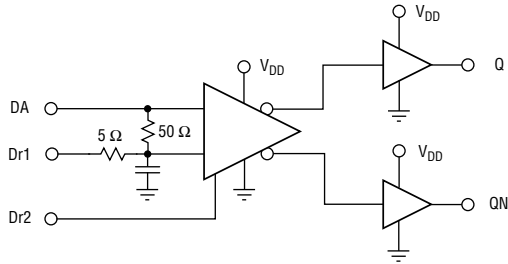
#### FEATURES

- High-speed operation: 10-Gbps data rate (min)
- High sensitivity: 50 to 600 mV<sub>PP</sub> (at 10 Gbps  $2^{23}$  -1 PRPS, capacitive coupling)
- Low-power dissipation: 250 mW (typ.) using 2-V power-supply
- 0.2- $\mu\text{m}$  gate length GaAs MESFET process
- DCFL (Direct Coupled FET Logic) technology
- 24-pin ceramic package

#### APPLICATION

- High-speed optical communication systems: 10 Gbps

## BLOCK DIAGRAM



Logic Symbol	Description
DA	Data input terminal
DR1	Terminal to connect external capacitors
DR2	Adjustment terminal for input signal threshold
Q, QN	Complimentary data outputs
VDD	Power supply

## ABSOLUTE MAXIMUM RATINGS

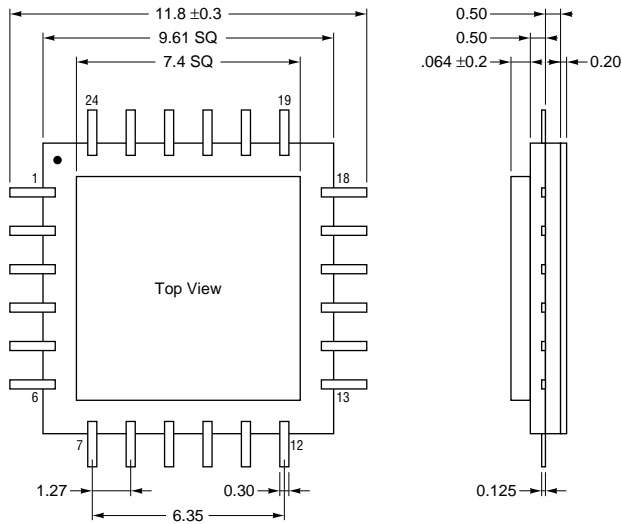
Description	Symbol	Min	Max	Units
Supply Voltage	VDD	- 0.3	2.3	V
Applied Voltage at DA, DR1	VD1	- 0.3	1.5	V
Bias Voltage at DR2	VR1	- 2.5	2.5	V
Temperature at Package Base Under Bias	T <sub>S</sub>	- 45	100	°C
Storage Temperature	T <sub>ST</sub>	- 45	125	°C

## ELECTRICAL CHARACTERISTICS

VDD = 2 V ± 0.1 V, T<sub>S</sub> = 0°C to 70°C

Description	Symbol	Min	Typ	Max	Units
Operating Data Rate Range	DAR	-	10	-	Gbps
Power Dissipation	PW	-	0.25	0.35	W
Data Input Voltage Swing	VI	0.05	-	0.6	V
Data Output Voltage Swing	VO	0.4	0.6	0.8	V

## PACKAGE OUTLINE



Dimension in mm.

## PIN CONFIGURATION

Pin No	Signal	Pin Definition
1	GND	Ground
2	QN	Data output (neg)
3	GND	Ground
4	GND	Ground
5	Q	Data output (pos)
6	GND	Ground
7	GND	Ground
8	DR2	Input threshold adjustment
9	GND	Ground
10	DR1	External capacitance
11	DR1	External capacitance
12	DR1	External capacitance

Pin No	Signal	Pin Definition
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	DA	Data input
18	GND	Ground
19	VDD	Power supply
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	VDD	Power supply
24	GND	Ground



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## KGL4221

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### 10-Gbps GaAs 16:1 Multiplexer Integrated Circuit

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#### INTRODUCTION

Oki Semiconductor's KGL4221 is an 10-Gbps GaAs 16:1 multiplexer IC that converts 16-bit parallel data into a single, serial data stream operating with a maximum clock frequency of over 10 GHz. The high-speed KGL4221 is manufactured using Oki's 0.2- $\mu\text{m}$  gate length GaAs MESFET process, and is mounted in a 48-pin package. By using Oki's unique MCFF (Memory Cell Flip Flop) and CBFF (Common-gate Bias Flip Flop) technology, the KGL4221 provides high-speed operation and low power dissipation. External capacitive coupling is required for clock input and data output connections. Low speed signal interfaces are compatible with ECL.

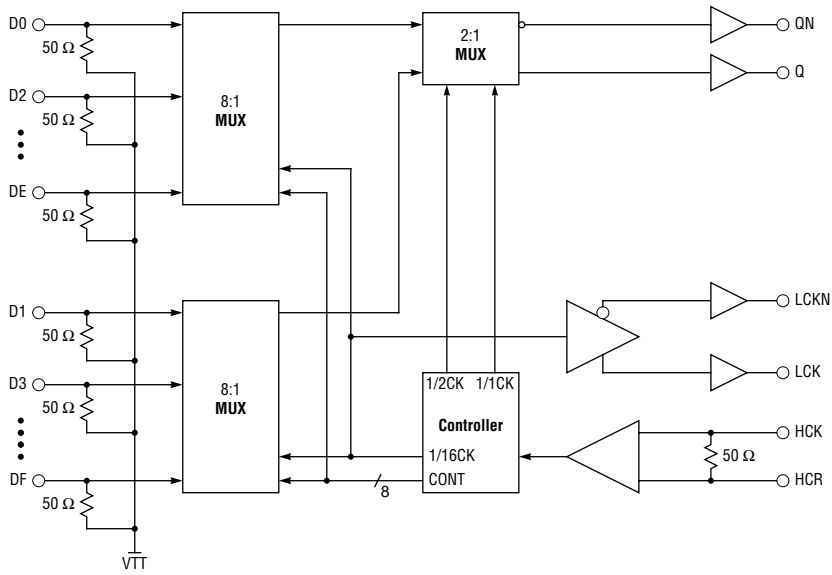
#### FEATURES

- High-speed operation: 10-Gbps data rate (max)
- Low power dissipation: 3 W (typ.) using - 2 V power supply
- 0.2- $\mu\text{m}$  gate length GaAs MESFET process
- 48-pin ceramic package
- Compatible with low-speed interfaces

#### APPLICATION

- High-speed optical communication systems: 10 Gbps
- High-speed test equipment

## BLOCK DIAGRAM



Logic Symbol	Description
D0 - DF	Data Inputs
HCK	Clock Input
HCR	Reference Clock Input
Q, QN	Complimentary Data Outputs
LCK, LCKN	Complimentary 1/16 Clock Outputs
VTT	Power Supply and Termination Supply

## ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Min	Max	Units
Supply Voltage	V <sub>TT</sub>	- 2.3	0.3	V
Clock and Data Input Voltage	V <sub>CDI</sub>	- 2.3	- 0.5	V
Temperature at Package Base Under Bias	T <sub>S</sub>	- 45	100	°C
Storage Temperature	T <sub>ST</sub>	- 45	125	°C

## ELECTRICAL CHARACTERISTICS

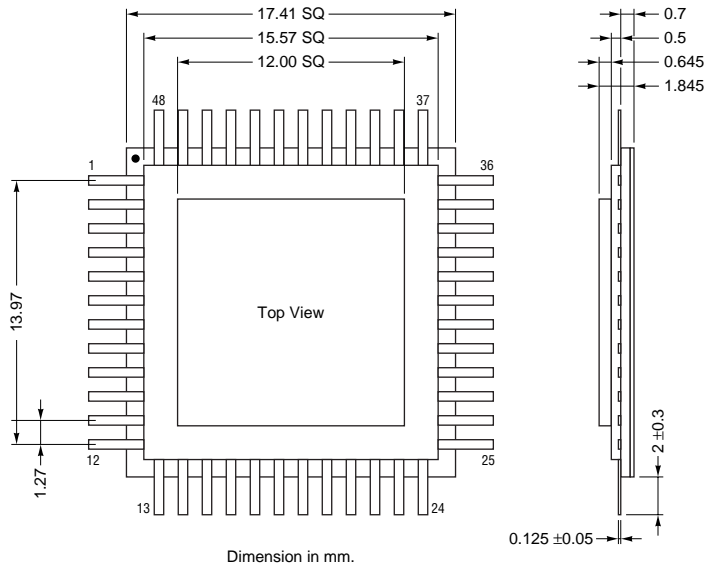
V<sub>TT</sub> = - 2 V ± 0.1 V, T<sub>S</sub> = 0°C to 70°C

Description	Symbol	Min	Typ	Max	Units
Maximum Clock Frequency	CKF	10	-	-	GHz
Power Dissipation	PW	-	3	-	W
Clock Input Voltage Swing (HCK) (see note 1)	V <sub>CKI</sub>	0.5	0.7	0.9	V <sub>PP</sub>
Low Level of Data Input (DO - DF)	V <sub>DIL</sub>	- 2.0	- 1.6	1.47	V
High Level of Data Input (DO - DF)	V <sub>DIH</sub>	- 1.16	- 1.1	- 0.65	V
Data Output Voltage Swing (Q, QN) (see note 1)	V <sub>DO</sub>	0.7	0.95	1.2	V <sub>PP</sub>
Low Level of 1/16 Clock Output (LCK, LCKN) (see note 2)	V <sub>COL</sub>	- 2.0	- 1.8	- 1.62	V
High Level of 1/16 Clock Output (LCK, LCKN) (see note 2)	V <sub>COH</sub>	- 1.03	- 0.93	- 0.75	V

### NOTES:

- External Capacitive Coupling
- Externally terminated to -2 V by 50-Ω load.

## PACKAGE OUTLINE



## PIN CONFIGURATION

Pin No	Signal	Pin Definition
1	G	Ground
2	LCKN	1/16 clock (neg)
3	G	Ground
4	LCKN	1/16 clock (pos)
5	G	Ground
6	VTT	Power supply
7	VTT	Power supply
8	G	Ground
9	Q	Data output (pos)
10	G	Ground
11	QN	Data output (neg)
12	G	Ground
13	VTT	Power supply
14	D0	Data input 0
15	D2	Data input 2
16	D4	Data input 4

Pin No	Signal	Pin Definition
17	D6	Data input 6
18	G	Ground
19	VTT	Power supply
20	D8	Data input 8
21	DA	Data input A
22	DC	Data input C
23	DE	Data input E
24	VTT	Power supply
25	G	Ground
26	HCR	Clock reference bias
27	G	Ground
28	HCK	Clock input
29	G	Ground
30	VTT	Power supply
31	VTT	Power supply
32	G	Ground

Pin No	Signal	Pin Definition
33	G	Ground
34	G	Ground
35	G	Ground
36	G	Ground
37	VTT	Power supply
38	DF	Data input F
39	DD	Data input D
40	DB	Data input B
41	D9	Data input 9
42	G	Ground
43	VTT	Power supply
44	D7	Data input 7
45	D5	Data input 5
46	D3	Data input 3
47	D1	Data input 1
48	VTT	Power supply

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## KGL4222

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### 10-Gbps GaAs 1:16 Demultiplexer Integrated Circuit

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#### INTRODUCTION

Oki Semiconductor's KGL4222 is an 10-Gbps GaAs 1:16 demultiplexer IC that converts a single, serial data stream into 16-bit parallel data operating with a maximum clock frequency of over 10 GHz. The high-speed KGL4222 is manufactured using Oki's 0.2- $\mu\text{m}$  gate length GaAs MESFET process, and is mounted in a 48-pin package. By using Oki's unique MCFF (Memory Cell Flip Flop) and CBFF (Common-gate Bias Flip Flop) technology, the KGL4222 provides high-speed operation and low power dissipation. External capacitive coupling is required for clock input and data output connections. Low speed signal interfaces are compatible with ECL.

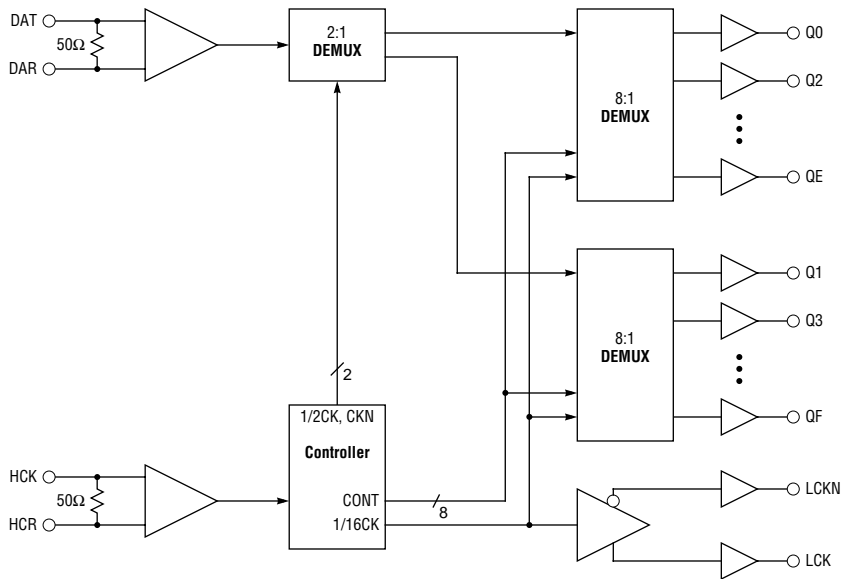
#### FEATURES

- High-speed operation: 10-Gbps data rate
- Low power dissipation: 2.4W (typ.) using - 2 V power supply
- 0.2- $\mu\text{m}$  gate length GaAs MESFET process
- 48-pin ceramic package
- Compatible with low-speed interfaces

#### APPLICATION

- 10-Gbps digital communication systems
- High-speed test equipment

## BLOCK DIAGRAM



Logic Symbol	Description
Q0 - QF	Data Outputs
HCK	Clock Input
HCR	Reference of Clock Input
DAT	Data Input
DAR	Reference of Clock Input
LCK, LCKN	Complimentary 1/16 Clock Outputs
VTT	Power Supply and Termination Supply

## ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Min	Max	Units
Supply Voltage	V <sub>TT</sub>	- 2.3	0.3	V
Clock and Data Input Voltage	V <sub>CDI</sub>	- 2.3	- 0.5	V
Temperature at Package Base Under Bias	T <sub>S</sub>	- 45	100	°C
Storage Temperature	T <sub>ST</sub>	- 45	125	°C

## ELECTRICAL CHARACTERISTICS

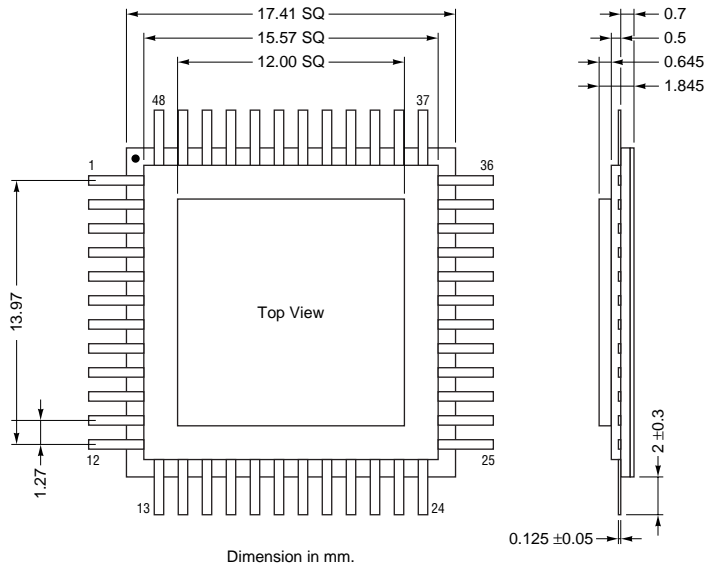
V<sub>TT</sub> = - 2 V ± 0.1 V, T<sub>S</sub> = 0°C to 70°C

Description	Symbol	Min	Typ	Max	Units
Maximum Clock Frequency	CKF	10	-	-	GHz
Power Dissipation	PW	-	2.4	2.8	W
Clock Input Voltage Swing (HCK) (see note 1)	V <sub>CKI</sub>	0.5	0.7	0.9	V <sub>PP</sub>
Data Input Voltage Swing (DAT) (see note 1)	V <sub>DI</sub>	0.5	0.7	0.9	V <sub>PP</sub>
Low Level of Data Output (Q0 - QF) (see note 2)	V <sub>DOL</sub>	- 2.0	- 1.8	- 1.62	V
High Level of Data Output (Q0 - QF) (see note 2)	V <sub>DOH</sub>	- 1.03	- 0.93	- 0.75	V
Low Level of 1/16 Clock Output (LCK, LCKN) (see note 2)	V <sub>COL</sub>	- 2.0	- 1.8	- 1.62	V
High Level of 1/16 Clock Output (LCK, LCKN) (see note 2)	V <sub>COH</sub>	- 1.03	- 0.93	- 0.75	V

NOTES:

1. External Capacitive Coupling.
2. Externally terminated to -2 V by 50-Ω load.

## PACKAGE OUTLINE



## PIN CONFIGURATION

Pin No	Signal	Pin Definition
1	G	Ground
2	LCKN	1/16 clock (neg)
3	G	Ground
4	LCKN	1/16 clock (pos)
5	G	Ground
6	VTT	Power supply
7	VTT	Power supply
8	G	Ground
9	DAT	Data input
10	G	Ground
11	DAR	Data reference bias
12	G	Ground
13	VTT	Power supply
14	Q1	Data output 1
15	Q3	Data output 3
16	Q5	Data output 5

Pin No	Signal	Pin Definition
17	Q7	Data input 7
18	G	Ground
19	VTT	Power supply
20	Q9	Data input 9
21	QB	Data input B
22	QD	Data input D
23	QF	Data input F
24	VTT	Power supply
25	G	Ground
26	HCR	Clock reference bias
27	G	Ground
28	HCK	Clock input
29	G	Ground
30	VTT	Power supply
31	VTT	Power supply
32	G	Ground

Pin No	Signal	Pin Definition
33	G	Ground
34	G	Ground
35	G	Ground
36	G	Ground
37	VTT	Power supply
38	QE	Data input E
39	QC	Data input C
40	QA	Data output A
41	Q8	Data output 8
42	G	Ground
43	VTT	Power supply
44	Q6	Data output 6
45	Q4	Data output 4
46	Q2	Data output 2
47	Q0	Data output 0
48	VTT	Power supply



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