OKI Semiconductor

This version: May 1999
Previous version: Nov. 1997

MSC1209

42-Bit Vacuum Fluorescent Display Tube Driver with Digital Dimming Function

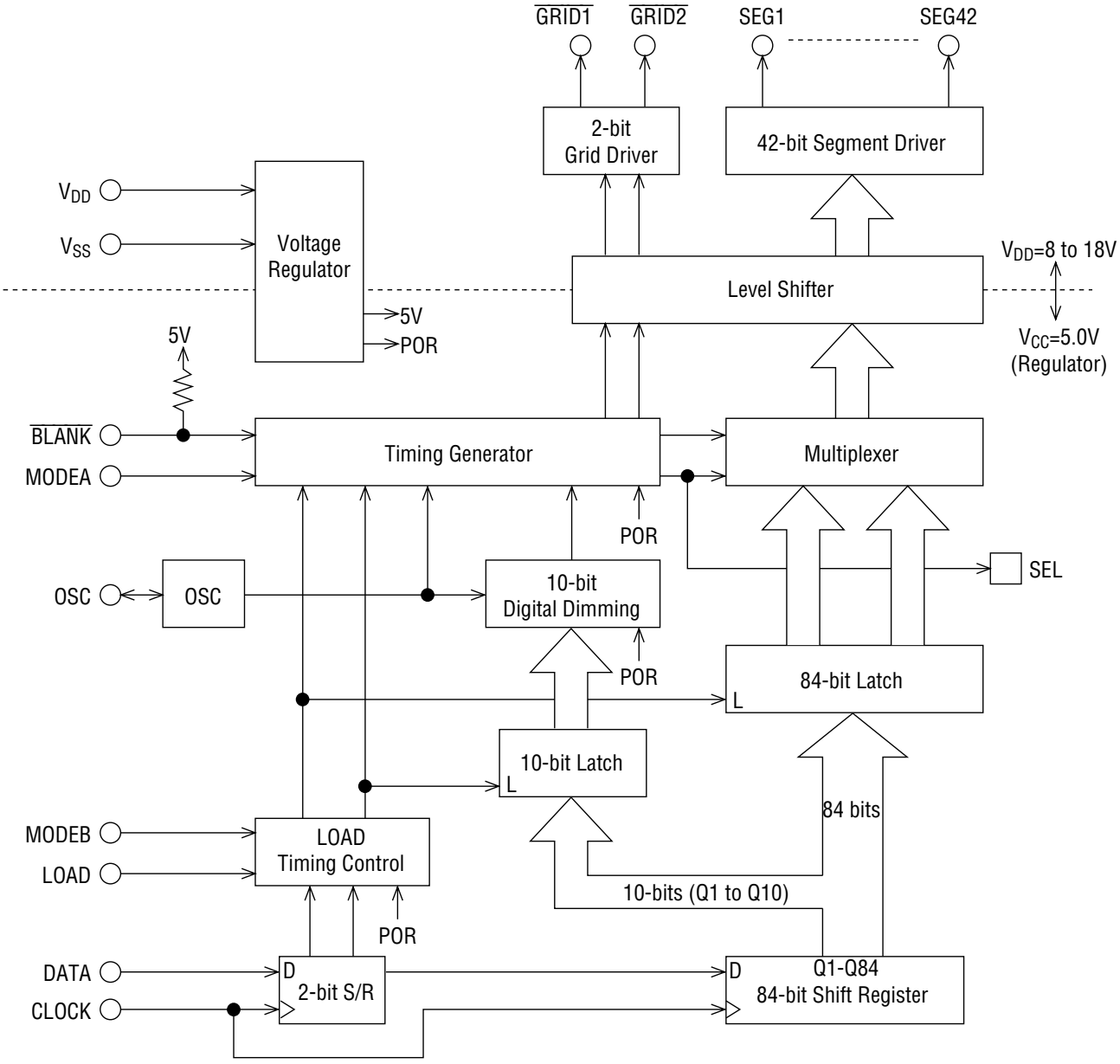
GENERAL DESCRIPTION

The MSC1209 is a Bi-CMOS display driver for a 1/2-duty vacuum fluorescent display tube. The MSC1209 consists of an 84-bit shift register, an 84-bit latch circuit, a 10-bit digital dimming circuit, 42-bit segment drivers, a 2-bit grid circuit, and a cascade control circuit.
The MSC1209 is interfaced with a microcontroller by using three signal lines of LOAD, CLOCK, and DATA. The cascaded MSC1209 ICs can share LOAD, CLOCK, and DATA.

FEATURES

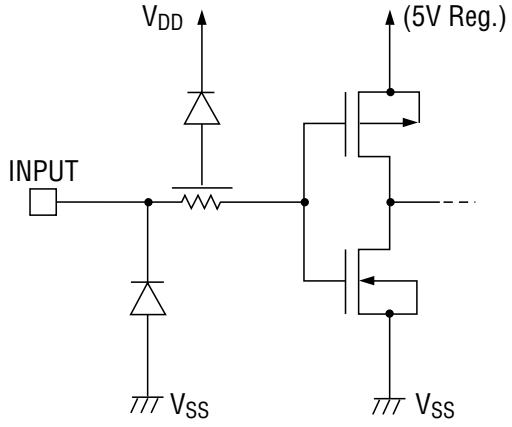
- Power supply voltage: 8V to 18V (Built-in 5V regulator for logic)
- Operating temperature range: –40 to +105°C
- Driving 42 segments directly: $V_{OH}=V_{DD}–0.5V$ at $I_{OH}=–3.0mA$ ($V_{DD}=15.0V$)
- Built-in digital dimming circuit
  10-bit resolution
  Programmable in the duty range of 0/2048 (0%) to 1016.5/2048 (49.6%)
- 3 interfaces with microcontroller: LOAD, CLOCK, DATA
- Cascade connection available
  (The cascaded MSC1209 ICs can share LOAD, CLOCK, and DATA.)
- Built-in oscillation circuit with an external capacitor (a single pin is used)
- Built-in power-on reset circuit
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSC1209GS-2K)

BLOCK DIAGRAM

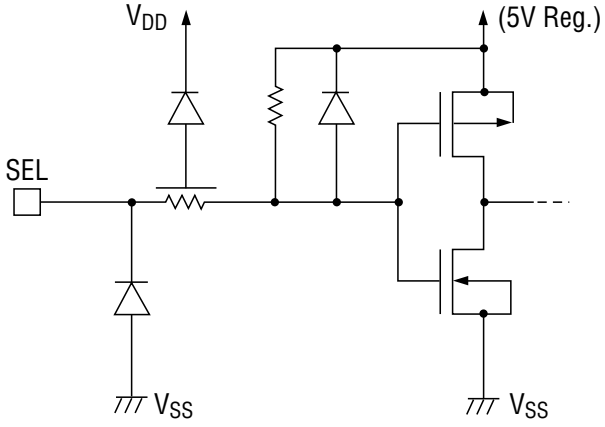


INPUT AND OUTPUT CONFIGURATION

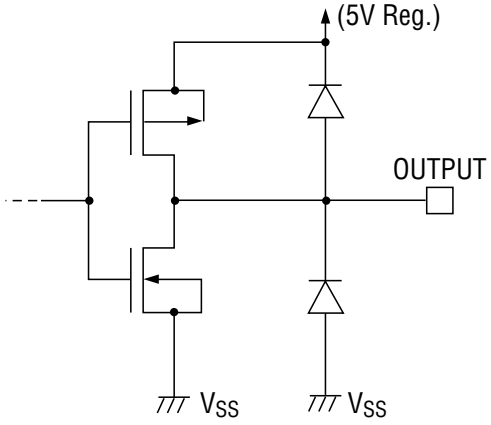
- Schematic Diagram of Logic Portion Input Circuit 1



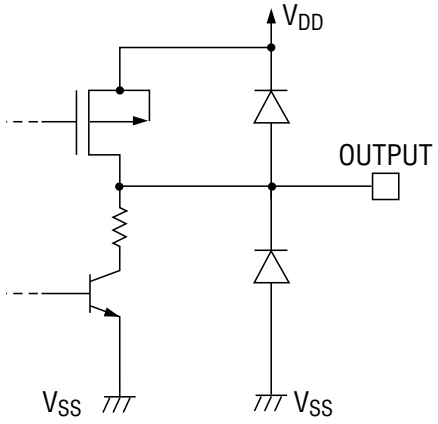
- Schematic Diagram of Logic Portion Input Circuit 2



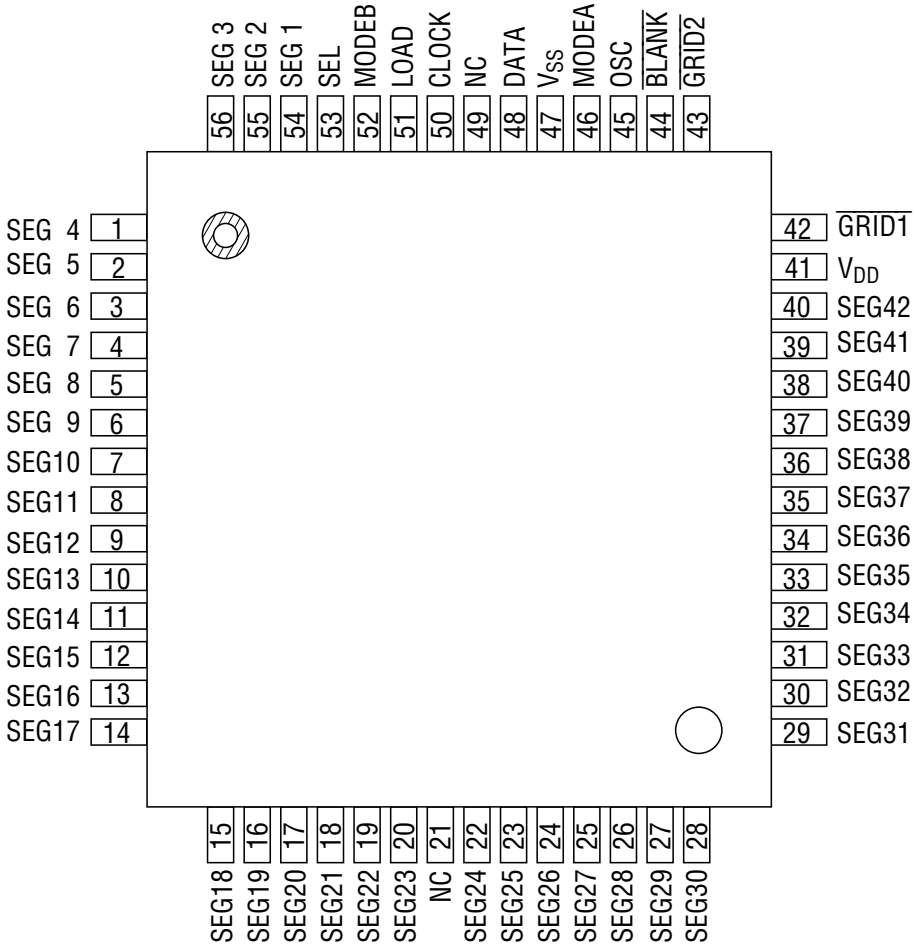
- Schematic Diagram of Logic Portion Output Circuit



- Schematic Diagram of Driver Output Circuit



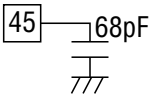
PIN CONFIGURATION (TOP VIEW)



NC: No connection

56-Pin Plastic QFP

PIN DESCRIPTION

Pin	Symbol	Type	Connected to	Description
48	DATA	I	Microcontroller	Serial data input. (Positive logic) Receives display data and dimming data.
50	CLOCK	I	Microcontroller	Shift clock input. Serial data is shifted on the rising edge of this shift clock pulse.
51	LOAD	I	Microcontroller	Load pulse input. The load signal is input when the transfer of serial data is completed.
1 to 20, 22 to 40, 54 to 56	SEG1 to SEG42	O	Anode electrode of VFD tube	Segment driver output.
42	$\overline{\text{GRID1}}$	O	Grid electrode of VFD tube	Grid driver output. When this pin is set to "L", the display goes on. Connect an external PNP transistor to this pin. The segment data of the first bit (S1) to the 42nd bit (S42) is valid in the 84-bit segment data.
43	$\overline{\text{GRID2}}$	O	Grid electrode of VFD tube	Grid driver output. When this pin is set to "L", the display goes on. Connect an external PNP transistor to this pin. The segment data of the 43rd bit (S43) to the 84th bit (S84) is valid in the 84-bit segment data.
44	$\overline{\text{BLANK}}$	I	—	Input with pull-up resistor for display blank. When this pin is set to "L", the display goes off. (SEGn="L")
45	OSC	I/O	—	Input and output for oscillation. Connect an external capacitor of 68pF. The typical value of oscillating frequency is 512kHz. 
46 52	MODEA MODEB	I	—	These pins specify the operating mode.

MODEA	MODEB	Operating Mode
0	0	Master Operation
1	0	Test Mode
0	1	Slave Operation
1	1	Slave Operation

53	SEL	O	MODEA pin at slave side	SEL pin of the master IC outputs switching signals for the segment data that corresponds to the grid signals. The SEL pin of the master IC is connected to the MODEA pin of the slave IC.
41	V_{DD}	—	Power source	Power supply pin (8V to 18V).
47	V_{SS}	—	Power source	GND pin. (Ground)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +20	V
Input Voltage	V_{IN}	All input pins	–0.3 to +6.0	V
Power Dissipation	P_D	Ta≥25°C	257	mW
Storage Temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	8.0	—	18.0	V
"H" Input Voltage	V_{IH}	All input pins other than OSC	3.8	—	5.5	V
"L" Input Voltage	V_{IL}	All input pins other than OSC	–0.3	—	+0.8	V
"H" Driver Output Current	I_{O-1}	V_{DD}=10.8V, 1 driver at the ON state	—	—	–2.2	mA
	I_{O-2}	V_{DD}=10.8V, all drivers at the ON state	—	—	–92.4	mA
CLOCK Frequency	f_C	—	—	—	1.0	MHz
Oscillation Frequency	f_{OSC}	C=68pF	307.2	512	716.8	kHz
Grid Frequency	f_{GRID}	C=68pF	150	250	350	Hz
Operating Temperature	T_{OP}	—	–40	—	+105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

Unless otherwise specified: Ta=–40 to +105°C, V_{DD}=8.0 to 18.0V

Parameter	Symbol	Condition	Min.	Max.	Unit	Applied pin
"H" Input Voltage	V_{IH}	—	3.8	5.5	V	All input pins
"L" Input Voltage	V_{IL}	—	–0.3	+0.8	V	
"H" Input Current	I_{IH1}	V_{DD}=18.0V, V_{IH1}=5.0V	–1.0	+1.0	µA	All input pins other than $\overline{BLANK}$
	I_{IH2}	V_{DD}=18.0V, V_{IH2}=5.0V	–60	+60	µA	$\overline{BLANK}$
"L" Input Current	I_{IL1}	V_{DD}=18.0V, V_{IL1}=0.0V	–1.0	+1.0	µA	All input pins other than $\overline{BLANK}$
	I_{IL2}	V_{DD}=18.0V, V_{IL2}=0.0V	–500	–100	µA	$\overline{BLANK}$
"H" Output Voltage	V_{OH1}	V_{DD}=9.5V, I_{OH1}=–2.0mA	V_{DD}–0.5	—	V	SEG1 to 42
	V_{OH2}	V_{DD}=12.0V, I_{OH2}=–2.5mA	V_{DD}–0.5	—	V	
	V_{OH3}	V_{DD}=15.0V, I_{OH3}=–3.0mA	V_{DD}–0.5	—	V	
	V_{OH4}	V_{DD}=9.5V, I_{OH4}=–0.8mA	V_{DD}–0.5	—	V	
	V_{OH5}	V_{DD}=12.0V, I_{OH5}=–1.0mA	4.0	—	V	SEL
"L" Output Voltage	V_{OL1}	V_{DD}=9.5V, I_{OL1}=500µA	—	4.0	V	SEG1 to 42
	V_{OL2}	V_{DD}=9.5V, I_{OL2}=200µA	—	2.0	V	
	V_{OL3}	V_{DD}=9.5V, I_{OL3}=1.0mA	—	4.0	V	$\overline{GRID1 to 2}$
	V_{OL4}	V_{DD}=9.5V, I_{OL4}=500µA	—	2.0	V	
	V_{OL5}	V_{DD}=9.5V, I_{OL5}=200µA	—	1.0	V	
	V_{OL6}	V_{DD}=12.0V, I_{OL6}=1.0mA	—	1.0	V	SEL
Supply Current	I_{DD}	f_{OSC}=512kHz, no load	—	20	mA	V_{DD}–V_{SS}

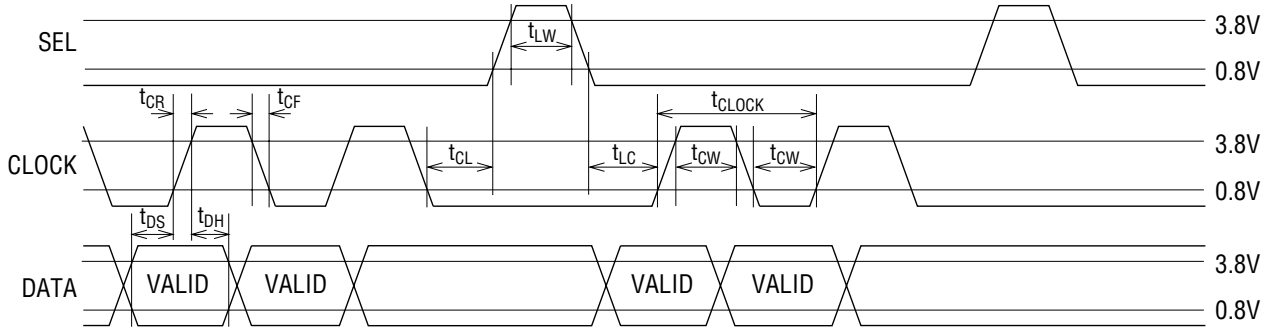
AC Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18V)

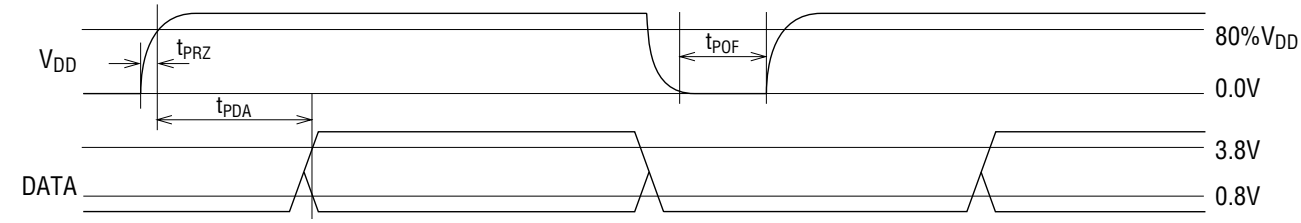
Parameter	Symbol	Condition	Min.	Max.	Unit
CLOCK Frequency	$f_C(1/t_{CLOCK})$	—	—	1.0	MHz
CLOCK Pulse Width	t_{CW}	—	400	—	ns
CLOCK Rise/Fall Time	t_{CR}/t_{CF}	—	—	300	ns
DATA Setup Time	t_{DS}	—	200	—	ns
DATA Hold Time	t_{DH}	—	200	—	ns
CLOCK→ LOAD Time	t_{CL}	—	100	—	ns
LOAD→ CLOCK Time	t_{LC}	—	100	—	ns
LOAD Pulse Width	t_{LW}	—	1.0	—	µs
SEGn Rise/Fall Time	t_R/t_F	C_L=50pF	—	1.0	µs
SEL Rise/Fall Time	t_R/t_F	C_L=50pF	—	1.0	µs
V_{DD}-DATA Input Time at V_{DD} ON	f_{PDA}	When mounted in a unit	300	—	µs
V_{DD}-Hold Time at V_{DD} OFF	f_{PDF}	When mounted in a unit	5.0	—	ms
V_{DD} Rise Time at V_{DD} ON	f_{PR2}	—	—	100	µs

TIMING DIAGRAM

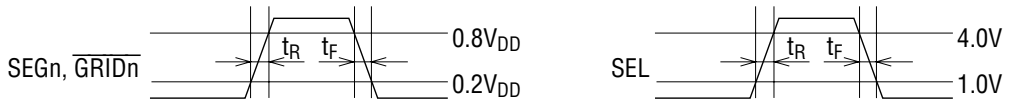
1) Data Timing



2) Reset Timing



3) Output Timing



FUNCTIONAL DESCRIPTION

DATA Input

This device uses 10-bit dimming data (D1 to D10) and 84-bit segment data (S1 to S84). To transfer these data, the mode bits (M0 and M1) must be sent after each of these data succeedingly. The data transfer timing diagram is shown below.

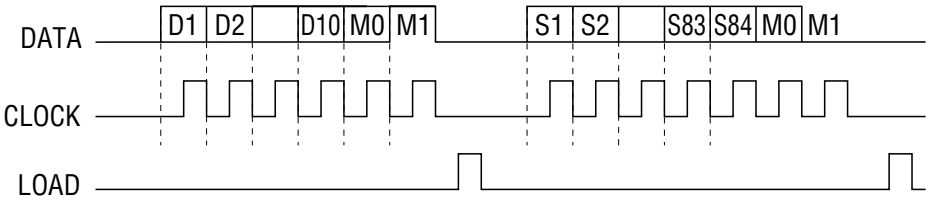


Figure 1 Data Transfer Timing

M0 : Enable bit
M0 = "0": Indicates the data from the master IC.
M0 = "1": Indicates the data from the slave IC.
M1 : Mode specification bit
M1 = "1": Indicates that the data sent on ahead is dimming data.
M1 = "0": Indicates that the data sent on ahead is segment data.
D1 : LSB of dimming data
S1 : data for GRID1 of SEG1
S2 : data for GRID1 of SEG2
:
S42 : data for GRID1 of SEG42
S43 : data for GRID2 of SEG1
:
S84 : data for GRID2 of SEG42

Notes: 1. When the number of input data bits are larger, the data bits are pushed out in the same order that they are input, and 86 bits of the data counted from the bit entered last are used as valid data. (In the case of segment data)
2. When the number of input data bits are smaller, the data remaining in the shift register before data transfer is shifted and used as valid data.

CLOCK Input

Data is shifted at the rising edge of the clock.

LOAD Input

The contents of the shift register are shifted in while the LOAD input is "H" level and latched at "H" to "L" transition. This LOAD signal is regenerated in the VFD tube driver for the latch pulse for dimming data and segment data. When 10-bit dimming data and 84-bit segment data have been transferred, input the LOAD signal prior to the next clock.

Blank Function

Inputting a "L" level to the $\overline{\text{BLANK}}$ pin turns display off (segment output = "L"). At this time, grid outputs are output normally.

Initial Setting

When power is turned on (i.e., when segment data has never been transferred), the display is turned off (segment output = "L"). Display is turned on at the moment when transfer of the segment data is complete. The relationship between the data transfer and display is shown in Figure 2.

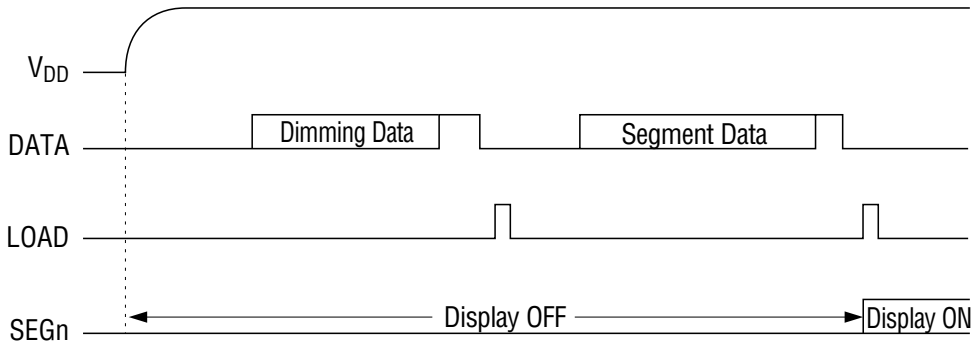


Figure 2 Relationship Between Data Transfer and Display

If, after power-on, the segment data is transferred before the dimming data is transferred, display is turned on at the moment when transfer of the segment data is complete, at which time the dimming value is undefined. The relationship between the data transfer and display is shown in Figure 3.

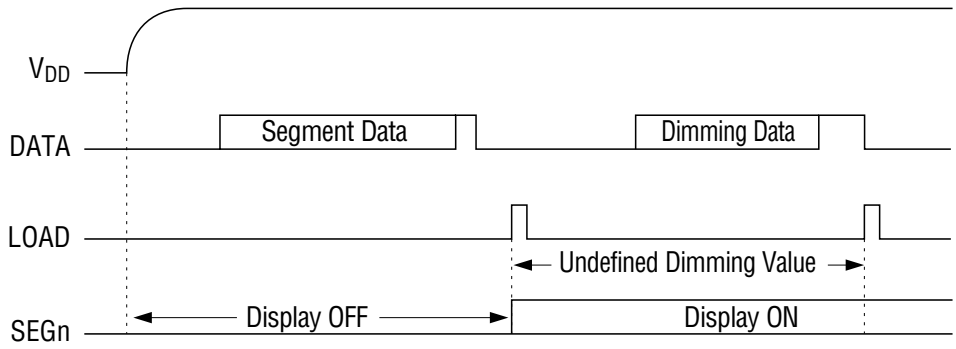


Figure 3 Relationship Between Advanced Transfer of Segment Data and Display

Oscillator

Connect an external capacitor (C), as shown in Figure 4. The oscillating frequency f_{OSC} depends on the external capacitor used. The following equation is true between f_{OSC} and grid frequency (f_{GRID}):

$f_{GRID} = f_{OSC}/2048$

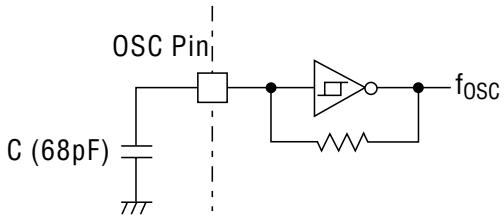


Figure 4 Oscillator Equivalent Circuit

Dimming Function

The duty cycle of grid output can be changed in 1/2048 step with respect to 10-bit dimming data. Table 1 shows the relationship between dimming data and duty ratio.

Table 1 Dimming Data and Duty Ratio

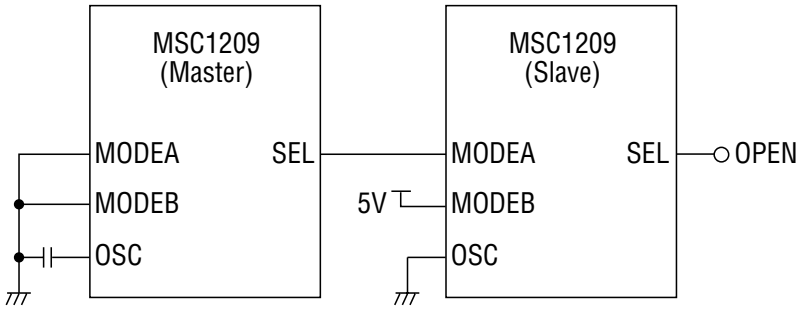
(MSB)	Dimming Data	(LSB)	Duty Ratio	
00	0000	0000	0/2048	
00	0000	0001	1/2048	
≀	≀	≀	≀	
11	1111	0111	1015/2048	
11	1111	1000	1016/2048	
11	1111	1001	1016.5/2048	Max
≀	≀	≀	≀	↓
11	1111	1110	1016.5/2048	Max

Note: Setting for address $3FF_H$ is invalid.

Duty ratios are programmable within the range of 0/2048 (0%) to 1016.5/2048 (49.6%). Figure 5 shows the grid output timing.

Cascade Connection

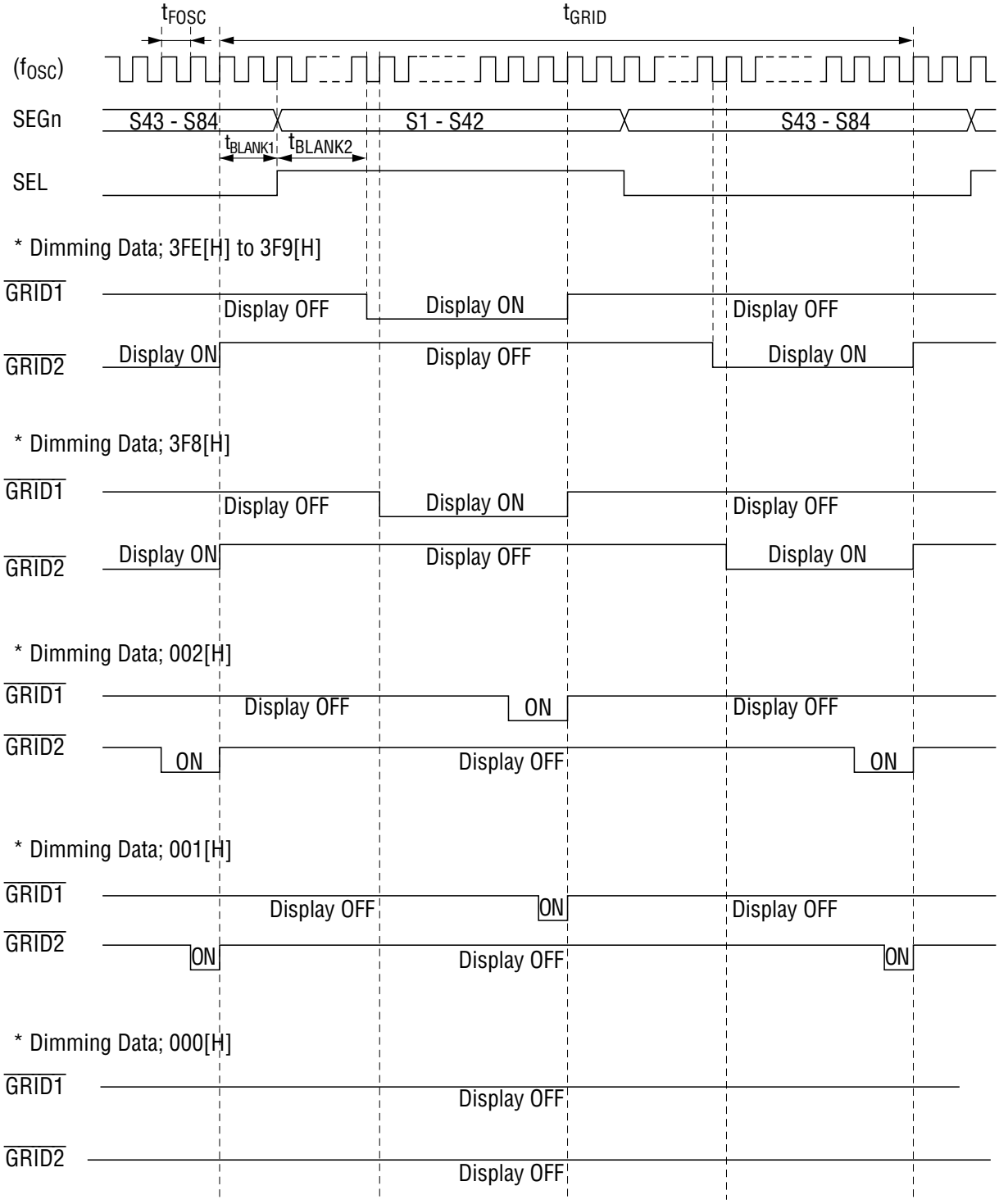
When two MSC1209 ICs are used in cascade connection, use the MODEA and MODEB pins to connect them, as shown below.



The IC where the MODEA and MODEB pins are set to "L" operates as the master, and the one where the MODEB pin is set to "H" as the slave.

By connecting the master side SEL output pin to the slave side MODEA pin, the segments on the slave side operate in synchronization with the grid on the master side.

GRID Output Timing

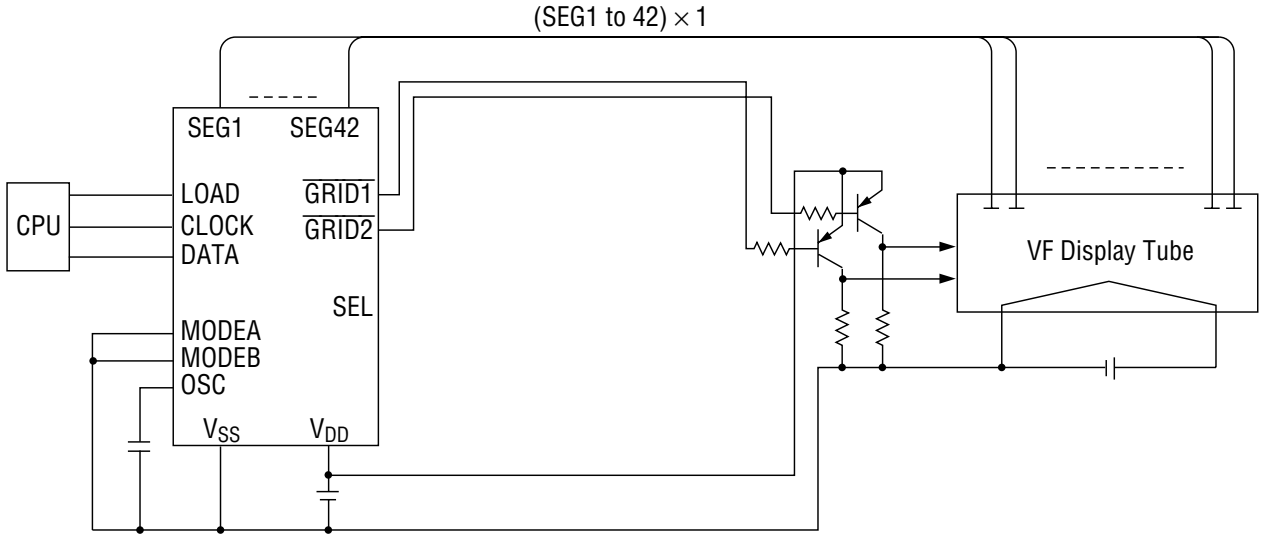


t_{FOSC} = 2µs Typical
$t_{GRID} = 2048t_{FOSC}$
$t_{BLANK1} = 2t_{FOSC}$, $t_{BLANK2} = 5.5t_{FOSC}$

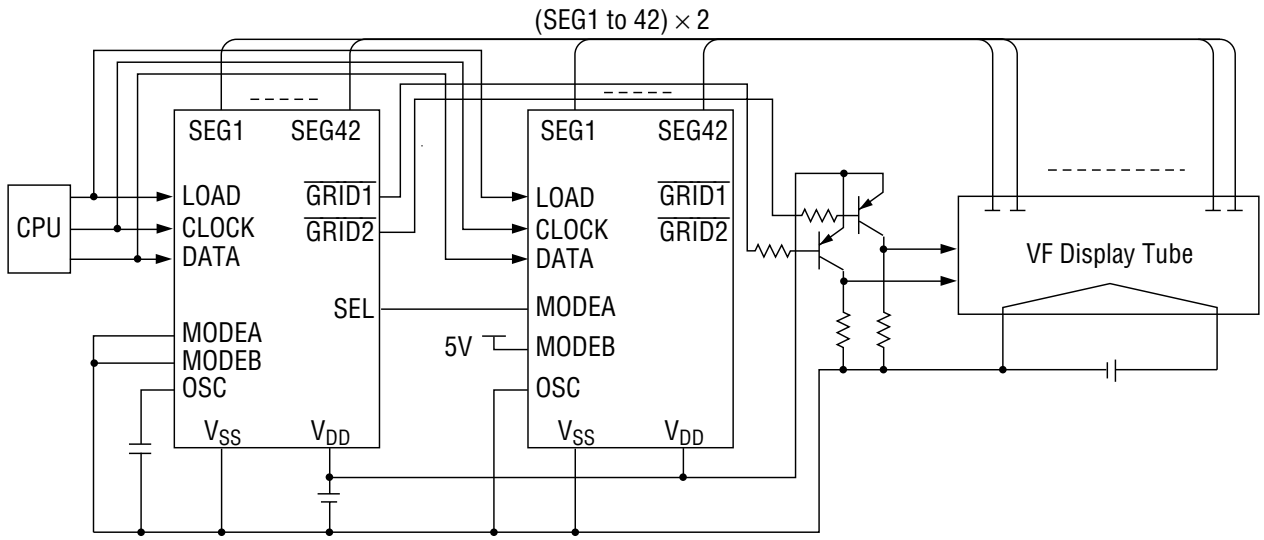
Figure 5 Dimming Data and Duty Ratio

APPLICATION CIRCUIT

* When one MSC1209 IC is used



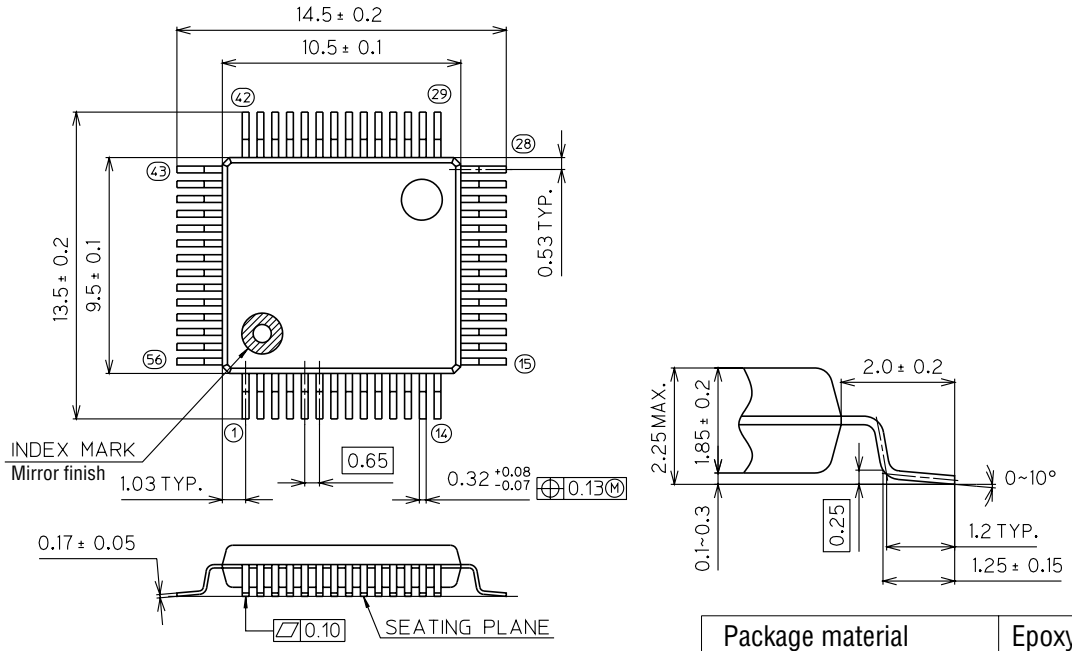
* When two MSC1209 ICs are used



PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents cotained herein may be reprinted or reproduced without our prior permission.

9. MS-DOS is a registered trademark of Microsoft Corporation.

Printed in Japan