MSC2343257A-xxBS8/DS8

4,194,304-Word × 32-Bit DRAM MODULE : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The Oki MSC2343257A-xxBS8/DS8 is a fully decoded 4,194,304-word × 32-bit CMOS dynamic random access memory composed of eight 16-Mb DRAMs (4M × 4) in SOJ. The mounting of eight DRAMs together with decoupling capacitors on a 72-pin glass epoxy SIMM Package supports any application where high density and large capacity of storage memory are required.

FEATURES

- 4,194,304-word × 32-bit organization
- 72-pin SIMM
  MSC2343257A-xxBS8 : Gold tab
  MSC2343257A-xxDS8 : Solder tab
- Single 5 V supply ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state, nonlatch
- Refresh : 2048 cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode with EDO capability

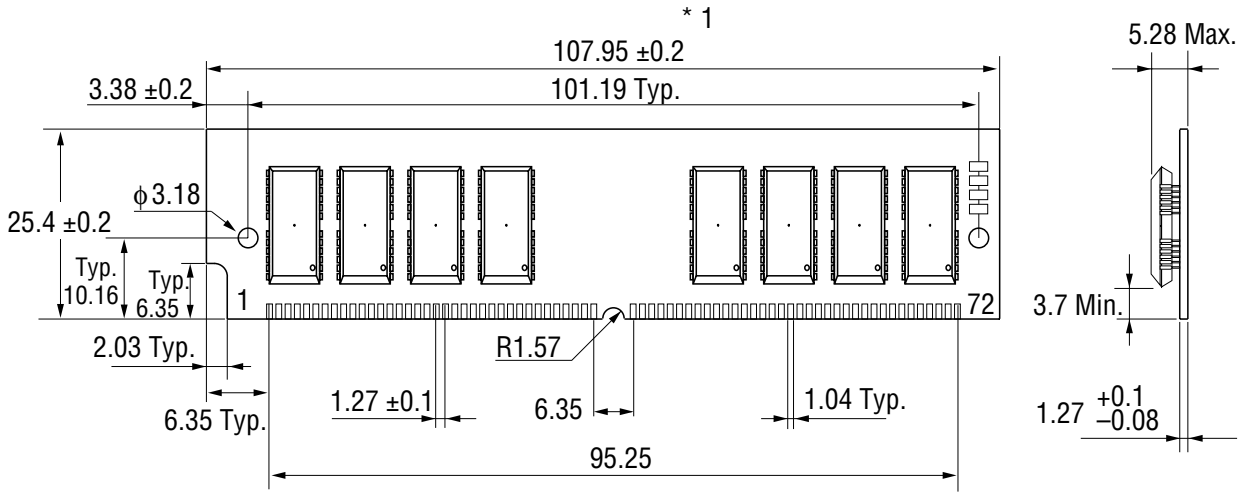
PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (Max.)	Standby (Max.)
MSC2343257A-60BS8/DS8	60 ns	30 ns	15 ns	110 ns	5280 mW	44 mW
MSC2343257A-70BS8/DS8	70 ns	35 ns	20 ns	130 ns	4840 mW	

PIN CONFIGURATION

MSC2343257A-xxBS8/DS8

(Unit : mm)



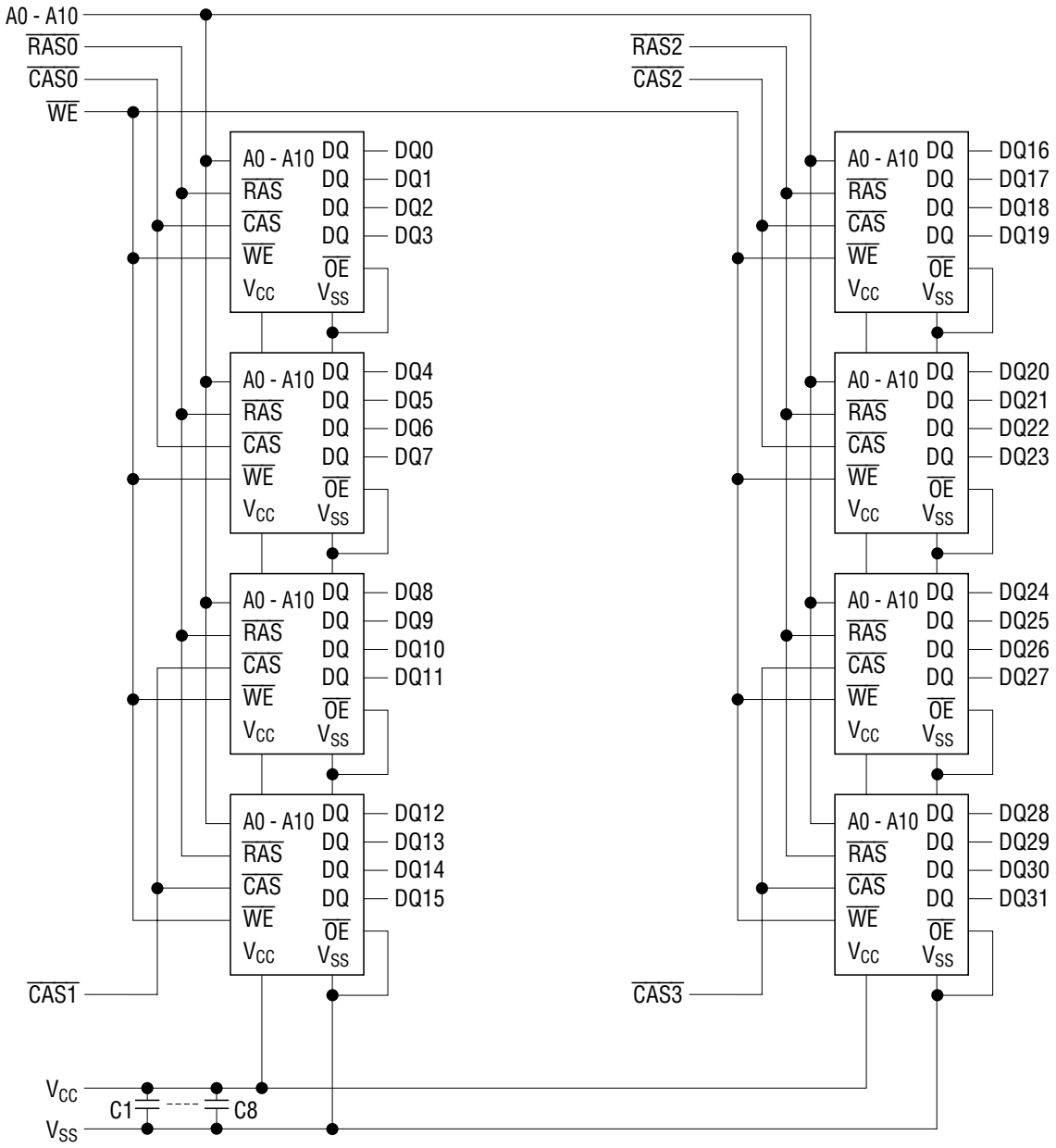
*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	16	A4	31	A8	46	NC	61	DQ13
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ30
3	DQ16	18	A6	33	NC	48	NC	63	DQ14
4	DQ1	19	A10	34	$\overline{RAS2}$	49	DQ8	64	DQ31
5	DQ17	20	DQ4	35	NC	50	DQ24	65	DQ15
6	DQ2	21	DQ20	36	NC	51	DQ9	66	NC
7	DQ18	22	DQ5	37	NC	52	DQ25	67	PD1
8	DQ3	23	DQ21	38	NC	53	DQ10	68	PD2
9	DQ19	24	DQ6	39	V_{SS}	54	DQ26	69	PD3
10	V_{CC}	25	DQ22	40	$\overline{CAS0}$	55	DQ11	70	PD4
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ27	71	NC
12	A0	27	DQ23	42	$\overline{CAS3}$	57	DQ12	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ28		
14	A2	29	NC	44	$\overline{RAS0}$	59	V_{CC}		
15	A3	30	Vcc	45	NC	60	DQ29		

Presence Detect Pins

Pin No.	Pin Name	MSC2343257A -60BS8/DS8	MSC2343257A -70BS8/DS8
67	PD1	V_{SS}	V_{SS}
68	PD2	NC	NC
69	PD3	NC	V_{SS}
70	PD4	NC	NC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–1.0 to 7.0	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	8	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C_{IN1}	—	57	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	—	65	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	—	35	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{IN4}	—	20	pF
I/O Capacitance (DQ0 - DQ31)	C_{DQ}	—	16	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSC2343257A -60BS8/DS8		MSC2343257A -70BS8/DS8		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	–80	80	–80	80	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V	–10	10	–10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = –5.0 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	960	—	880	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	16	—	16	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	8	—	8	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	960	—	880	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = Min.	—	960	—	880	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{HPC} = Min.	—	1120	—	1040	mA	1, 3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,10,11

Parameter	Symbol	MSC2343257A -60BS8/DS8		MSC2343257A -70BS8/DS8		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	25	—	30	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	ns	4
Output Hold Time from $\overline{CAS}$ Low	t_{DOH}	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	15	0	20	ns	7, 8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	15	0	20	ns	7, 8
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	15	0	20	ns	7
Transition Time	t_T	2	50	2	50	ns	3
Refresh Period	t_{REF}	—	32	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10k	10	10k	ns	
$\overline{RAS}$ Low to $\overline{CAS}$ High Delay Time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ High to $\overline{RAS}$ Low Delay Time	t_{CRP}	10	—	10	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	6
$\overline{RAS}$ to Second $\overline{CAS}$ Delay Time	t_{RSCD}	60	—	70	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	40	—	45	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,10,11

Parameter	Symbol	MSC2343257A -60BS8/DS8		MSC2343257A -70BS8/DS8		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	10	—	15	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	50	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	ns	
Write Command Pulse Width (Output Disable)	t_{WPE}	5	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	15	—	15	—	ns	
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	40	—	45	—	ns	
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	—	20	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	20	—	20	—	ns	

Notes:

1. A start-up delay of 200 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.

7. t_{CEZ} (Max.), t_{REZ} (Max.) and t_{WEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.

9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
    The test mode specified in this data sheet is an 8-bit parallel test function. CA0, CA1 and CA10 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
    The 4M × 32 module can be tested as an 1M × 32 module in this test mode.

11. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM I for AC Timing Waveforms