

OKI Semiconductor

MSC23836AA-xxBS20/DS20

8,388,608-Word × 36-Bit DRAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The OKI MSC23836AA-xxBS20/DS20 is a fully decoded 8,388,608-word × 36-bit CMOS Dynamic Random Access Memory Module composed of sixteen 16-Mb DRAMs (4M × 4) and four 8-Mb DRAMs (4M × 2) in SOJ packages mounted with decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for non-parity memory expansion applications such as fax machines, printers and personal computers.

FEATURES

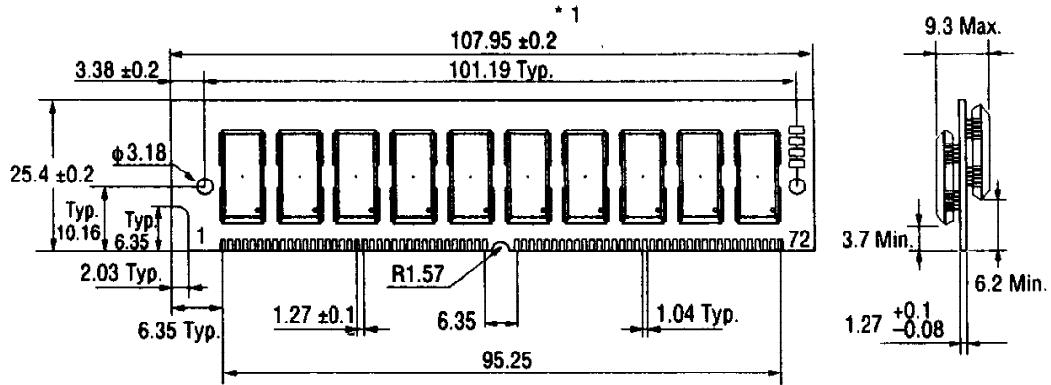
- 8-Meg × 36-bit organization
- 72-Pin Socket Insertable Module
 - MSC23836AA-xxBS20 : Gold tab
 - MSC23836AA-xxDS20 : Solder tab
- Single 5 V supply ±10% tolerance
- Access times : 60, 70, 80 ns
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 2048 cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

PRODUCT FAMILY

| Family | Access Time (Max.) | | | Cycle Time (Min.) | Power Dissipation | |
|------------------------|--------------------|-----------------|------------------|-------------------|-------------------|-----------------------|
| | t _{RAC} | t _{AA} | t _{CAC} | | Operating (Max.) | Standby (Max.) |
| MSC23836AA-60BS20/DS20 | 60 ns | 30 ns | 15 ns | 110 ns | 6875 mW | 110 mW (MOS level) |
| MSC23836AA-70BS20/DS20 | 70 ns | 35 ns | 20 ns | 130 ns | 6325 mW | |
| MSC23836AA-80BS20/DS20 | 80 ns | 40 ns | 20 ns | 150 ns | 5775 mW | |

PIN CONFIGURATION

MSC23836AA-xxBS20/DS20



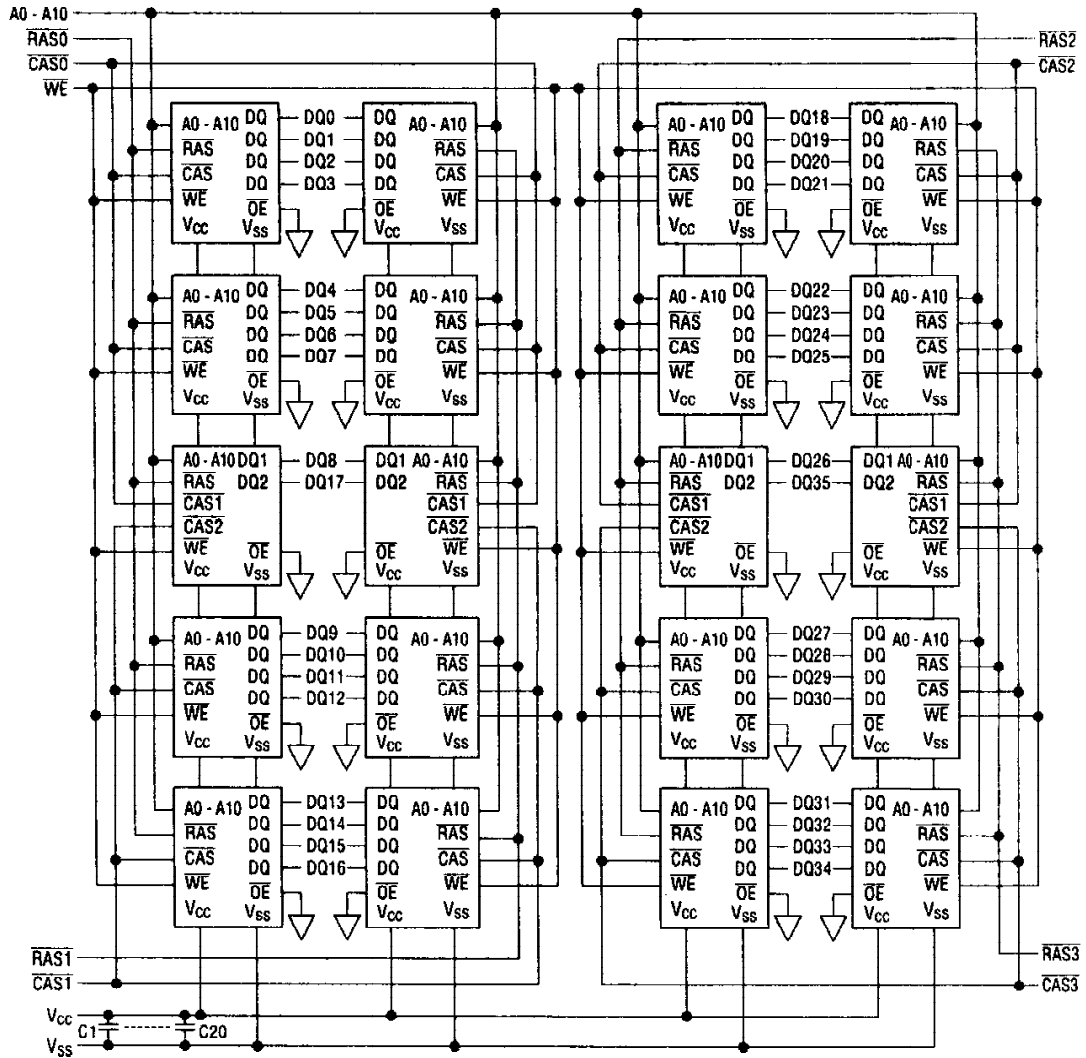
*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---------|-----------------|---------|-----------------|---------|-------------------|---------|-----------------|---------|-----------------|
| 1 | V _{SS} | 16 | A4 | 31 | A8 | 46 | NC | 61 | DQ14 |
| 2 | DQ0 | 17 | A5 | 32 | A9 | 47 | \overline{WE} | 62 | DQ33 |
| 3 | DQ18 | 18 | A6 | 33 | $\overline{RAS3}$ | 48 | NC | 63 | DQ15 |
| 4 | DQ1 | 19 | A10 | 34 | $\overline{RAS2}$ | 49 | DQ9 | 64 | DQ34 |
| 5 | DQ19 | 20 | DQ4 | 35 | DQ26 | 50 | DQ27 | 65 | DQ16 |
| 6 | DQ2 | 21 | DQ22 | 36 | DQ8 | 51 | DQ10 | 66 | NC |
| 7 | DQ20 | 22 | DQ5 | 37 | DQ17 | 52 | DQ28 | 67 | PD1 |
| 8 | DQ3 | 23 | DQ23 | 38 | DQ35 | 53 | DQ11 | 68 | PD2 |
| 9 | DQ21 | 24 | DQ6 | 39 | V _{SS} | 54 | DQ29 | 69 | PD3 |
| 10 | V _{CC} | 25 | DQ24 | 40 | $\overline{CAS0}$ | 55 | DQ12 | 70 | PD4 |
| 11 | NC | 26 | DQ7 | 41 | $\overline{CAS2}$ | 56 | DQ30 | 71 | NC |
| 12 | A0 | 27 | DQ25 | 42 | $\overline{CAS3}$ | 57 | DQ13 | 72 | V _{SS} |
| 13 | A1 | 28 | A7 | 43 | $\overline{CAS1}$ | 58 | DQ31 | | |
| 14 | A2 | 29 | NC | 44 | $\overline{RAS0}$ | 59 | V _{CC} | | |
| 15 | A3 | 30 | V _{CC} | 45 | $\overline{RAS1}$ | 60 | DQ32 | | |

Presence Detect Pins

| Pin No. | Pin Name | MSC23836AA -60BS20/DS20 | MSC23836AA -70BS20/DS20 | MSC23836AA -80BS20/DS20 |
|---------|----------|----------------------------|----------------------------|----------------------------|
| 67 | PD1 | NC | NC | NC |
| 68 | PD2 | V _{SS} | V _{SS} | V _{SS} |
| 69 | PD3 | NC | V _{SS} | NC |
| 70 | PD4 | NC | NC | V _{SS} |

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit |
|------------------------------------------------------------|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to V _{SS} | V _{IN} , V _{OUT} | -1.0 to 7.0 | V |
| Voltage V _{CC} Supply Relative to V _{SS} | V _{CC} | -1.0 to 7.0 | V |
| Short Circuit Output Current | I _{OS} | 50 | mA |
| Power Dissipation | P _D | 20 | W |
| Operating Temperature | T _{opr} | 0 to 70 | °C |
| Storage Temperature | T _{stg} | -40 to 125 | °C |

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions(T_a = 0°C to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|-----------------|------|------|------|------|
| Power Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | — | 6.5 | V |
| Input Low Voltage | V _{IL} | -1.0 | — | 0.8 | V |

Capacitance(T_a = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---------------------------------|------------------|------|------|------|
| Input Capacitance (A0 - A10) | C _{IN1} | — | 135 | pF |
| Input Capacitance (WE) | C _{IN2} | — | 155 | pF |
| Input Capacitance (RAS0 - RAS3) | C _{IN3} | — | 43 | pF |
| Input Capacitance (CAS0 - CAS3) | C _{IN4} | — | 50 | pF |
| I/O Capacitance (DQ0 - DQ35) | C _{DO} | — | 26 | pF |

Note: Capacitance measured with Boonton Meter.

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C)

| Parameter | Symbol | Condition | MSC23836AA -60BS20/DS20 | | MSC23836AA -70BS20/DS20 | | MSC23836AA -80BS20/DS20 | | Unit | Note |
|-------------------------------------------------------------|-----------|------------------------------------------------------------------------------------------------------------------------|----------------------------|----------|----------------------------|----------|----------------------------|----------|---------------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Input Leakage Current | I_{LI} | $0\text{ V} \leq V_I \leq 6.5\text{ V}$; All other pins not under test = 0 V | -200 | 200 | -200 | 200 | -200 | 200 | μA | |
| Output Leakage Current | I_{LO} | Dout disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$ | -20 | 20 | -20 | 20 | -20 | 20 | μA | |
| Output High Voltage | V_{OH} | $I_{OH} = -5.0\text{ mA}$ | 2.4 | V_{CC} | 2.4 | V_{CC} | 2.4 | V_{CC} | V | |
| Output Low Voltage | V_{OL} | $I_{OL} = 4.2\text{ mA}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |
| Average Power Supply Current (Operating) | I_{CC1} | $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$ | — | 1250 | — | 1150 | — | 1050 | mA | 1, 2 |
| Power Supply Current (Standby) | I_{CC2} | $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$ | — | 40 | — | 40 | — | 40 | mA | 1 |
| | | $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ $\geq V_{CC} - 0.2\text{ V}$ | — | 20 | — | 20 | — | 20 | mA | 1 |
| Average Power Supply Current (RAS-only Refresh) | I_{CC3} | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = \text{Min.}$ | — | 1250 | — | 1150 | — | 1050 | mA | 1, 2 |
| Average Power Supply Current (CAS before RAS Refresh) | I_{CC6} | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, $t_{RC} = \text{Min.}$ | — | 1250 | — | 1150 | — | 1050 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | I_{CC7} | $\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$ | — | 1150 | — | 1050 | — | 950 | mA | 1, 3 |

- Notes: 1. Specified values are obtained with the output open.
 2. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 3. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3,9,10

| Parameter | Symbol | MSC23836AA -80BS20/DS20 | | MSC23836AA -70BS20/DS20 | | MSC23836AA -80BS20/DS20 | | Unit | Note |
|------------------------------------|-------------------|---------------------------------|-----------------|----------------------------|------|----------------------------|------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| | | Random Read or Write Cycle Time | t _{RC} | 110 | — | 130 | — | | |
| Fast Page Mode Cycle Time | t _{PC} | 40 | — | 45 | — | 50 | — | ns | |
| Access Time from RAS | t _{RAC} | — | 60 | — | 70 | — | 80 | ns | 4, 5, 6 |
| Access Time from CAS | t _{CAC} | — | 15 | — | 20 | — | 20 | ns | 4, 5 |
| Access Time from Column Address | t _{AA} | — | 30 | — | 35 | — | 40 | ns | 4, 6 |
| Access Time from CAS Precharge | t _{CPA} | — | 35 | — | 40 | — | 45 | ns | 4 |
| Output Low Impedance Time from CAS | t _{CLZ} | 0 | — | 0 | — | 0 | — | ns | 4 |
| Output Buffer Turn-off Delay Time | t _{OFF} | 0 | 15 | 0 | 20 | 0 | 20 | ns | 7 |
| Transition Time | t _T | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | t _{REF} | — | 32 | — | 32 | — | 32 | ms | |
| RAS Precharge Time | t _{RP} | 40 | — | 50 | — | 60 | — | ns | |
| RAS Pulse Width | t _{RAS} | 60 | 10K | 70 | 10K | 80 | 10K | ns | |
| RAS Pulse Width (Fast Page Mode) | t _{RASP} | 60 | 100K | 70 | 100K | 80 | 100K | ns | |
| RAS Hold Time | t _{RSH} | 15 | — | 20 | — | 20 | — | ns | |
| CAS Precharge Time | t _{CP} | 10 | — | 10 | — | 10 | — | ns | |
| CAS Pulse Width | t _{CAS} | 15 | 10K | 20 | 10K | 20 | 10K | ns | |
| CAS Hold Time | t _{CSH} | 60 | — | 70 | — | 80 | — | ns | |
| CAS to RAS Precharge Time | t _{CRP} | 10 | — | 10 | — | 10 | — | ns | |
| RAS to CAS Delay Time | t _{RCD} | 20 | 45 | 20 | 50 | 20 | 60 | ns | 5 |
| RAS to Column Address Delay Time | t _{RAD} | 15 | 30 | 15 | 35 | 15 | 40 | ns | 6 |
| Row Address Set-up Time | t _{ASR} | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | t _{RAH} | 10 | — | 10 | — | 10 | — | ns | |
| Column Address Set-up Time | t _{ASC} | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | t _{CAH} | 15 | — | 15 | — | 15 | — | ns | |
| Column Address Hold Time from RAS | t _{AR} | 50 | — | 55 | — | 60 | — | ns | |
| Column Address to RAS Lead Time | t _{RAL} | 30 | — | 35 | — | 40 | — | ns | |

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3,9,10

| Parameter | Symbol | MSC23836AA -60BS20/DS20 | | MSC23836AA -70BS20/DS20 | | MSC23836AA -80BS20/DS20 | | Unit | Note |
|-----------------------------------------------------------------------------------------------------------------------------|------------------|----------------------------|------------------|----------------------------|------|----------------------------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| | | Read Command Set-up Time | t _{RCS} | 0 | — | 0 | — | | |
| Read Command Hold Time | t _{RCH} | 0 | — | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{\text{RAS}}$ | t _{RRH} | 0 | — | 0 | — | 0 | — | ns | 8 |
| Write Command Set-up Time | t _{WCS} | 0 | — | 0 | — | 0 | — | ns | |
| Write Command Hold Time | t _{WCH} | 10 | — | 15 | — | 15 | — | ns | |
| Write Command Hold Time from $\overline{\text{RAS}}$ | t _{WCR} | 45 | — | 55 | — | 60 | — | ns | |
| Write Command Pulse Width | t _{WP} | 10 | — | 10 | — | 10 | — | ns | |
| Write Command to $\overline{\text{RAS}}$ Lead Time | t _{RWL} | 15 | — | 20 | — | 20 | — | ns | |
| Write Command to CAS Lead Time | t _{CWL} | 15 | — | 20 | — | 20 | — | ns | |
| Data-in Set-up Time | t _{DS} | 0 | — | 0 | — | 0 | — | ns | |
| Data-in Hold Time | t _{DH} | 15 | — | 15 | — | 15 | — | ns | |
| Data-in Hold Time from $\overline{\text{RAS}}$ | t _{DHR} | 50 | — | 55 | — | 60 | — | ns | |
| CAS Active Delay Time from $\overline{\text{RAS}}$ Precharge | t _{RPC} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{RAS}}$ to CAS Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) | t _{CSR} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{RAS}}$ to CAS Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) | t _{CHR} | 20 | — | 20 | — | 20 | — | ns | |
| CAS Precharge Time (Refresh Counter Test) | t _{CPT} | 40 | — | 40 | — | 40 | — | ns | |
| $\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) | t _{WRP} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) | t _{WRH} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode) | t _{WTS} | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode) | t _{WTH} | 20 | — | 20 | — | 20 | — | ns | |

- Notes:
1. A start-up delay of 200 μ s is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
When using the internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
 2. AC measurement assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is an 8-bit parallel test function. CA10, CA1 and CA0 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 10. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM E for AC Timing Waveforms