OKI semiconductor

MSC23V13258D-xxBS2

1,048,576 Word X 32 Bit DYNAMIC RAM MODULE

DESCRIPTION

The Oki MSC23V13258D-xxBS2 is a fully decoded, 1,048,576-word X 32 bit CMOS dynamic random access memory composed of two 16-Mb (1Mx16) DRAMs in TSOP packages. The mounting of two DRAMs together with decoupling capacitors on a 100-pin glass epoxy DIMM Package supports any application where high density and large capacity of storage memory are required.

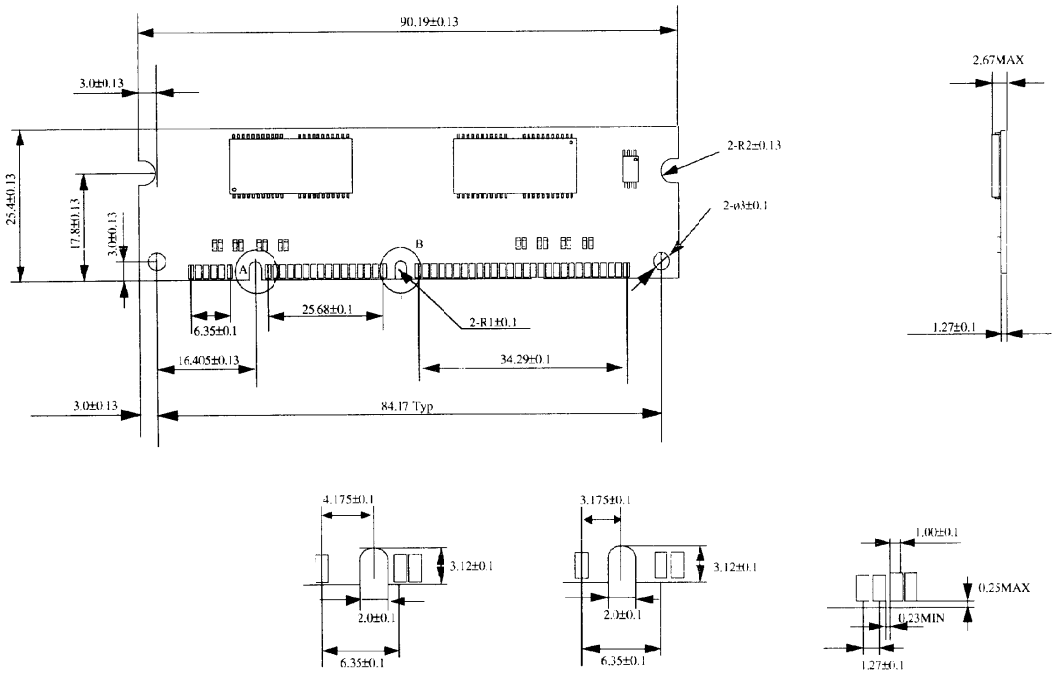
FEATURES

- 1,048,576- word X 32-Bit organization
- Single 3.3V supply ± 0.3V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible,3-state,nonlatch
- Refresh : 1024 cycles/16 ms (10 Row/10 Column Addresses)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Fast Page Mode With EDO capability
- Serial Presence Detect
- Unbuffered, with damping resistors on all DQ signals.

FAMILY ORGANIZATION

FAMILY	ACCESS TIME (MAX)				Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	(MAX)	Operating (MAX)	Standby (Max)
MSC23V13258D-60BS2	60ns	30ns	15ns	15ns	104ns	1152mW	3.6mW
MSC23V13258D-70BS2	70ns	35ns	20ns	20ns	124ns	1008mW	

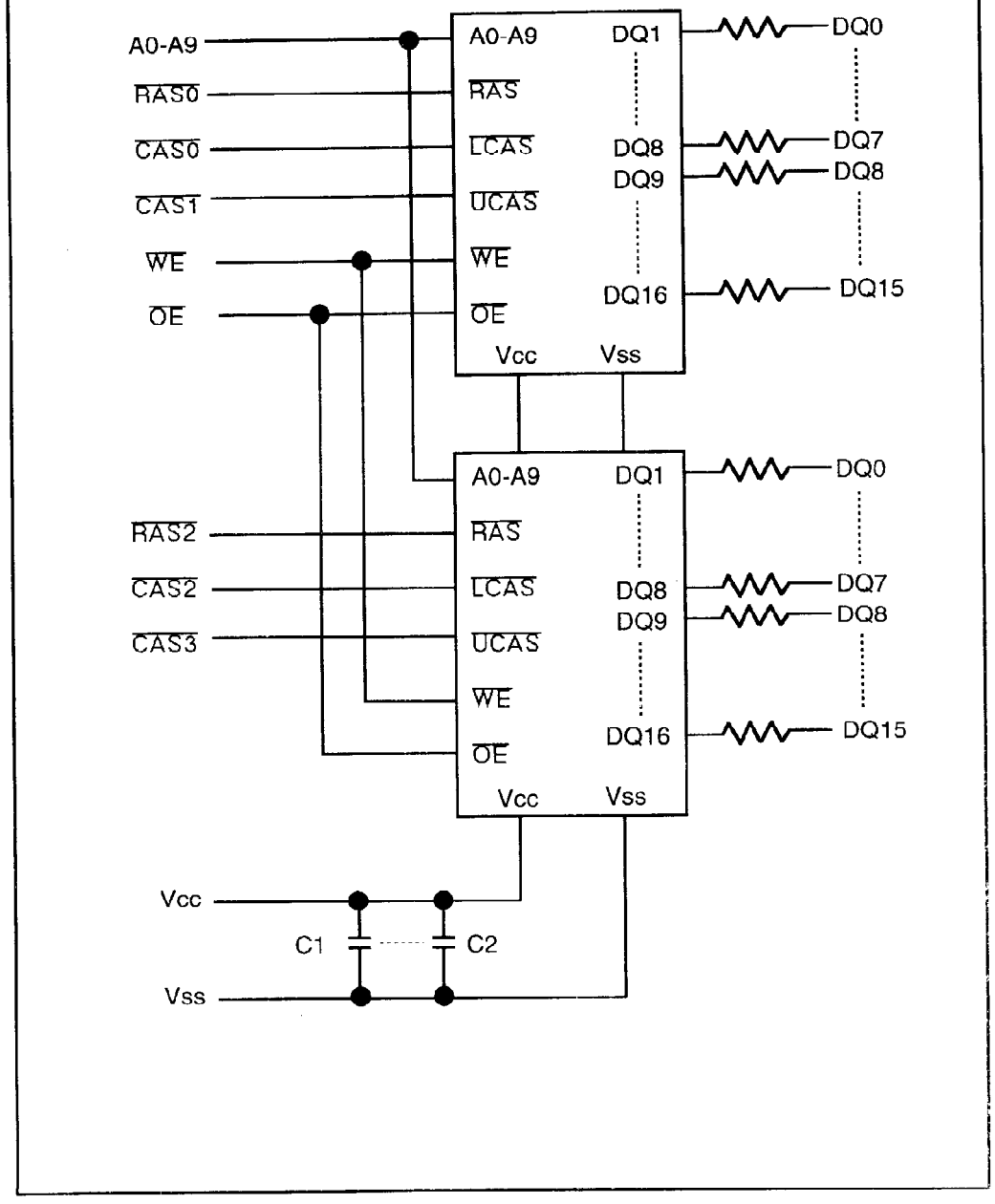
MSC23V13258D-60BS2



DETAIL A DETAIL B

FUNCTIONAL BLOCK DIAGRAM

MSC23V13258D-xxBS2/DS2



PIN CONFIGURATION

MSC23V13258D-xxBS2

Front Side

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	Vss	16	A6	31	Vcc	46	DQ23
2	DQ0	17	A8	32	NC	47	Vss
3	DQ1	18	NC	33	NC	48	SDA
4	DQ2	19	NC	34	NC	49	SCL
5	DQ3	20	NC	35	NC	50	Vcc
6	Vcc	21	Vcc	36	Vss		
7	DQ4	22	NC	37	$\overline{CAS2}$		
8	DQ5	23	NC	38	DQ16		
9	DQ6	24	NC	39	DQ17		
10	DQ7	25	NC	40	DQ18		
11	$\overline{CAS0}$	26	Vss	41	DQ19		
12	Vss	27	NC	42	Vcc		
13	A0	28	$\overline{WE}$	43	DQ20		
14	A2	29	$\overline{RAS0}$	44	DQ21		
15	A4	30	$\overline{RAS2}$	45	DQ22		

Back Side

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
51	Vss	66	A7	81	Vcc	96	DQ31
52	DQ8	67	A9	82	NC	97	Vss
53	DQ9	68	NC	83	NC	98	SA0
54	DQ10	69	NC	84	NC	99	SA1
55	DQ11	70	NC	85	NC	100	SA2
56	Vcc	71	Vcc	86	Vss		
57	DQ12	72	NC	87	$\overline{CAS3}$		
58	DQ13	73	NC	88	DQ24		
59	DQ14	74	NC	89	DQ25		
60	DQ15	75	NC	90	DQ26		
61	$\overline{CAS1}$	76	Vss	91	DQ27		
62	Vss	77	NC	92	Vcc		
63	A1	78	$\overline{OE}$	93	DQ28		
64	A3	79	NC	94	DQ29		
65	A5	80	NC	95	DQ30		

Serial PD Matrix

Byte Number	HEX DATA	Remark
0	0D	Number of Byte used(13 Byte)
1	08	Total SPD Memory size (256 Bytes)
2	02	Memory type(EDO)
3	0A	Number of Rows(10)
4	0A	Number of Columns(10)
5	01	Number of Banks(1)
6	20	Module Data With(32)
7	00	Not defined
8	01	Supply Voltage(3.3v, LVTTL)
9(-60)	3C	RAS Access time(60ns)
9(-70)	46	RAS Access time(70ns)
10(-60)	0F	CAS Access time(15ns)
10(-70)	14	CAS Access time(20ns)
11	00	Non-Parity
12	00	Normal Refresh

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.5 ~ +4.6	V
Voltage Vcc supply relative to Vss	V_{CC}	- 0.5 ~+4.6	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	2	W
Operating temperature	T_{OPR}	-0 ~ +70	°C
Storage temperature	T_{STG}	- 40 ~ +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliabity.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYPE	MAX	UNIT	Operating temperature
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	0 °C ~ +70 °C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	-	Vcc+0.3	V	
Input low voltage	V_{IL}	-0.3	-	0.8	V	

CAPACITANCE

Parameter	Symbol	Type	MAX	Unit
Input Capacitance(A0-A9)	C_{IN1}	-	16	pF
Input Capacitance($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN2}	-	13	pF
Input Capacitance($\overline{CAS0}$-$\overline{CAS3}$)	C_{IN3}	-	13	pF
Input Capacitance($\overline{WE}$)	C_{IN4}	-	20	pF
I/O Capacitance(DQ0-DQ31)	CDQ	-	13	pF

NOTE: Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(Vcc = 3.3V ± 0.3V, Ta = 0~70)

Parameter	Symbol	Condition	MSC23V13258D -60BS2		MSC23V13258D -70BS2		Unit	Note
			Min	Max	Min	Max		
Input Leakage Current	I_{LI}	$0V \le V_{in} \le Vcc+0.3V$: All other pins not under test = 0V	-20	20	-20	20	μA	
Output Leakage Current	I_{LO}	DQ=disable $0V \le V_{out} \le V_{cc+}0.3V$	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	I_{OH} = -2.0mA	2.4	Vcc	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling RC=min	-	320	-	280	mA	1,2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ =V_{IH}	-	4	-	4	mA	
		$\overline{RAS}$≥ Vcc-0.2V $\overline{CAS}$≥ Vcc-0.2V	-	1	-	1	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ =VIH, t_{RC}=min	-	320	-	280	mA	1,2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$ refresh	-	320	-	280	mA	1
Average power supply current (Fast page)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	-	320	-	280	mA	1,3

NOTE: 1. Icc Max. is Specified as Icc for output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC CHARACTERISTIC

(Vcc = 3.3V ± 0.3V, Ta = 0 ~+70)

NOTE 1.2.3.9.10

Parameter	Symbol	MSC23V13258D -60BS2		MSC23V13258D -70BS2		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	104	-	124	-	ns	
Fast page mode cycle time	t_{HPC}	25	-	30	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	-	15	-	20	ns	4,5
Access time from column address	t_{AA}	-	30	-	35	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	ns	4
Access time from $\overline{OE}$	t_{OEA}	-	15	-	20	ns	4
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0	-	0	-	ns	4
Data Output Hold After $\overline{CAS}$ Low	t_{DOH}	5	-	5	-	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	15	0	20	ns	7,8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	15	0	20	ns	7,8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	20	ns	7
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	15	0	20	ns	7
Transition time	t_T	1	50	1	50	ns	3
Refresh period	t_{REF}	-	16	-	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	40	-	50	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	10	-	13	-	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	10	-	13	-	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	-	10	-	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	13	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	-	45	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	50	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	6
Row address set-up time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	ns	
Column address hold time	t_{CAH}	10	-	13	-	ns	

AC CHARACTERISTICS (Continued)

(Vcc = 5V ± 10%, Ta = 0 ~70 °C)

NOTE 1.2.3.9.10

Parameter	Symbol	MSC23V13258D -60BS2		MSC23V13258D -70BS2		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	ns	9
Write command set-up time	t_{WCS}	0	-	0	-	ns	10
Write command hold time	t_{WCH}	10	-	13	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	ns	
Write command pulse width	t_{WPE}	10	-	10	-	ns	
$\overline{OE}$ command hold time	t_{OEH}	10	-	13	-	ns	
$\overline{OE}$ precharge time	t_{OEP}	10	-	10	-	ns	
$\overline{OE}$ low to $\overline{CAS}$ high delay time	t_{OCH}	10	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	-	13	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	-	13	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	ns	
Data-in hold time	t_{DH}	10	-	13	-	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	15	-	20	-	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	-	44	-	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	49	-	59	-	ns	10
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	-	94	-	ns	10
$\overline{CAS}$ precharge $\overline{WE}$ delay time	t_{CPWD}	54	-	64	-	ns	10
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	-	10	-	ns	

NOTES: 1) An initial pause of 200 µs is required after power-up followed by a minimum of 8 initializatin cycles (examples: $\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2) The AC measurements assume tT = 2 ns.

3) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals.Transition times are measured between V_{IH} and V_{IL}.

4) Measured with a load circuit equivalent to 2 TTL + 100 pF.

5) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD}(max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.

6) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD}(max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

7) The t_{CEZ} (max.), t_{REZ} (max.), T_{WEZ} (max.) and t_{OEZ} (max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8) The t_{CEZ} and t_{Rez} must be satisfied for open circuit condition.

9) t_{RCH} or the t_{REZ} must be satisfied for a read cycle.

10) t_{WCS}, t_{CWD}, t_{RWD} t_{AWD} and t_{CPWD} are not restrictive operating parameters. they are included in the data sheet as electricalcharacteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min.)}$, $t_{RWD} \geq t_{RWD(min.)}$ $t_{AWD} \geq t_{AWD(min.)}$and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read modify write cycle and data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data(at access time) is indeterminate