Preliminary

OKI Semiconductor

MSC23V26457TA-xxBS8/ MSC23V26457SA-xxBS8

2,097,152-Word × 64-Bit DRAM MODULE : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The Oki MSC23V26457TA-xxBS8/MSC23V26457SA-xxBS8 is a fully decoded 2,097,152-word × 64-bit CMOS dynamic random access memory composed of eight 16-Mb DRAMs (2M × 8) in TSOP or SOJ packages mounted with decoupling capacitors on an 168-pin glass epoxy DIMM Package supports any application where high density and large capacity of storage memory are required.

FEATURES

- 2,097,152-word × 64-bit (8 Byte) organization
- 168-pin DIMM
  MSC23V26457TA-xxBS8 : TSOP type
  MSC23V26457SA-xxBS8 : SOJ type
- Single 3.3 V supply ±0.3 V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible, 3-state, nonlatch
- Refresh : 2048 cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode with EDO capability
- Serial Presence Detect

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSC23V26457TA-60BS8 MSC23V26457SA-60BS8	60 ns	30 ns	15 ns	15 ns	110 ns	4320 mW	28.8 mW
MSC23V26457TA-70BS8 MSC23V26457SA-70BS8	70 ns	35 ns	20 ns	20 ns	130 ns	3744 mW	

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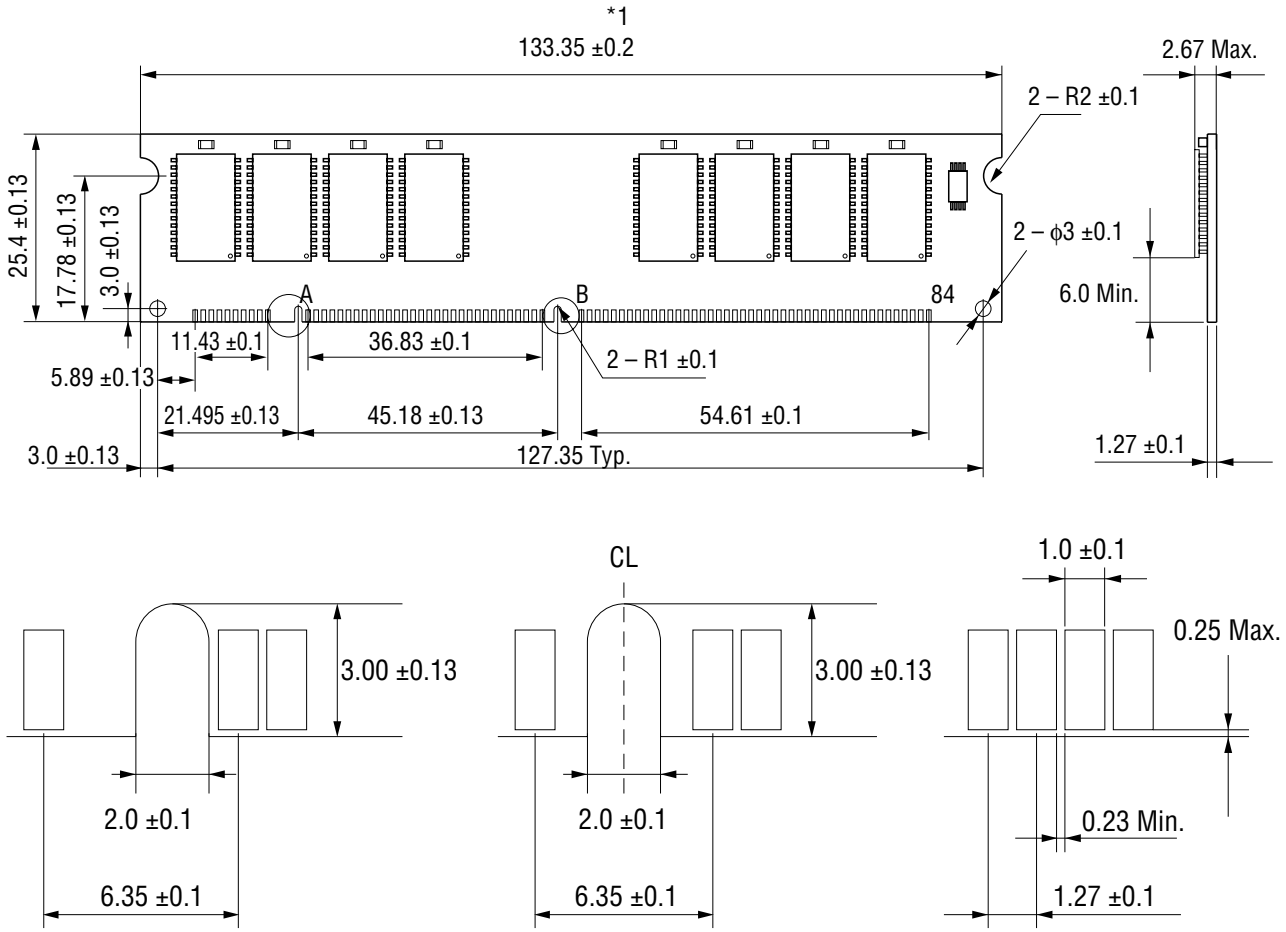
PIN CONFIGURATION

MSC23V26457TA-xxBS8

(Unit : mm)



*1 The common size difference of the board width 19.78 mm of its height is specified as ±0.2. The value above 19.78 mm is specified as ±0.5.

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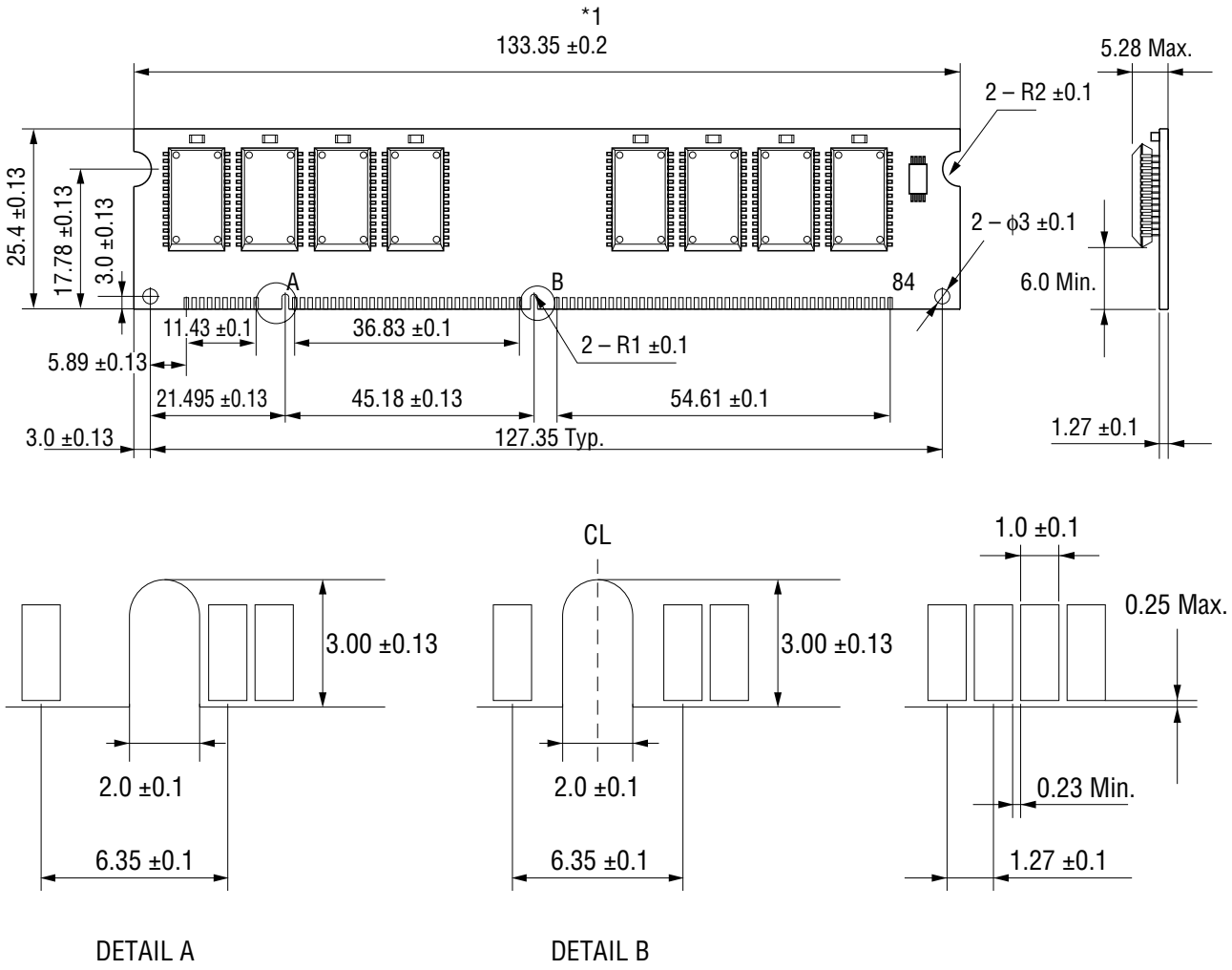
MSC23V26457SA-xxBS8

(Unit : mm)



*1 The common size difference of the board width 19.78 mm of its height is specified as ±0.2. The value above 19.78 mm is specified as ±0.5.

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Front Side

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	18	V_{CC}	35	A4	52	NC	69	DQ24
2	DQ0	19	DQ14	36	A6	53	NC	70	DQ25
3	DQ1	20	DQ15	37	A8	54	V_{SS}	71	DQ26
4	DQ2	21	NC	38	A10R	55	DQ16	72	DQ27
5	DQ3	22	NC	39	NC	56	DQ17	73	V_{CC}
6	V_{CC}	23	V_{SS}	40	V_{CC}	57	DQ18	74	DQ28
7	DQ4	24	NC	41	V_{CC}	58	DQ19	75	DQ29
8	DQ5	25	NC	42	NC	59	V_{CC}	76	DQ30
9	DQ6	26	V_{CC}	43	V_{SS}	60	DQ20	77	DQ31
10	DQ7	27	$\overline{WE0}$	44	$\overline{OE2}$	61	NC	78	V_{SS}
11	DQ8	28	$\overline{CAS0}$	45	$\overline{RAS2}$	62	NC	79	NC
12	V_{SS}	29	$\overline{CAS1}$	46	$\overline{CAS2}$	63	NC	80	NC
13	DQ9	30	$\overline{RAS0}$	47	$\overline{CAS3}$	64	V_{SS}	81	NC
14	DQ10	31	$\overline{OE0}$	48	$\overline{WE2}$	65	DQ21	82	SDA
15	DQ11	32	V_{SS}	49	V_{CC}	66	DQ22	83	SCL
16	DQ12	33	A0	50	NC	67	DQ23	84	V_{CC}
17	DQ13	34	A2	51	NC	68	V_{SS}		

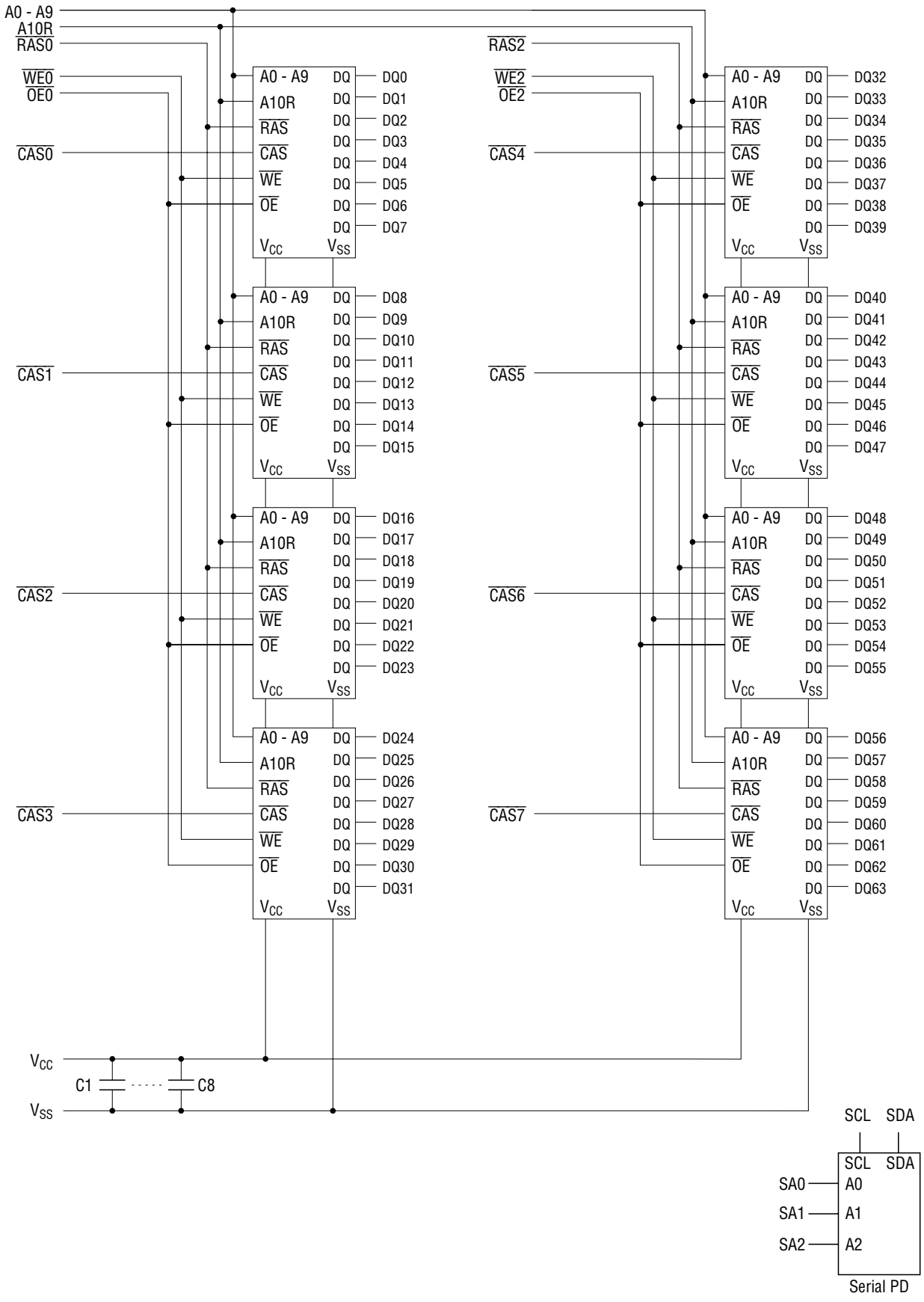
Back Side

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
85	V_{SS}	102	V_{CC}	119	A5	136	NC	153	DQ56
86	DQ32	103	DQ46	120	A7	137	NC	154	DQ57
87	DQ33	104	DQ47	121	A9	138	V_{SS}	155	DQ58
88	DQ34	105	NC	122	NC	139	DQ48	156	DQ59
89	DQ35	106	NC	123	NC	140	DQ49	157	V_{CC}
90	V_{CC}	107	V_{SS}	124	V_{CC}	141	DQ50	158	DQ60
91	DQ36	108	NC	125	NC	142	DQ51	159	DQ61
92	DQ37	109	NC	126	NC	143	V_{CC}	160	DQ62
93	DQ38	110	V_{CC}	127	V_{SS}	144	DQ52	161	DQ63
94	DQ39	111	NC	128	NC	145	NC	162	V_{SS}
95	DQ40	112	$\overline{CAS4}$	129	NC	146	NC	163	NC
96	V_{SS}	113	$\overline{CAS5}$	130	$\overline{CAS6}$	147	NC	164	NC
97	DQ41	114	NC	131	$\overline{CAS7}$	148	V_{SS}	165	SA0
98	DQ42	115	NC	132	NC	149	DQ53	166	SA1
99	DQ43	116	V_{SS}	133	V_{CC}	150	DQ54	167	SA2
100	DQ44	117	A1	134	NC	151	DQ55	168	V_{CC}
101	DQ45	118	A3	135	NC	152	V_{SS}		

Serial PD Matrix

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Remark
0	0	0	0	0	1	1	0	1	Number of Bytes used (13 Bytes)
1	0	0	0	0	1	0	0	0	Total SPD Memory size (256 Bytes)
2	0	0	0	0	0	0	1	0	Memory type (EDO)
3	0	0	0	0	1	0	1	1	Number of Rows (11)
4	0	0	0	0	1	0	1	0	Number of Columns (10)
5	0	0	0	0	0	0	0	1	Number of Banks (1)
6	0	1	0	0	0	0	0	0	Module Data Width (64)
7	0	0	0	0	0	0	0	0	Module Data Width Continued (0)
8	0	0	0	0	0	0	1	0	Supply Voltage (3.3 V, LVTTL)
9 (-60)	0	0	1	1	1	1	0	0	$\overline{\text{RAS}}$ Access Time (60 ns)
9 (-70)	0	1	0	0	0	1	1	0	$\overline{\text{RAS}}$ Access Time (70 ns)
10 (-60)	0	0	0	0	1	1	1	1	$\overline{\text{CAS}}$ Access Time (15 ns)
10 (-70)	0	0	0	1	0	1	0	0	$\overline{\text{CAS}}$ Access Time (20 ns)
11	0	0	0	0	0	0	0	0	Non parity
12	0	0	0	0	0	0	0	0	Normal Refresh

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to 4.6	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	8	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, A10R)	C_{IN1}	—	49	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$, $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$)	C_{IN2}	—	35	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS7}$)	C_{IN3}	—	13	pF
I/O Capacitance (DQ0 - DQ63)	C_{DQ}	—	13	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	-60		-70		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ V_{CC} + 0.3 V; All other pins not under test = 0 V	–80	80	–80	80	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 3.6 V	–10	10	–10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	1200	—	1040	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	16	—	16	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	8	—	8	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	1200	—	1040	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = Min.	—	1200	—	1040	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{HPC} = Min.	—	1200	—	1040	mA	1, 3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

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AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1,2,3,12,13

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	ns	
Read Modify Write Cycle Time	t_{RWC}	150	—	180	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	80	—	95	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	ns	4
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	ns	4
Output Hold Time from $\overline{CAS}$ Low	t_{DOH}	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	15	0	15	ns	7, 8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	15	0	15	ns	7, 8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	15	ns	7
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	15	0	15	ns	7
Transition Time	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	32	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	15	—	20	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10k	20	10k	ns	
$\overline{RAS}$ Low to $\overline{CAS}$ High Delay Time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ High to $\overline{RAS}$ Low Delay Time	t_{CRP}	5	—	5	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$, $\overline{OE}$ Hold Time (Output Disable)	t_{CHO}	5	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	6
$\overline{RAS}$ to Second $\overline{CAS}$ Delay Time	t_{RSCD}	60	—	70	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	40	—	45	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1,2,3,12,13

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	10	—	15	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	40	—	45	—	ns	
Write Command Pulse Width	t_{WP}	10	—	15	—	ns	
Write Command Pulse Width (Output Disable)	t_{WPE}	5	—	10	—	ns	
$\overline{WE}$ Low to $\overline{OE}$ Low Delay Time	t_{OEH}	15	—	20	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	10	—	10	—	ns	
$\overline{OE}$ Low to $\overline{CAS}$ High Delay Time	t_{OCH}	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	ns	11
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	40	—	45	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	15	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	ns	10
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	55	—	65	—	ns	10
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	15	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	10	—	10	—	ns	

Notes:

1. A start-up delay of 200 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.

7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.

9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.) the cycle is an early write cycle and the data output pin will remain in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and the data output pin will contain data read from the selected cell. If neither conditions is satisfied, the data output logic state (at access time) is undefined.

11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle or a read modify write cycle.

12. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
    In the test mode CA9 is not used and each DQ pin now accesses 2 bit locations. In a read cycle, if the 2 data bits are equal, the DQ pin will indicate a high level. If the 2 data bits are not equal, the DQ pin will indicate a low level.
    The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

13. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM K for AC Timing Waveforms