

MSM5116400B

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM5116400B is a 4,194,304-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5116400B achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5116400B is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.

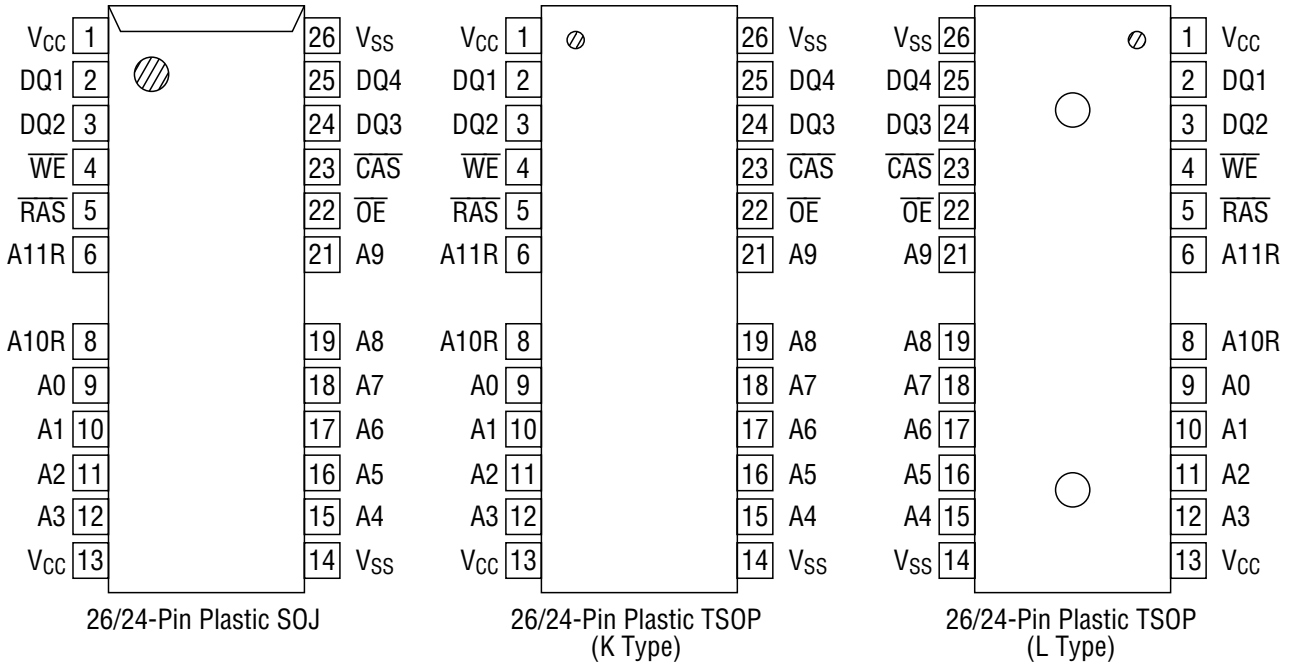
FEATURES

- 4,194,304-word × 4-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 4096 cycles/64 ms
- Fast page mode, read modify write capability
- CAS before RAS refresh, hidden refresh, RAS-only refresh capability
- Multi-bit test mode capability
- Package options:
 26/24-pin 300 mil plastic SOJ (SOJ26/24-P-300-1.27) (Product : MSM5116400B-xxSJ)
 26/24-pin 300 mil plastic TSOP (TSOPII26/24-P-300-1.27-K) (Product : MSM5116400B-xxTS-K)
 (TSOPII26/24-P-300-1.27-L) (Product : MSM5116400B-xxTS-L)
 xx indicates speed rank.

PRODUCT FAMILY

| Family | Access Time (Max.) | | | | Cycle Time (Min.) | Power Dissipation | |
|----------------|--------------------|-----------------|------------------|------------------|-------------------|-------------------|----------------|
| | t _{RAC} | t _{AA} | t _{CAC} | t _{OEA} | | Operating (Max.) | Standby (Max.) |
| MSM5116400B-50 | 50 ns | 25 ns | 13 ns | 13 ns | 90 ns | 550 mW | 5.5 mW |
| MSM5116400B-60 | 60 ns | 30 ns | 15 ns | 15 ns | 110 ns | 495 mW | |
| MSM5116400B-70 | 70 ns | 35 ns | 20 ns | 20 ns | 130 ns | 440 mW | |

PIN CONFIGURATION (TOP VIEW)

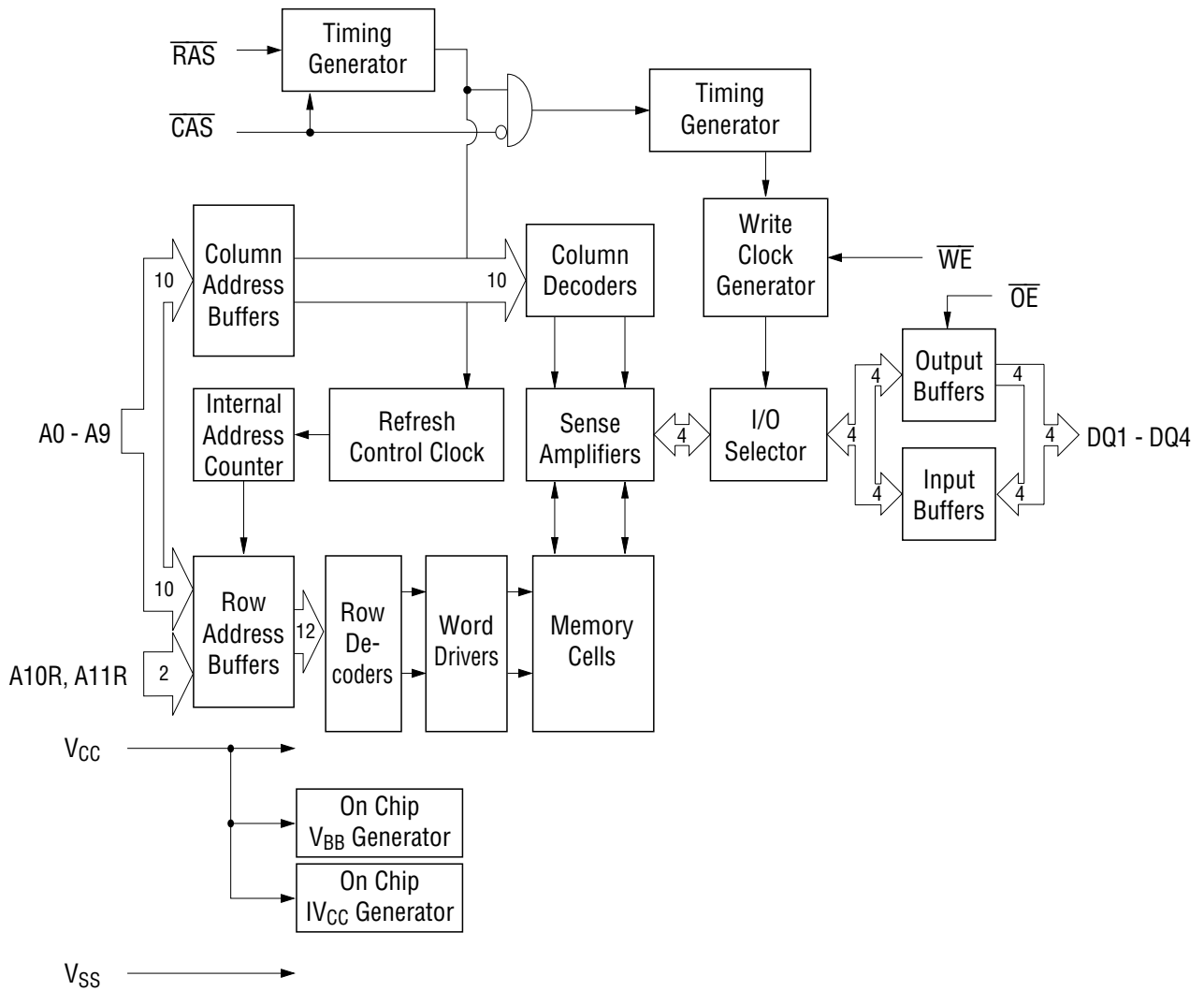


| Pin Name | Function |
|-------------------------|------------------------|
| A0 - A9, A10R, A11R | Address Input |
| $\overline{\text{RAS}}$ | Row Address Strobe |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| DQ1 - DQ4 | Data Input/Data Output |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{WE}}$ | Write Enable |
| V _{CC} | Power Supply (5 V) |
| V _{SS} | Ground (0 V) |

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

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BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|------------------------------------|-------------------------------|------|
| Voltage on Any Pin Relative to V _{SS} | V _{IN} , V _{OUT} | -0.5 to V _{CC} + 0.5 | V |
| Voltage on V _{CC} Supply Relative to V _{SS} | V _{CC} | -0.5 to 7 | V |
| Short Circuit Output Current | I _{OS} | 50 | mA |
| Power Dissipation | P _D * | 1 | W |
| Operating Temperature | T _{opr} | 0 to 70 | °C |
| Storage Temperature | T _{stg} | -55 to 150 | °C |

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|-----------------|--------------------|------|-------------------------------------|------|
| Power Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | — | V _{CC} + 0.5* ¹ | V |
| Input Low Voltage | V _{IL} | -0.5* ² | — | 0.8 | V |

Notes : *1. The input voltage is V_{CC} + 2.0 V when the pulse width is less than 20 ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is V_{SS} - 2.0 V when the pulse width is less than 20 ns (the pulse width is with respect to the point at which V_{SS} is applied).

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|------------------|------|------|------|
| Input Capacitance (A0 - A9, A10R, A11R) | C _{IN1} | — | 5 | pF |
| Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$) | C _{IN2} | — | 7 | pF |
| Output Capacitance (DQ1 - DQ4) | C _{I/O} | — | 7 | pF |

DC Characteristics

($V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ C$ to $70^\circ C$)

| Parameter | Symbol | Condition | MSM5116400 B-50 | | MSM5116400 B-60 | | MSM5116400 B-70 | | Unit | Note |
|--|-----------|--|--------------------|----------|--------------------|----------|--------------------|----------|---------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output High Voltage | V_{OH} | $I_{OH} = -5.0\text{ mA}$ | 2.4 | V_{CC} | 2.4 | V_{CC} | 2.4 | V_{CC} | V | |
| Output Low Voltage | V_{OL} | $I_{OL} = 4.2\text{ mA}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |
| Input Leakage Current | I_{LI} | $0V \leq V_I \leq 6.5V$; All other pins not under test = 0V | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Output Leakage Current | I_{LO} | DQ disable $0V \leq V_O \leq 5.5V$ | -10 | 10 | -10 | 10 | -10 | 10 | μA | |
| Average Power Supply Current (Operating) | I_{CC1} | \overline{RAS} , \overline{CAS} cycling, $t_{RC} = \text{Min.}$ | — | 100 | — | 90 | — | 80 | mA | 1, 2 |
| Power Supply Current (Standby) | I_{CC2} | \overline{RAS} , $\overline{CAS} = V_{IH}$ | — | 2 | — | 2 | — | 2 | mA | 1 |
| | | \overline{RAS} , \overline{CAS} $\geq V_{CC} - 0.2V$ | — | 1 | — | 1 | — | 1 | | |
| Average Power Supply Current (\overline{RAS} -only Refresh) | I_{CC3} | \overline{RAS} cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = \text{Min.}$ | — | 100 | — | 90 | — | 80 | mA | 1, 2 |
| Power Supply Current (Standby) | I_{CC5} | $\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, DQ = enable | — | 5 | — | 5 | — | 5 | mA | 1 |
| Average Power Supply Current (\overline{CAS} before \overline{RAS} Refresh) | I_{CC6} | \overline{RAS} cycling, \overline{CAS} before \overline{RAS} | — | 100 | — | 90 | — | 80 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | I_{CC7} | $\overline{RAS} = V_{IL}$, \overline{CAS} cycling, $t_{PC} = \text{Min.}$ | — | 90 | — | 80 | — | 70 | mA | 1, 3 |

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. The address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3, 11, 12

| Parameter | Symbol | MSM5116400 B-50 | | MSM5116400 B-60 | | MSM5116400 B-70 | | Unit | Note |
|--|-------------------|--------------------|---------|--------------------|---------|--------------------|---------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | t _{RC} | 90 | — | 110 | — | 130 | — | ns | |
| Read Modify Write Cycle Time | t _{RWC} | 131 | — | 155 | — | 185 | — | ns | |
| Fast Page Mode Cycle Time | t _{PC} | 35 | — | 40 | — | 45 | — | ns | |
| Fast Page Mode Read Modify Write Cycle Time | t _{PRWC} | 76 | — | 85 | — | 100 | — | ns | |
| Access Time from $\overline{\text{RAS}}$ | t _{RAC} | — | 50 | — | 60 | — | 70 | ns | 4, 5, 6 |
| Access Time from $\overline{\text{CAS}}$ | t _{CAC} | — | 13 | — | 15 | — | 20 | ns | 4, 5 |
| Access Time from Column Address | t _{AA} | — | 25 | — | 30 | — | 35 | ns | 4, 6 |
| Access Time from $\overline{\text{CAS}}$ Precharge | t _{CPA} | — | 30 | — | 35 | — | 40 | ns | 4 |
| Access Time from $\overline{\text{OE}}$ | t _{OEA} | — | 13 | — | 15 | — | 20 | ns | 4 |
| Output Low Impedance Time from $\overline{\text{CAS}}$ | t _{CLZ} | 0 | — | 0 | — | 0 | — | ns | 4 |
| $\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time | t _{OFF} | 0 | 13 | 0 | 15 | 0 | 20 | ns | 7 |
| $\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time | t _{OEZ} | 0 | 13 | 0 | 15 | 0 | 20 | ns | 7 |
| Transition Time | t _T | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | t _{REF} | — | 64 | — | 64 | — | 64 | ms | |
| $\overline{\text{RAS}}$ Precharge Time | t _{RP} | 30 | — | 40 | — | 50 | — | ns | |
| $\overline{\text{RAS}}$ Pulse Width | t _{RAS} | 50 | 10,000 | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode) | t _{RASP} | 50 | 100,000 | 60 | 100,000 | 70 | 100,000 | ns | |
| $\overline{\text{RAS}}$ Hold Time | t _{RSH} | 13 | — | 15 | — | 20 | — | ns | |
| $\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$ | t _{ROH} | 13 | — | 15 | — | 20 | — | ns | |
| $\overline{\text{CAS}}$ Precharge Time (Fast Page Mode) | t _{CP} | 7 | — | 10 | — | 10 | — | ns | |
| $\overline{\text{CAS}}$ Pulse Width | t _{CAS} | 13 | 10,000 | 15 | 10,000 | 20 | 10,000 | ns | |
| $\overline{\text{CAS}}$ Hold Time | t _{CSH} | 50 | — | 60 | — | 70 | — | ns | |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | t _{CRP} | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | t _{RHCP} | 30 | — | 35 | — | 40 | — | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | t _{RCD} | 17 | 37 | 20 | 45 | 20 | 50 | ns | 5 |
| $\overline{\text{RAS}}$ to Column Address Delay Time | t _{RAD} | 12 | 25 | 15 | 30 | 15 | 35 | ns | 6 |
| Row Address Set-up Time | t _{ASR} | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | t _{RAH} | 7 | — | 10 | — | 10 | — | ns | |
| Column Address Set-up Time | t _{ASC} | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | t _{CAH} | 7 | — | 15 | — | 15 | — | ns | |
| Column Address to $\overline{\text{RAS}}$ Lead Time | t _{RAL} | 25 | — | 30 | — | 35 | — | ns | |
| Read Command Set-up Time | t _{RCS} | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time | t _{RCH} | 0 | — | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{\text{RAS}}$ | t _{RRH} | 0 | — | 0 | — | 0 | — | ns | 8 |

AC Characteristics (2/2)

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C) Note 1, 2, 3, 11, 12

| Parameter | Symbol | MSM5116400 B-50 | | MSM5116400 B-60 | | MSM5116400 B-70 | | Unit | Note |
|---|------------|--------------------|------|--------------------|------|--------------------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Write Command Set-up Time | t_{WCS} | 0 | — | 0 | — | 0 | — | ns | 9 |
| Write Command Hold Time | t_{WCH} | 7 | — | 10 | — | 15 | — | ns | |
| Write Command Pulse Width | t_{WP} | 7 | — | 10 | — | 10 | — | ns | |
| \overline{OE} Command Hold Time | t_{OEHL} | 13 | — | 15 | — | 20 | — | ns | |
| Write Command to \overline{RAS} Lead Time | t_{RWL} | 13 | — | 15 | — | 20 | — | ns | |
| Write Command to \overline{CAS} Lead Time | t_{CWL} | 13 | — | 15 | — | 20 | — | ns | |
| Data-in Set-up Time | t_{DS} | 0 | — | 0 | — | 0 | — | ns | 10 |
| Data-in Hold Time | t_{DH} | 7 | — | 10 | — | 15 | — | ns | 10 |
| \overline{OE} to Data-in Delay Time | t_{OED} | 13 | — | 15 | — | 20 | — | ns | |
| \overline{CAS} to \overline{WE} Delay Time | t_{CWD} | 36 | — | 40 | — | 50 | — | ns | 9 |
| Column Address to \overline{WE} Delay Time | t_{AWD} | 48 | — | 55 | — | 65 | — | ns | 9 |
| \overline{RAS} to \overline{WE} Delay Time | t_{RWD} | 73 | — | 85 | — | 100 | — | ns | 9 |
| \overline{CAS} Precharge \overline{WE} Delay Time | t_{CPWD} | 53 | — | 60 | — | 70 | — | ns | 9 |
| \overline{CAS} Active Delay Time from \overline{RAS} Precharge | t_{RPC} | 5 | — | 5 | — | 5 | — | ns | |
| \overline{RAS} to \overline{CAS} Set-up Time (\overline{CAS} before \overline{RAS}) | t_{CSR} | 10 | — | 10 | — | 10 | — | ns | |
| \overline{RAS} to \overline{CAS} Hold Time (\overline{CAS} before \overline{RAS}) | t_{CHR} | 10 | — | 10 | — | 10 | — | ns | |
| \overline{WE} to \overline{RAS} Precharge Time (\overline{CAS} before \overline{RAS}) | t_{WRP} | 10 | — | 10 | — | 10 | — | ns | |
| \overline{WE} Hold Time from \overline{RAS} (\overline{CAS} before \overline{RAS}) | t_{WRH} | 10 | — | 10 | — | 10 | — | ns | |
| \overline{RAS} to \overline{WE} Set-up Time (Test Mode) | t_{WTS} | 10 | — | 10 | — | 10 | — | ns | |
| \overline{RAS} to \overline{WE} Hold Time (Test Mode) | t_{WTH} | 10 | — | 10 | — | 10 | — | ns | |

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 11. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 4-bit locations. Since all 4 DQ pins are used, a total of 16 data bits can be written in parallel into the memory array. In a read cycle, if 4 data bits are equal, the DQ pin will indicate a high level. If the 4 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

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See ADDENDUM F for AC Timing Waveforms