

## MSM5116400D

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

### DESCRIPTION

The MSM5116400D is a 4,194,304-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5116400D achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5116400D is available in a 26/24-pin plastic SOJ, 26/24-pin plastic TSOP.

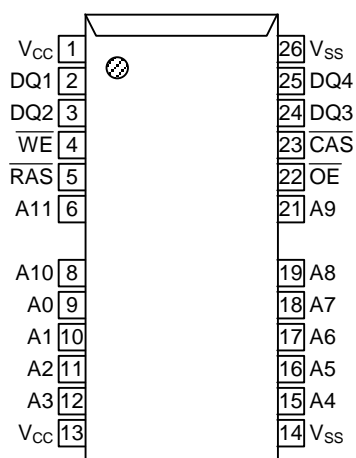
### FEATURES

- 4,194,304-word × 4-bit configuration
  - Single 5V power supply, ±10% tolerance
  - Input : TTL compatible, low input capacitance
  - Output : TTL compatible, 3-state
  - Refresh : 4096 cycles/64 ms
  - Fast page mode, read modify write capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
  - Multi-bit test mode capability
  - Package options:
    - 26/24-pin 300mil plastic SOJ (SOJ26/24-P-300-1.27) (Product : MSM5116400D-xxSJ)
    - 26/24-pin 300mil plastic TSOP (TSOPII26/24-P-300-1.27-K) (Product : MSM5116400D-xxTS-K)
- xx : indicates speed rank.

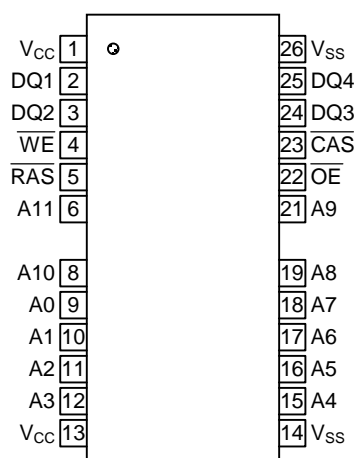
### PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM5116400D-50	50ns	25ns	13ns	13ns	90ns	413mW	5.5mW
MSM5116400D-60	60ns	30ns	15ns	15ns	110ns	385mW	
MSM5116400D-70	70ns	35ns	20ns	20ns	130ns	358mW	

## PIN CONFIGURATION (TOP VIEW)

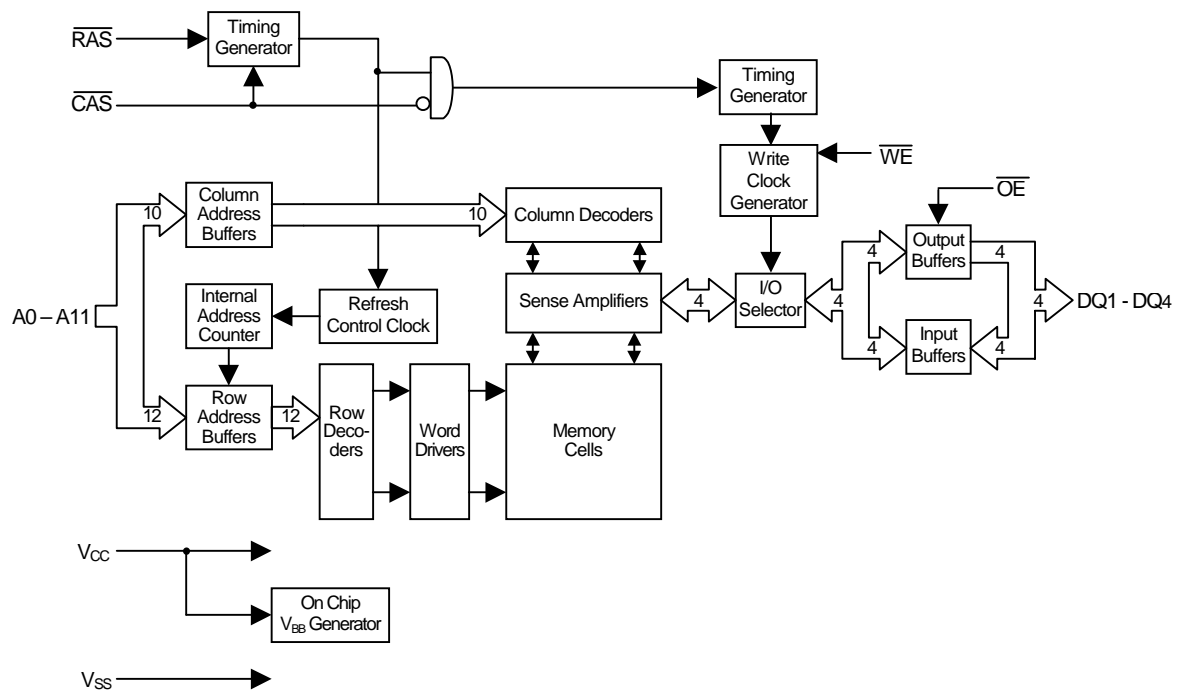


26/24-Pin Plastic SOJ

26/24-Pin Plastic TSOP  
(K Type)

Pin Name	Function
A0–A11	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1–DQ4	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V <sub>CC</sub>	Power Supply (5V)
V <sub>SS</sub>	Ground (0V)
NC	No Connection

## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_T$	-0.5 to 7.0	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^\circ\text{C}$

### Recommended Operating Conditions

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	$V_{IL}$	$-0.5^{*2}$	—	0.8	V

Notes: \*1. The input voltage is  $V_{CC} + 2.0\text{V}$  when the pulse width is less than 20ns (the pulse width is with respect to the point at which  $V_{CC}$  is applied).

\*2. The input voltage is  $V_{SS} - 2.0\text{V}$  when the pulse width is less than 20ns (the pulse width respect to the point at which  $V_{SS}$  is applied).

### Capacitance

( $V_{CC} = 5.0\text{V} \pm 10\%$ ,  $T_a = 25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 – A11)	$C_{IN1}$	—	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{IN2}$	—	7	pF
Output Capacitance (DQ1 – DQ4)	$C_{I/O}$	—	7	pF

## DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ C \text{ to } 70^\circ C)$ 

Parameter	Symbol	Condition	MSM5116400 D-50		MSM5116400 D-60		MSM5116400 D-70		Unit	Note
			Min.	Max	Min.	Max	Min.	Max		
Output High Voltage	$V_{OH}$	$I_{OH} = -5.0mA$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2mA$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0V \leq V_I \leq 6.5V$ ; All other pins not under test = 0V	-10	10	-10	10	-10	10	$\mu A$	
Output Leakage Current	$I_{LO}$	DQ disable $0V \leq V_O \leq V_{CC}$	-10	10	-10	10	-10	10	$\mu A$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = \text{Min.}$	—	75	—	70	—	65	mA	1,2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{RAS}$ , $\overline{CAS} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{RAS}$ , $\overline{CAS} \geq V_{CC} - 0.2V$	—	0.5	—	0.5	—	0.5		
Average Power Supply Current ( $\overline{RAS}$ -only Refresh)	$I_{CC3}$	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	75	—	70	—	65	mA	1,2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{RAS} = V_{IH}$ , $\overline{CAS} = V_{IL}$ , DQ = enable	—	2	—	2	—	2	mA	1
Average Power Supply Current ( $\overline{CAS}$ before $\overline{RAS}$ Refresh)	$I_{CC6}$	$\overline{RAS} = \text{cycling}$ , $\overline{CAS}$ before $\overline{RAS}$	—	75	—	70	—	65	mA	1,2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling, $t_{PC} = \text{Min.}$	—	70	—	65	—	60	mA	1,3

- Notes: 1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.  
2. The address can be changed once or less while  $\overline{RAS} = V_{IL}$ .  
3. The address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

## AC Characteristic (1/2)

(V<sub>CC</sub> = 5V ± 10%, Ta = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM5116400 D-50		MSM5116400 D-60		MSM5116400 D-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	76	—	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	50	—	60	—	70	ns	4,5,6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	13	—	15	—	20	ns	4,5
Access Time from Column Address	t <sub>AA</sub>	—	25	—	30	—	35	ns	4,6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	30	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	13	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	13	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	64	—	64	—	64	m	
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	13	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t <sub>ROH</sub>	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t <sub>CP</sub>	7	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	13	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t <sub>RHCP</sub>	30	—	35	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	17	37	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	12	25	15	30	15	35	ns	
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	7	—	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	

## AC Characteristic (2/2)

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0°C to 70°C) Note1,2,3

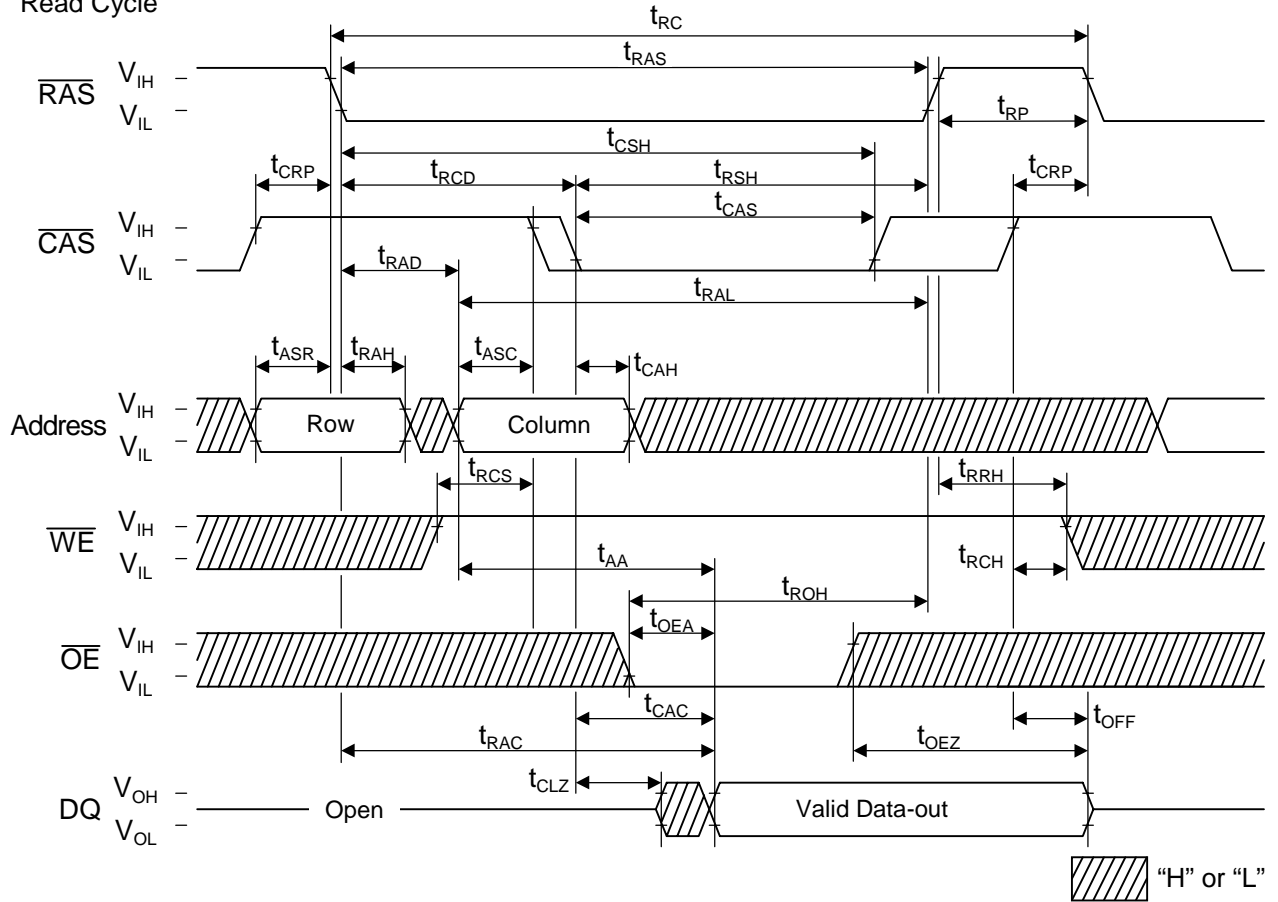
Parameter	Symbol	MSM5116400 D-50		MSM5116400 D-60		MSM5116400 D-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Column Address Hold Time	t <sub>CAH</sub>	7	—	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	25	—	30	—	35	—	ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	9
Write Command Hold Time	t <sub>WCH</sub>	7	—	10	—	15	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OEH</sub>	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	13	—	15	—	20	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	10
Data-in Hold Time	t <sub>DH</sub>	7	—	10	—	15	—	ns	10
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>OED</sub>	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	36	—	40	—	50	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	48	—	55	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	73	—	85	—	100	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	53	—	60	—	70	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	10	—	10	—	ns	

- Notes:
1. A start-up delay of 200 $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5\text{ns}$ .
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2 TTL load and 100pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  10. These parameters are referenced to the  $\overline{\text{CAS}}$  leading edge in an early write cycle, and to the  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle, or a read modify write cycle.

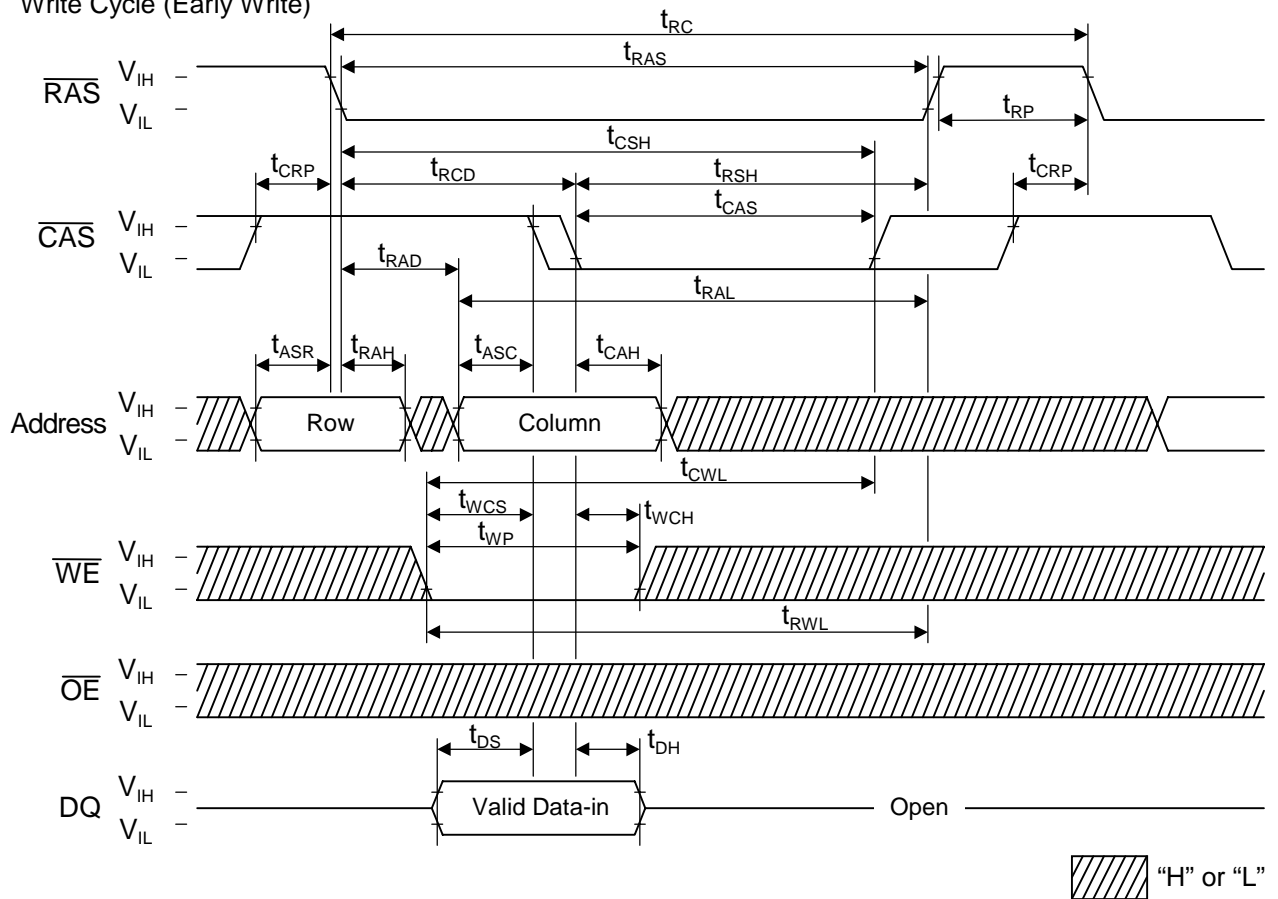


# Timing Chart

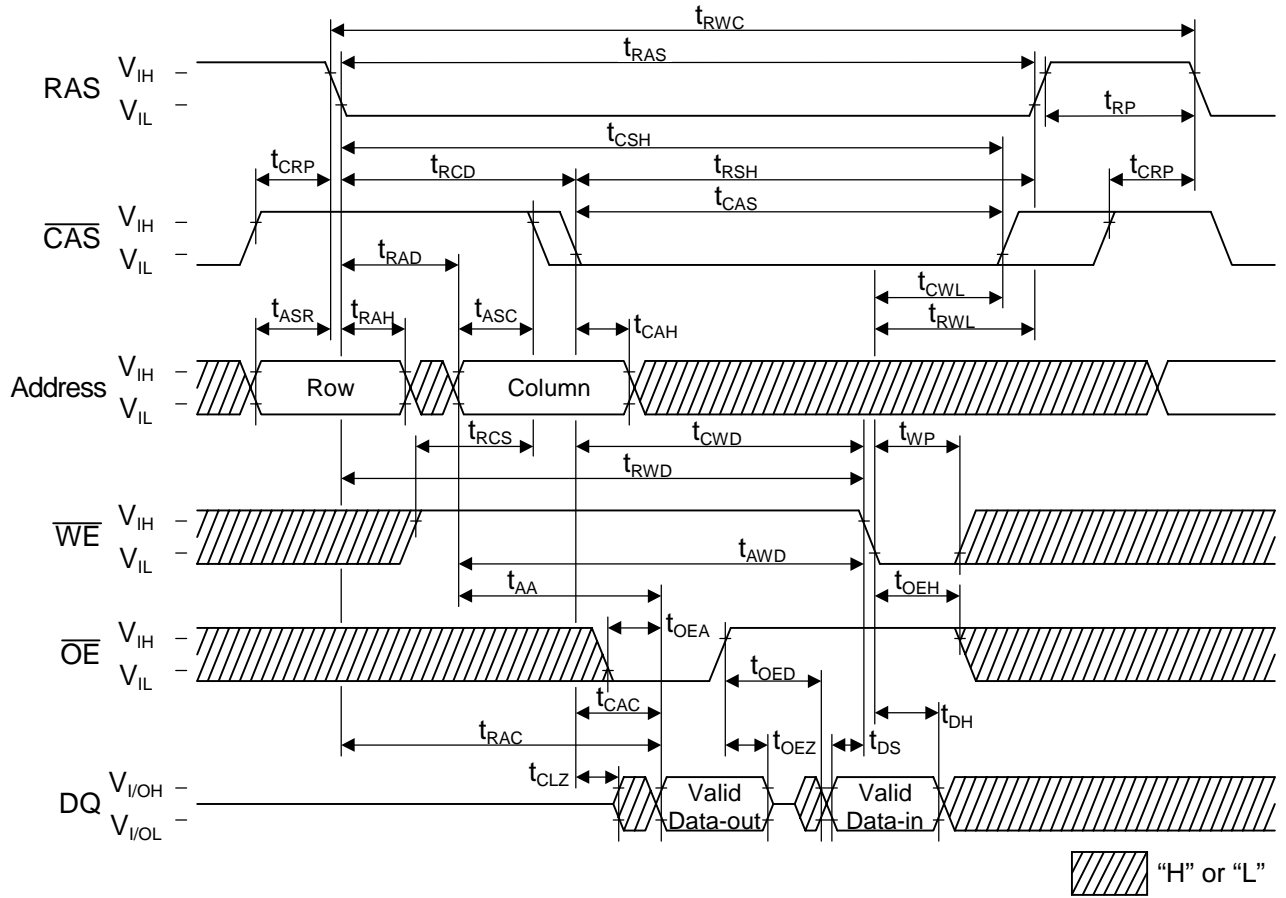
- Read Cycle



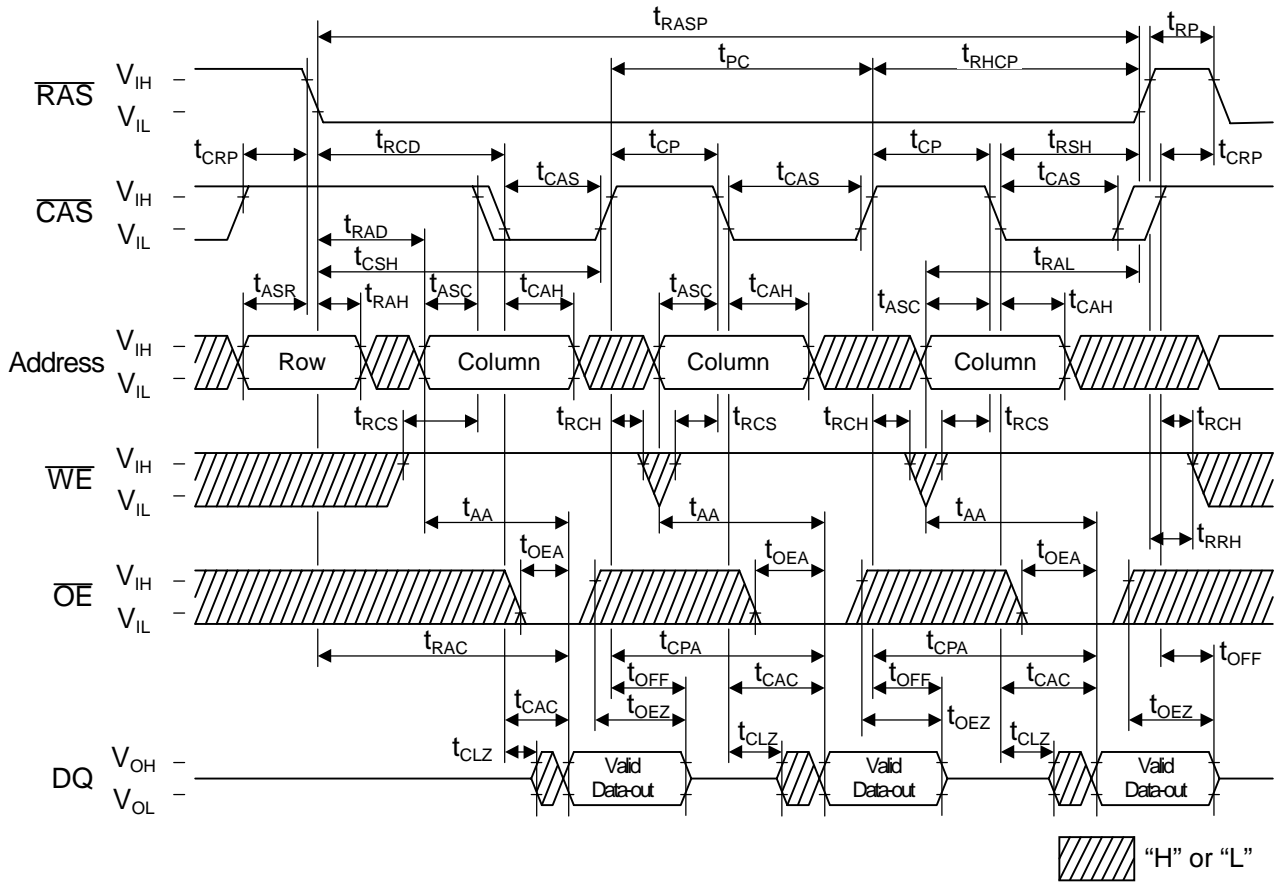
- Write Cycle (Early Write)



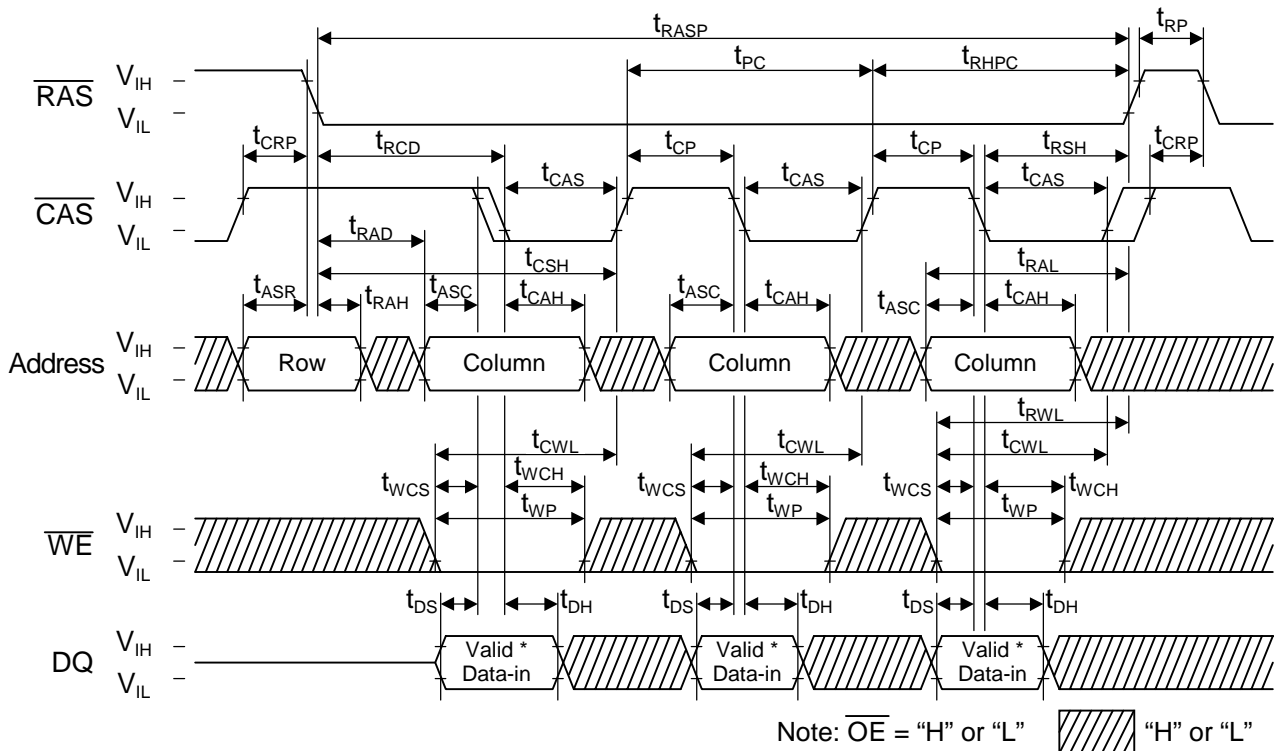
• Read Modify Write Cycle



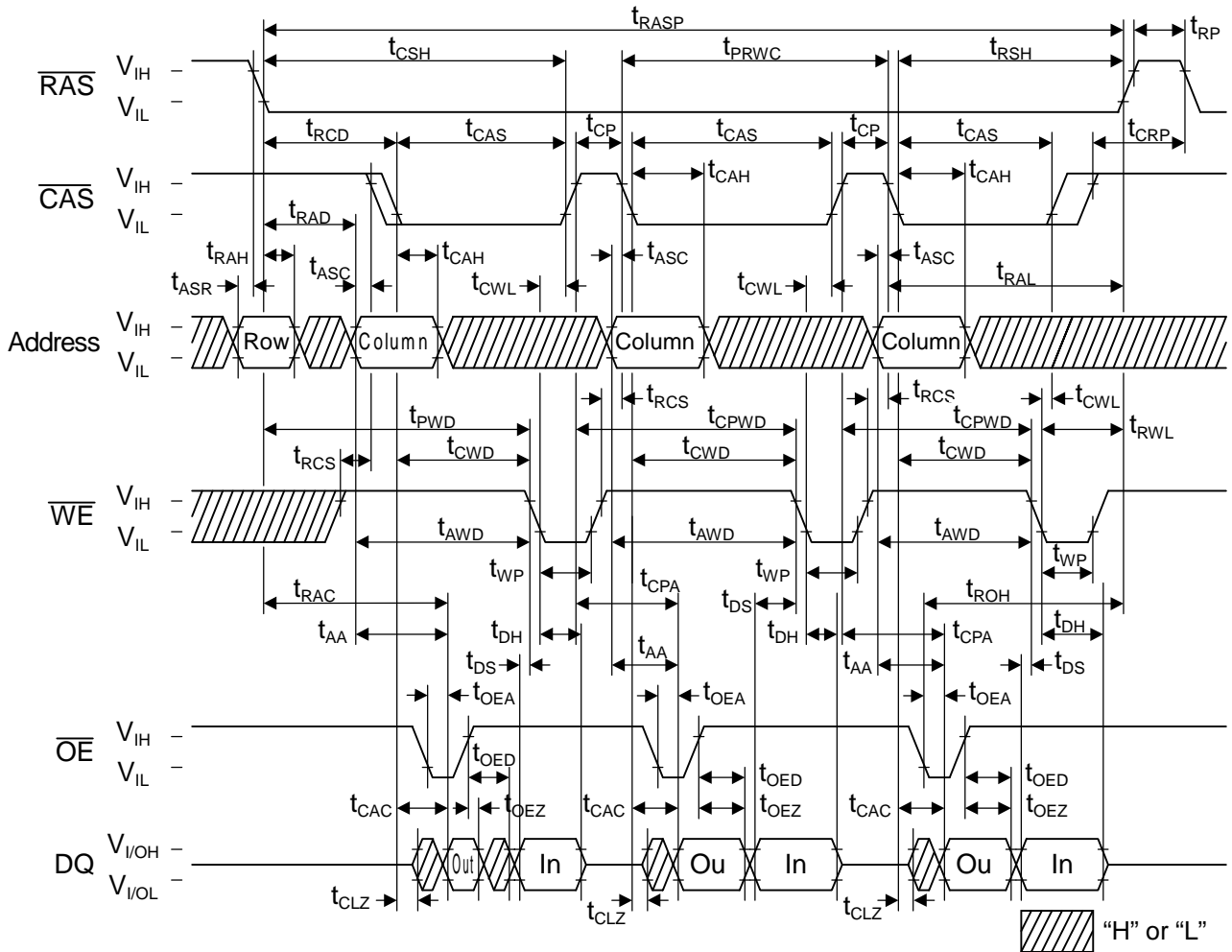
• Fast Page Mode Cycle



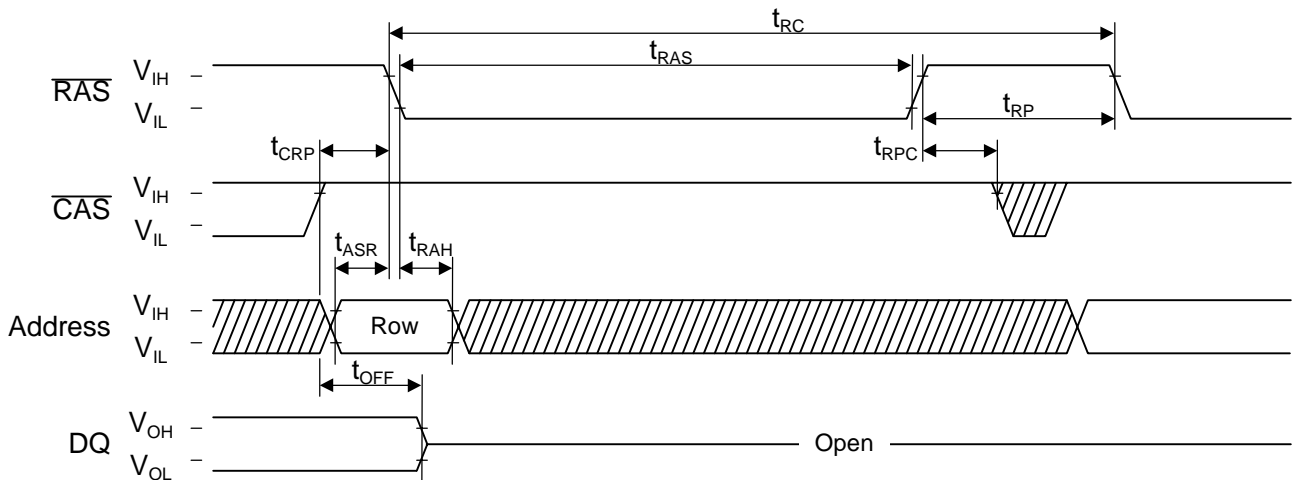
• Fast Page Mode Write Cycle (Early Write)



• Fast Page Mode Read Modify Write Cycle

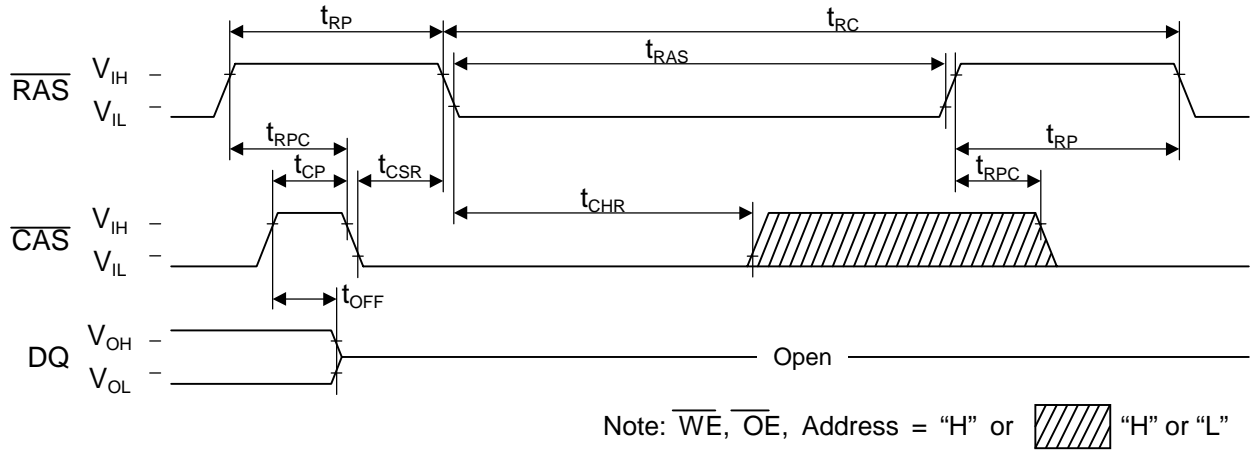


•  $\overline{\text{RAS}}$ -only Refresh Cycle

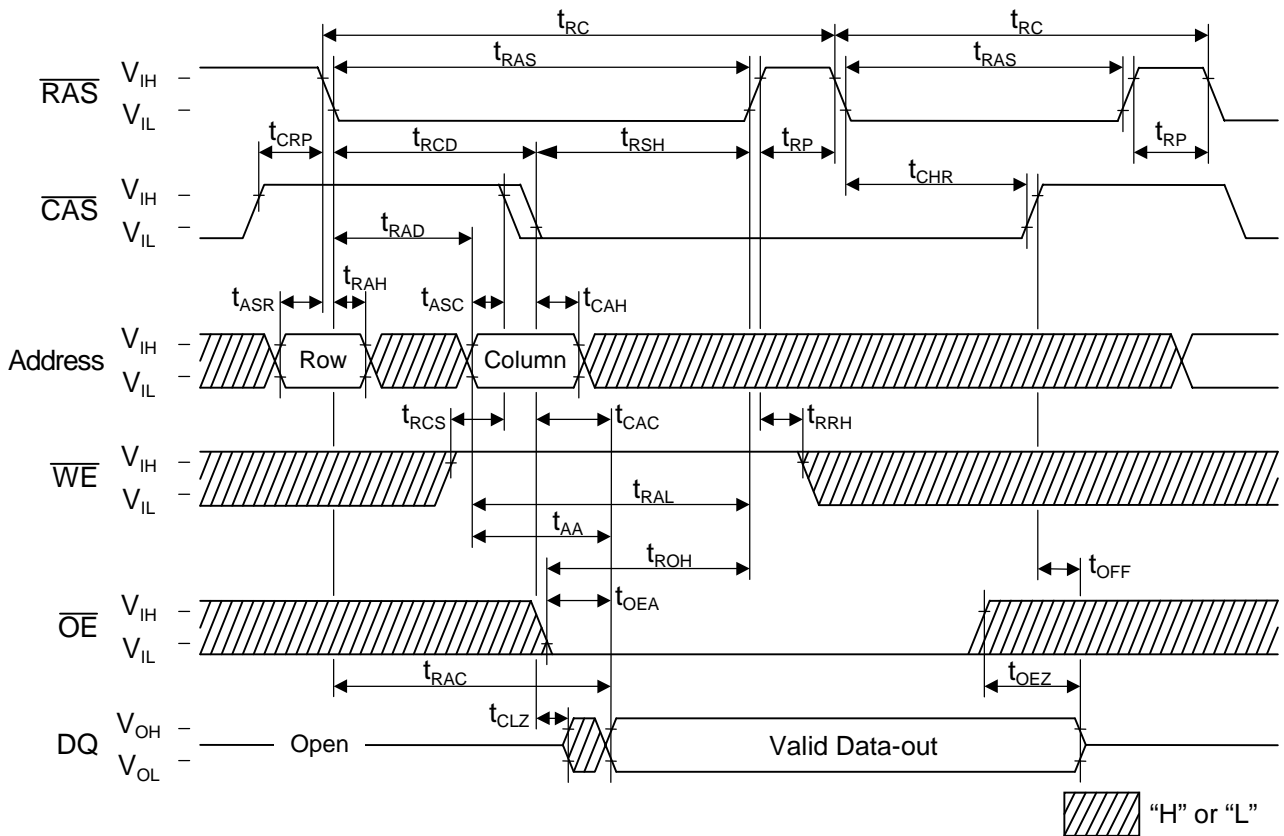


Note:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  = "H" or "H" or "L"

•  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh Cycle



• Hidden Refresh Read Cycle



Hidden Refresh Write Cycle

