Preliminary

# OKI Semiconductor

# MSM5117100

## 16 Meg x 1-Bit DYNAMIC RAM

### DESCRIPTION

The MSM5117100 is a 16 Megabit dynamic memory organized as 16,777,216 word by 1 bit. The technology used to fabricate the MSM5117100 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. All inputs and outputs are TTL compatible. This 16-Meg DRAM can be used for high end PC's & work stations which need high density main memory.

### FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- **16 Meg density: 16Mx1**
- 400mil 28 pin plastic SOJ, 400mil 28 pin plastic TSOP
- Single +5V Supply, ±10% tolerance
- Input : TTL compatible
- Output: TTL compatible, tri-state, non-latch
- **Refresh: 2048 cycles/32ms: provides backward compatibility with 4-Meg sockets.**
- Read Modify Write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Fast Page Mode capability
- Multi bit test mode capability
- Built-in $V_{BB}$ generator circuit
- Package
  28PIN PLASTIC SOJ (SOJ28-P-400)
  28PIN PLASTIC TSOP (TSOP28-P-400-K)
  (TSOP28-P-400-L)

### MSM5117100 FAMILY

| Family | Access Time (Max.) | | | Cycle Time (Min.) | Power Dissipation (Max.) | |
|---|---|---|---|---|---|---|
| | $t_{RAC}$ | $t_{AA}$ | $t_{CAC}$ | | Operating | Standby |
| MSM5117100 - 60JS/TK/TL | 60ns | 30ns | 15ns | 110ns | 660mW | 5.5mW (MOS level) |
| MSM5117100 - 70JS/TK/TL | 70ns | 35ns | 20ns | 130ns | 605mW | |
| MSM5117100 - 80JS/TK/TL | 80ns | 40ns | 20ns | 150ns | 550mW | |

JS ; SOJ / TK ; TSOP(NORMAL) / TL ; TSOP (REVERSE)

## PIN CONFIGURATION (TOP VIEW)

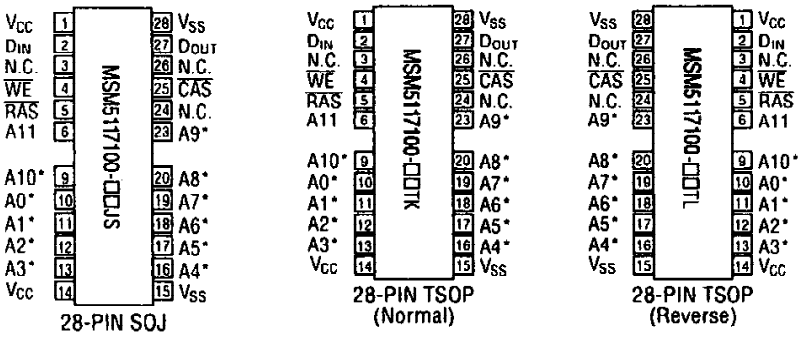


**Figure 1. Pin Configuration**

| Pin Names | Function |
|---|---|
| A0~A11 | Address Input |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power Supply (+5V) |
| $V_{SS}$ | Ground (0V) |
| N.C. | No Connection |

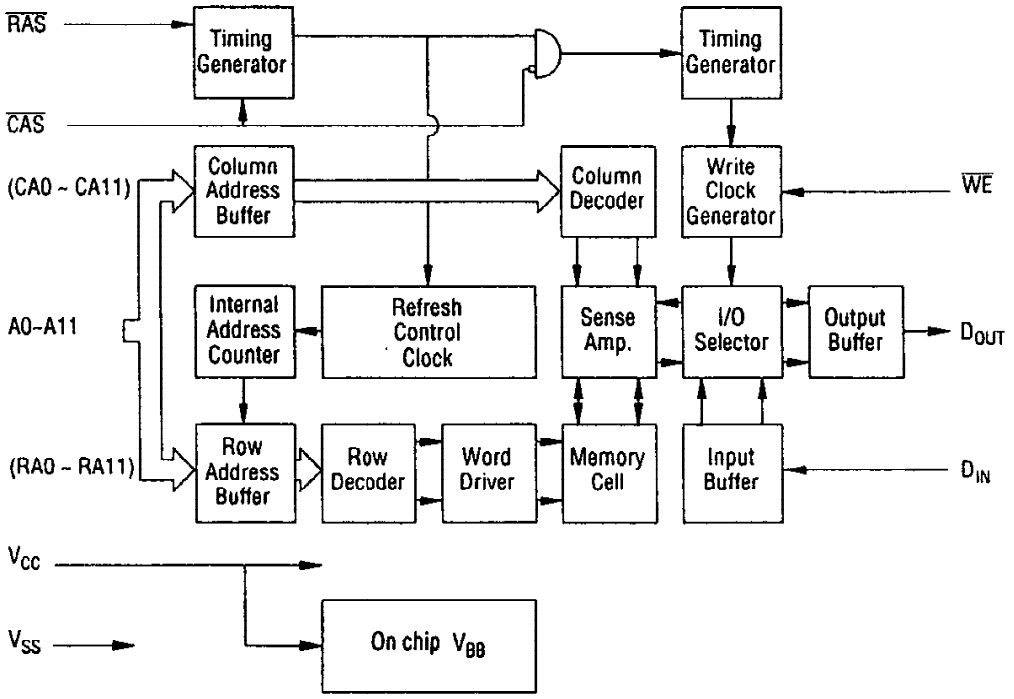


**Figure 2. Block Diagram**

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Voltage on any Pin Relative to $V_{SS}$ | $V_T$ | Ta = 25°C | -1.0 ~ +7.0 | V |
| Short Circuit Output Current | $I_{OS}$ | Ta = 25°C | 50 | mA |
| Power Dissipation | $P_D$ | Ta = 25°C | 1 | W |
| Operating Temperature | $T_{opr}$ | — | 0 ~ +70 | °C |
| Storage Temperature | $T_{stg}$ | — | -55 ~ +150 | °C |

### Recommended Operating Conditions (Ta = 0 ~ 70°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | — | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | — | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | — | 2.4 | — | 6.5 | V |
| Input Low Voltage | $V_{IL}$ | — | -1.0 | — | 0.8 | V |

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to $V_{SS}$.

## DC Characteristics ($V_{CC}$ = 5.0 V ± 10%, Ta = 0 ~ +70°C)

| Parameter | Symbol | Condition | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -5.0mA | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | — |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.2mA | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | — |
| Input Leakage Current | $I_{LI}$ | 0V ≤ $V_I$ ≤ 6.5V<br>All other pins not under test = 0V | -10 | 10 | -10 | 10 | -10 | 10 | µA | — |
| Output Leakage Current | $I_{LO}$ | $D_{OUT}$ disable<br>0V ≤ $V_O$ ≤ 5.5V | -10 | 10 | -10 | 10 | -10 | 10 | µA | — |
| Average Power Supply Current (Operating) | $I_{CC1}$ | $\overline{RAS}$, $\overline{CAS}$ cycling<br>$t_{RC}$ = min. | — | 120 | — | 110 | — | 100 | mA | 1, 2 |
| Power Supply Current (Standby) | $I_{CC2}$ | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IH}$<br>$D_{OUT}$ = HZ | — | 2 | — | 2 | — | 2 | mA | TTL |
| Average Power Supply Current ($\overline{RAS}$ only Refresh) | $I_{CC3}$ | $\overline{RAS}$ cycling<br>$\overline{CAS}$ = $V_{IH}$<br>$t_{RC}$ = min. | — | 120 | — | 110 | — | 100 | mA | 2 |
| Power Supply Current (Standby) | $I_{CC5}$ | $\overline{RAS}$ = $V_{CC}$ -0.2V<br>$\overline{CAS}$ = $V_{CC}$ -0.2V<br>$D_{OUT}$ = HZ | — | 1 | — | 1 | — | 1 | mA | MOS |
| Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $I_{CC6}$ | $\overline{RAS}$ cycling<br>$\overline{CAS}$ before $\overline{RAS}$ | — | 120 | — | 110 | — | 100 | mA | 1 |
| Average Power Supply Current (Fast Page Mode) | $I_{CC7}$ | $\overline{RAS}$ = $V_{IL}$<br>$\overline{CAS}$ cycling<br>$t_{PC}$ = min. | — | 110 | — | 100 | — | 90 | mA | 1, 3 |

Notes: 1. $I_{CC}$ is dependent on output loading and cycle rates.
Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.

## Capacitance ($V_{CC}$ = 5.0 V ± 10%, Ta = 25°C, f = 1MHz)

| Parameter | Symbol | Condition | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Capacitance (A0 to A11, $D_{IN}$) | $C_{IN1}$ | — | — | 6 | pF |
| Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | $C_{IN2}$ | — | — | 7 | pF |
| Output Capacitance ($D_{OUT}$) | $C_{OUT}$ | — | — | 7 | pF |

## AC Characteristics ($V_{CC}$ = 5.0 V ± 10%, Ta = 0 ~ +70°C)

(For the following tables under the AC Characteristics, please refer to the Notes listed on page 13.)

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 110 | — | 130 | — | 150 | — | ns | — |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | — |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 60 | 10000 | 70 | 10000 | 80 | 10000 | ns | — |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 15 | 10000 | 20 | 10000 | 20 | 10000 | ns | — |
| Row Address Set-up Time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Row Address Hold Time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | — |
| Column Address Set-up Time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Column Address Hold Time | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | ns | — |
| Column Address Hold Time referenced to $\overline{RAS}$ | $t_{AR}$ | 50 | — | 55 | — | 60 | — | ns | — |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 20 | 45 | 20 | 50 | 20 | 60 | ns | 5 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 6 |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 15 | — | 20 | — | 20 | — | ns | — |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 60 | — | 70 | — | 80 | — | ns | — |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| Transition Time | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | $t_{REF}$ | — | 32 | — | 32 | — | 32 | ms | — |

## Read Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 4, 5 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | — | 15 | — | 20 | — | 20 | ns | 4, 5 |
| Access Time from Column Address | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 4, 6 |
| Read Command Set-up Time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Read Command Hold Time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 8 |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | — |
| $\overline{CAS}$ to Output in Low-Z | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | 4 |
| Output Buffer Turn-off Delay | $t_{OFF}$ | 0 | 15 | 0 | 20 | 0 | 20 | ns | 7 |

## Write Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Write Command Set-up Time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 9 |
| Write Command Hold Time | $t_{WCH}$ | 10 | — | 15 | — | 15 | — | ns | — |
| Write Command Hold Time referenced to $\overline{RAS}$ | $t_{WCR}$ | 45 | — | 55 | — | 60 | — | ns | — |
| Write Command Pulse Width | $t_{WP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 15 | — | 20 | — | 20 | — | ns | — |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 15 | — | 20 | — | 20 | — | ns | — |
| Data Set-up Time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Data Hold Time | $t_{DH}$ | 15 | — | 15 | — | 15 | — | ns | — |
| Data Hold Time referenced to $\overline{RAS}$ | $t_{DHR}$ | 50 | — | 55 | — | 60 | — | ns | — |

## Read/Write Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read/Write Cycle Time | $t_{RWC}$ | 130 | — | 155 | — | 175 | — | ns | — |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 60 | — | 70 | — | 80 | — | ns | 9 |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 15 | — | 20 | — | 20 | — | ns | 9 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 30 | — | 35 | — | 40 | — | ns | 9 |

## Refresh Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CSR}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CHR}$ | 20 | — | 20 | — | 20 | — | ns | — |
| $\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | $t_{RPC}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{CAS}$ Precharge Time | $t_{CPN}$ | 10 | — | 10 | — | 10 | — | ns | — |

## Fast Page Mode Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Fast Page Mode Cycle time | $t_{PC}$ | 40 | — | 45 | — | 50 | — | ns | — |
| $\overline{CAS}$ Precharge Time (Fast Page Mode) | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{RAS}$ Pulse Width (Fast Page Mode) | $t_{RASP}$ | 60 | 100000 | 70 | 100000 | 80 | 100000 | ns | — |
| Access Time from $\overline{CAS}$ Precharge | $t_{CPA}$ | — | 35 | — | 40 | — | 45 | ns | 4 |
| $\overline{RAS}$ Hold Time referenced to $\overline{CAS}$ Precharge | $t_{RHCP}$ | 35 | — | 40 | — | 45 | — | ns | — |

## Fast Page Mode Read /Write Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Fast Page Mode Read/Write Cycle Time | $t_{PRWC}$ | 60 | — | 70 | — | 75 | — | ns | — |
| $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | $t_{CPW}$ | 35 | — | 40 | — | 45 | — | ns | 9 |

## Counter Test Cycle

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test) | $t_{CPT}$ | 40 | — | 40 | — | 40 | — | ns | — |

## Read,Write, Read/Write Refresh Cycle In the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 115 | — | 135 | — | 155 | — | ns | — |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | — |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 65 | 10000 | 75 | 10000 | 85 | 10000 | ns | — |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 20 | 10000 | 25 | 10000 | 25 | 10000 | ns | — |
| Row Address Set-up Time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Row Address Hold Time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | — |
| Column Address Set-up Time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Column Address Hold Time | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | ns | — |
| Column Address Hold Time referenced to $\overline{RAS}$ | $t_{AR}$ | 50 | — | 55 | — | 60 | — | ns | — |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 20 | 45 | 20 | 50 | 20 | 60 | ns | 5 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 6 |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 20 | — | 25 | — | 25 | — | ns | — |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 65 | — | 75 | — | 85 | — | ns | — |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| Transition Time | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | $t_{REF}$ | — | 32 | — | 32 | — | 32 | ms | — |

## Read Cycle in the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 65 | — | 75 | — | 85 | ns | 4, 5 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | — | 20 | — | 25 | — | 25 | ns | 4,5 |
| Access Time from Column Address | $t_{AA}$ | — | 35 | — | 40 | — | 45 | ns | 4,6 |
| Read Command Set-up Time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Read Command Hold Time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 8 |
| Column Addres to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 35 | — | 40 | — | 45 | — | ns | — |
| $\overline{CAS}$ to Output in Low-Z | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | 4 |
| Output Buffer Turn-off Delay | $t_{OFF}$ | 0 | 15 | 0 | 20 | 0 | 20 | ns | 7 |

## Write Cycle in the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Write Command Set-up Time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 9 |
| Write Command Hold Time | $t_{WCH}$ | 10 | — | 15 | — | 15 | — | ns | — |
| Write Command Hold Time referenced to $\overline{RAS}$ | $t_{WCR}$ | 45 | — | 55 | — | 60 | — | ns | — |
| Write Command Pulse Width | $t_{WP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 15 | — | 20 | — | 20 | — | ns | — |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 15 | — | 20 | — | 20 | — | ns | — |
| Data Set-up Time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | — |
| Data Hold Time | $t_{DH}$ | 15 | — | 15 | — | 15 | — | ns | — |
| Data Hold Time referenced to $\overline{RAS}$ | $t_{DHR}$ | 50 | — | 55 | — | 60 | — | ns | — |

## Read/Write Cycle in the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read/Write Cycle Time | $t_{RWC}$ | 135 | — | 160 | — | 180 | — | ns | — |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 65 | — | 75 | — | 85 | — | ns | 9 |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 20 | — | 25 | — | 25 | — | ns | 9 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 35 | — | 40 | — | 45 | — | ns | 9 |

## Refresh Cycle in the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CSR}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CHR}$ | 20 | — | 20 | — | 20 | — | ns | — |
| $\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | $t_{RPC}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{CAS}$ Precharge Time | $t_{CPN}$ | 10 | — | 10 | — | 10 | — | ns | — |

## Fast Page Mode Cycle in the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Fast Page Mode Cycle time | $t_{PC}$ | 45 | — | 50 | — | 55 | — | ns | — |
| $\overline{CAS}$ Precharge Time (Fast Page Mode) | $t_{CP}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{RAS}$ Pulse Width (Fast Page Mode) | $t_{RASP}$ | 65 | 100000 | 75 | 100000 | 85 | 100000 | ns | — |
| Access Time from $\overline{CAS}$ Precharge | $t_{CPA}$ | — | 40 | — | 45 | — | 50 | ns | 4 |
| $\overline{RAS}$ Hold Time referenced to $\overline{CAS}$ Precharge | $t_{RHCP}$ | 40 | — | 45 | — | 50 | — | ns | — |

## Fast Page Mode Read /Write Cycle In the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Fast Page Mode Read/Write Cycle Time | $t_{PRWC}$ | 65 | — | 75 | — | 80 | — | ns | — |
| $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | $t_{CPW}$ | 40 | — | 45 | — | 50 | — | ns | 9 |

## Test Mode Cycle In the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $\overline{WE}$ Set-up Time | $t_{WSR}$ | 10 | — | 10 | — | 10 | — | ns | — |
| $\overline{WE}$ Hold Time | $t_{WHR}$ | 20 | — | 20 | — | 20 | — | ns | — |

## Counter Test Cycle In the Test Mode

| Parameter | Symbol | MSM 5117100-60 JS/TK/TL | | MSM 5117100-70 JS/TK/TL | | MSM 5117100-80 JS/TK/TL | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test) | $t_{CPT}$ | 40 | — | 40 | — | 40 | — | ns | — |

Notes : 1. An initial pause of 200μs is required after power-up, followed by 8 $\overline{RAS}$ cycles before the proper device operation is achieved. In the case of using an internal refresh counter, a minimum of 8 $\overline{CAS}$ cycles before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2. AC measurements assume $t_T$ = 5ns

3. $V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring the timing of input signals. Also transition times are measured between $V_{IH}$ and $V_{IL}$.

4. Measured with a load circuit equivalent to 2 TLL loads and 100pF.

5. Operation within the $t_{RCD}$(max.) limit insures that $t_{RAC}$(max.) can be met. $t_{RCD}$(max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max.) limit, then the access time is controlled by $t_{CAC}$.

6. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit , then the access time is controlled by tAA.

7. $t_{OFF}$(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

9. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WSC} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain as an open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPW} \geq t_{CPW}$(min.), then the cycle is a read/write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

10. $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ Cycle (Test mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". In "Test Mode", the RAM is internally organized by 512K words by 32 bits, and data is written into 32 sectors in parallel and is retrieved the same way. A0 (Column), A1 (Column), A10 (Column), A11 (Row), A11 (Column) are not used. If upon reading, all bits are equal ( all "H"s or "L"s), the data output pin indicates an "H". If any of the bits differed, the data output pin would indicate an "L". In "Test Mode", the16M x 1 DRAM can be tested as if it were a 512K x 1 DRAM.

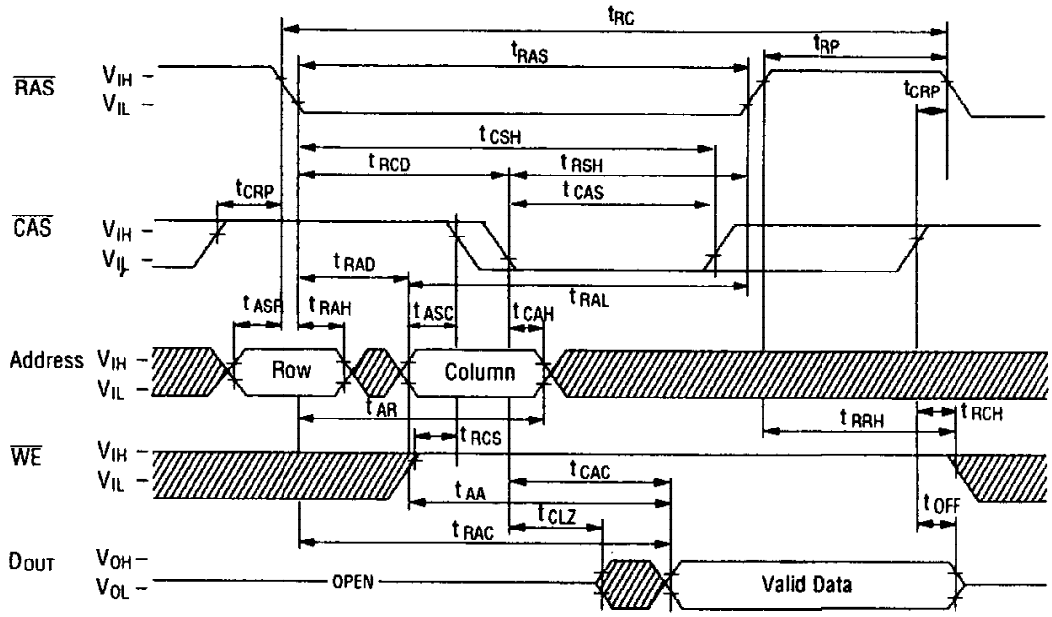


**Figure 3. Read Cycle**

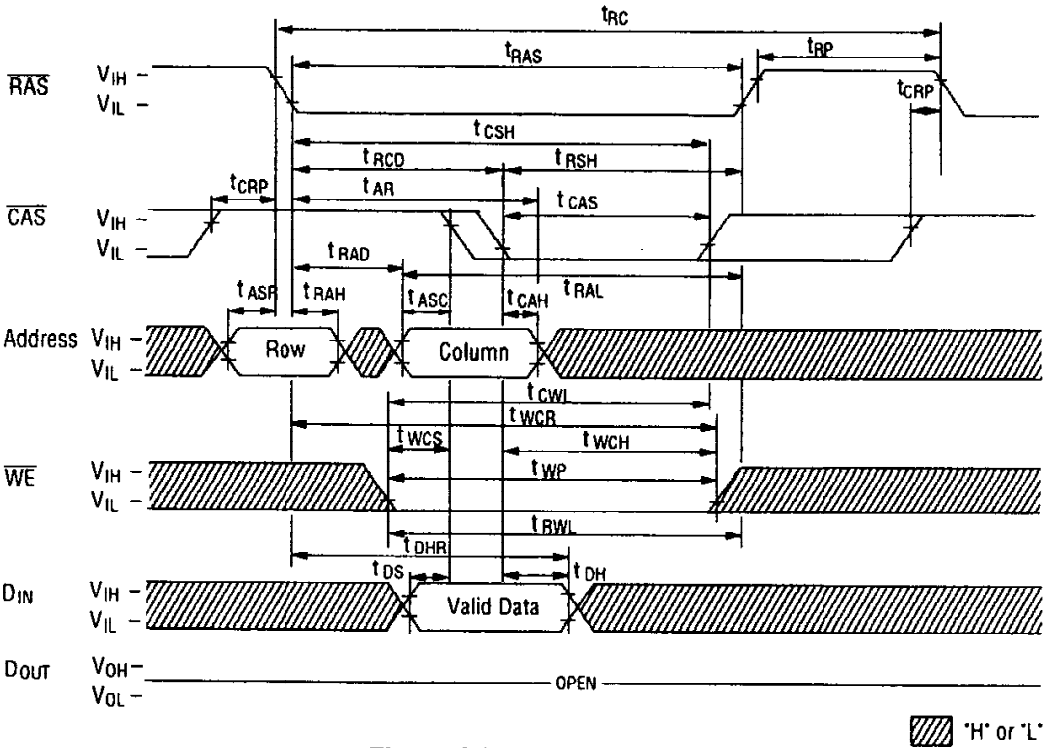


**Figure 4. Write Cycle (Early Write)**

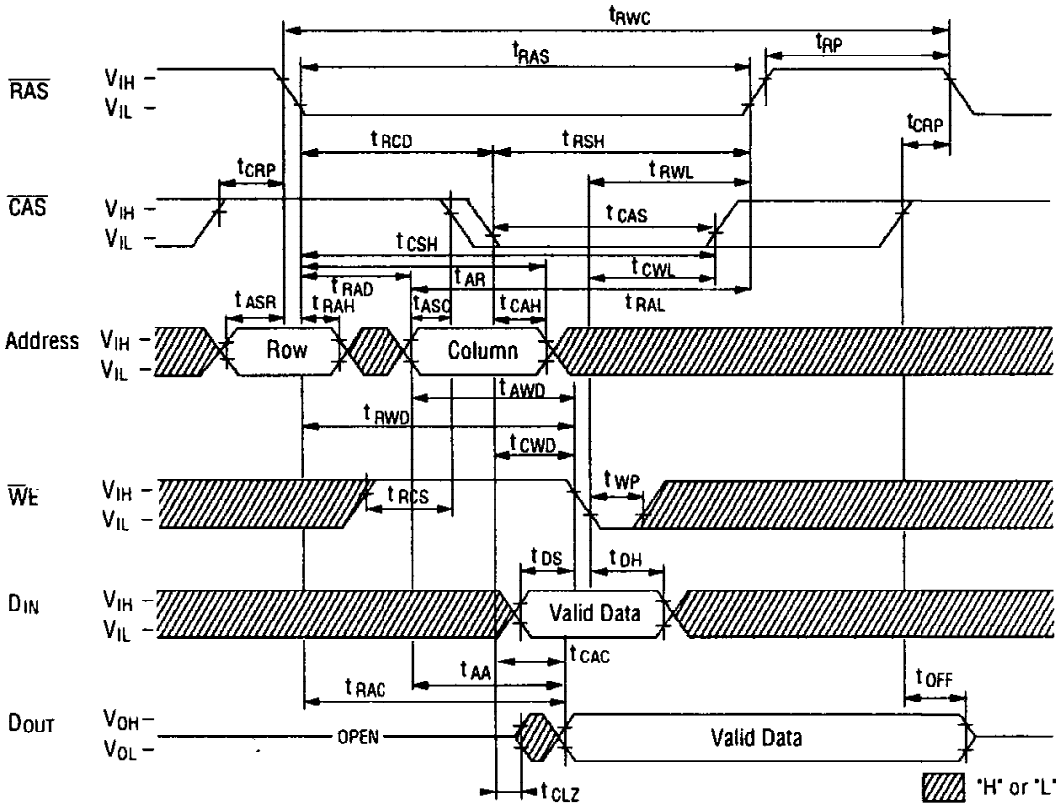


**Figure 5. Read/Write Cycle**

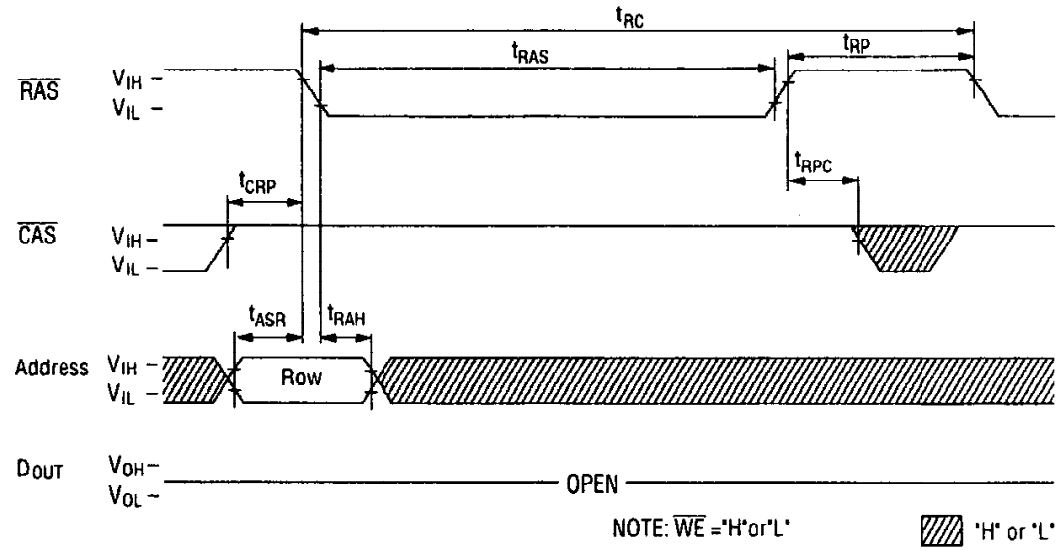


**Figure 6. RAS Only Refresh Cycle**

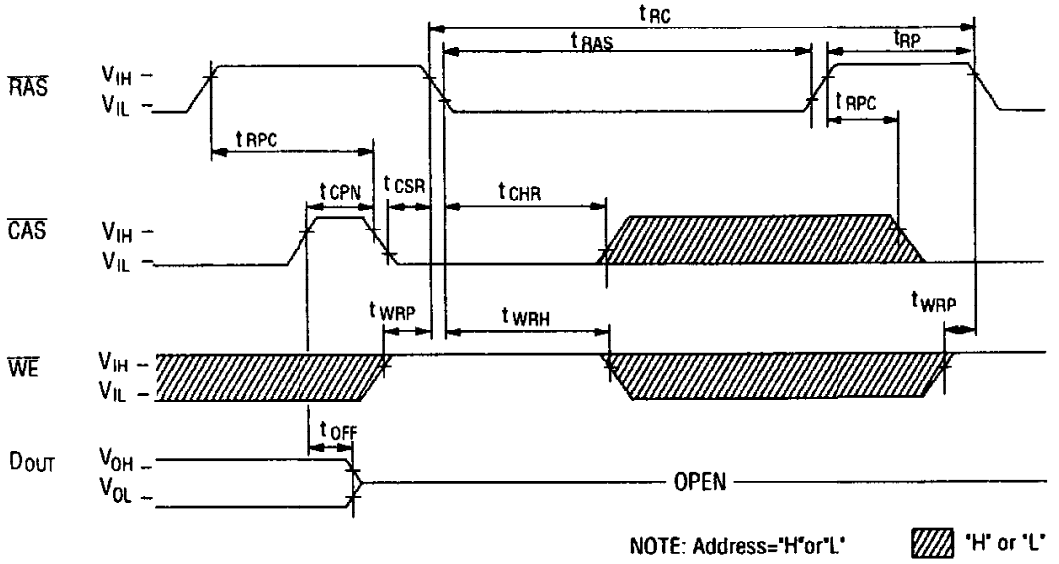


**Figure 7. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**

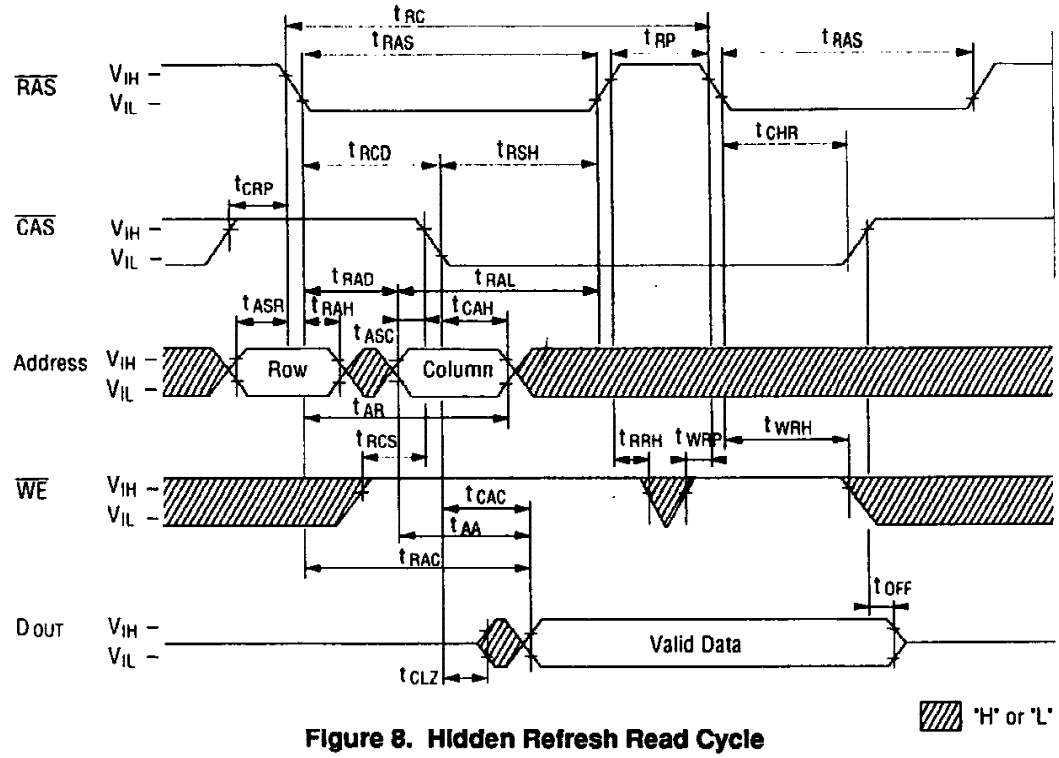


**Figure 8. Hidden Refresh Read Cycle**

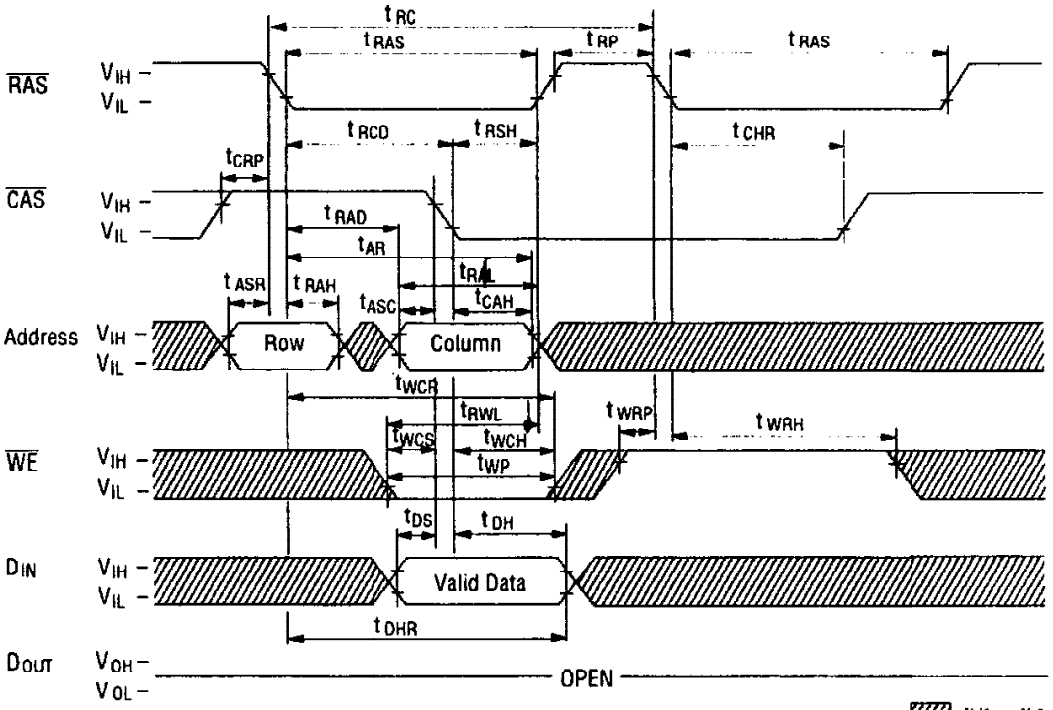


**Figure 9. Hidden Refresh Write Cycle**

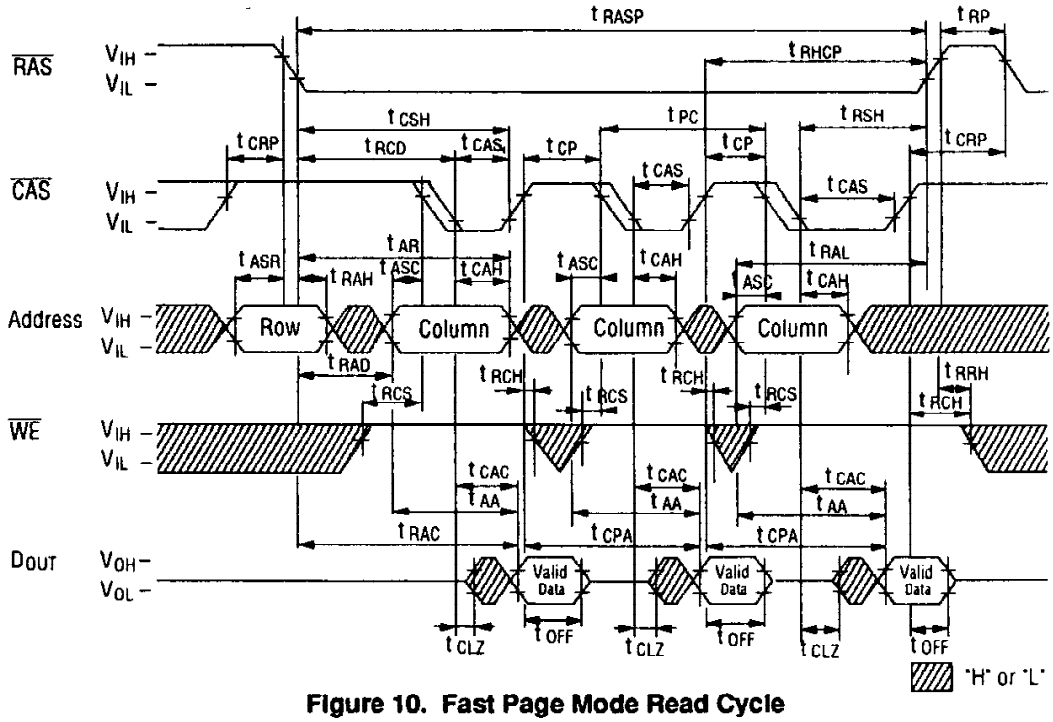


**Figure 10. Fast Page Mode Read Cycle**

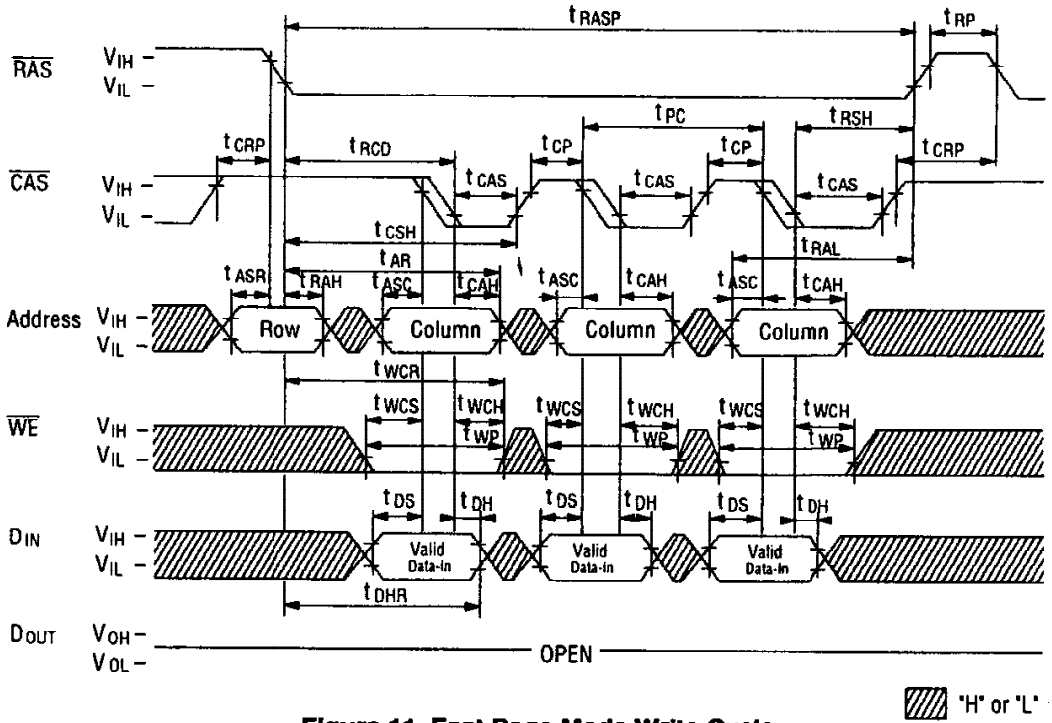


**Figure 11. Fast Page Mode Write Cycle**

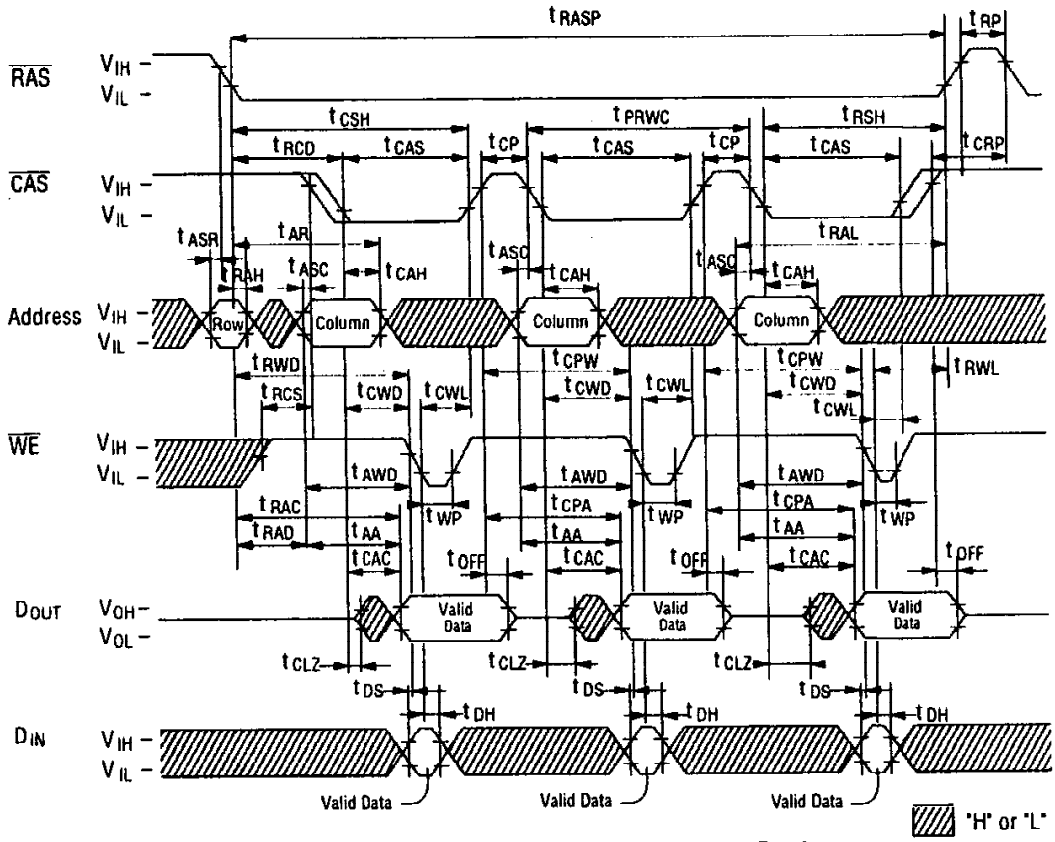


**Figure 12. Fast Page Mode Read/Write Cycle**

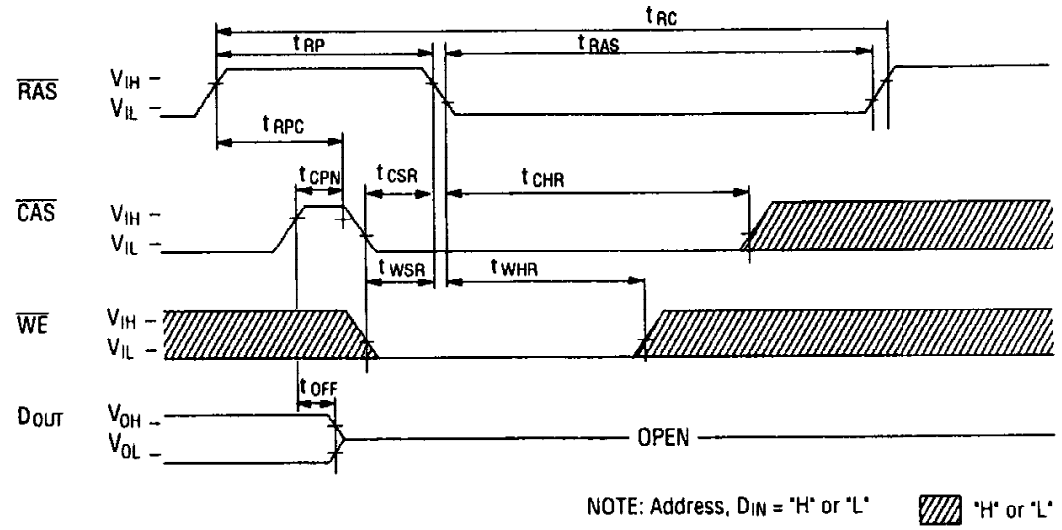


**Figure 13. Test Mode In Cycle**

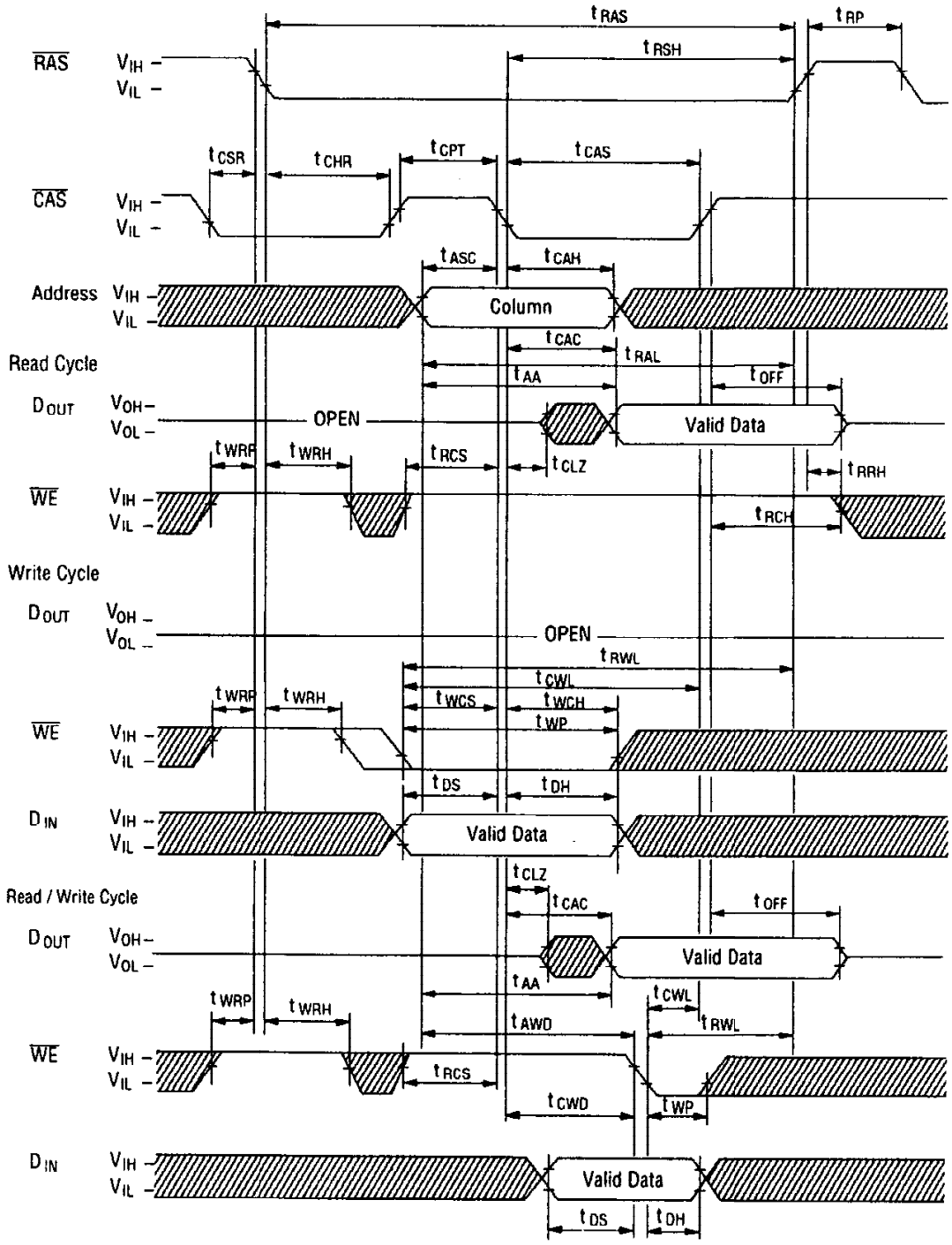


**Figure 14. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle**