OKI Semiconductor

This version: Jan. 1998
Previous version: Dec. 1996

MSM514252A

262,144-Word × 4-Bit Multiport DRAM

DESCRIPTION

The MSM514252A is an 1-Mbit CMOS multiport DRAM composed of a 262,144-word by 4-bit dynamic RAM, and a 512-word by 4-bit static serial access memory, SAM port. The RAM port and SAM port operate independently and asynchronously.
The MSM514252A supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

FEATURES

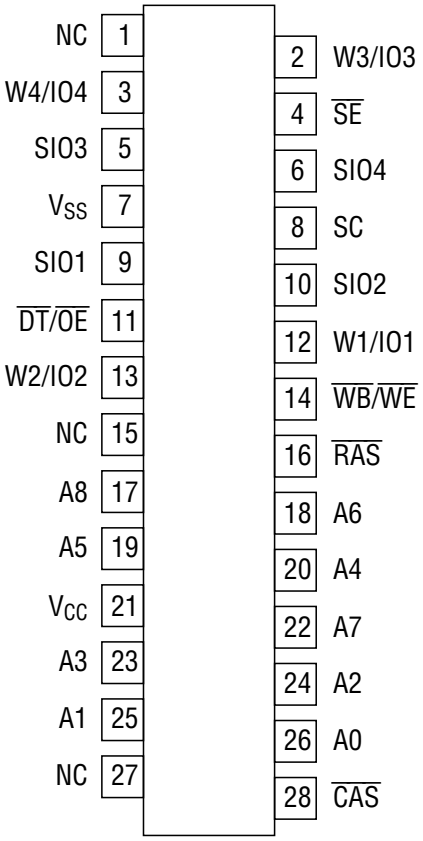
- Single power supply of 5 V ±10% with a built-in V_{BB} generator
- All inputs and outputs: TTL compatible
- Multiport organization
  RAM port: 256K word × 4 bits
  SAM port: 512 word × 4 bits
- RAM port
  Fast page mode, Read-modify-write
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
  $\overline{RAS}$ only refresh, Standard write-per-bit
- SAM port
  High speed serial
  Read/Write capability
  Fully static register
  512 tap location
- RAM-SAM bidirectional, Read/Write/Pseudo write, Real time read transfer
- Package options:

28-pin 400 mil plastic ZIP	(ZIP28-P-400-1.27)	(Product : MSM514252A-xxZS)
28-pin 400 mil plastic SOJ	(SOJ28-P-400-1.27)	(Product : MSM514252A-xxJS)
		xx indicates speed rank.

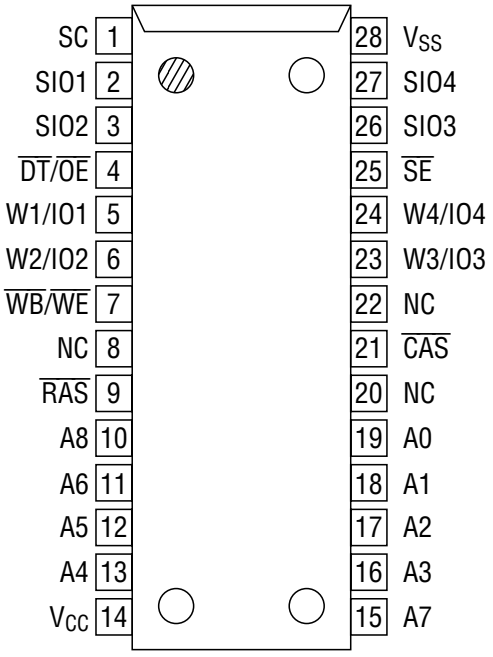
PRODUCT FAMILY

Family	Access Time		Cycle Time		Power Dissipation	
	RAM	SAM	RAM	SAM	Operating	Standby
MSM514252A-70	70 ns	25 ns	140 ns	30 ns	120 mA	8 mA
MSM514252A-80	80 ns	25 ns	150 ns	30 ns	110 mA	8 mA
MSM514252A-10	100 ns	25 ns	180 ns	30 ns	100 mA	8 mA

PIN CONFIGURATION (TOP VIEW)



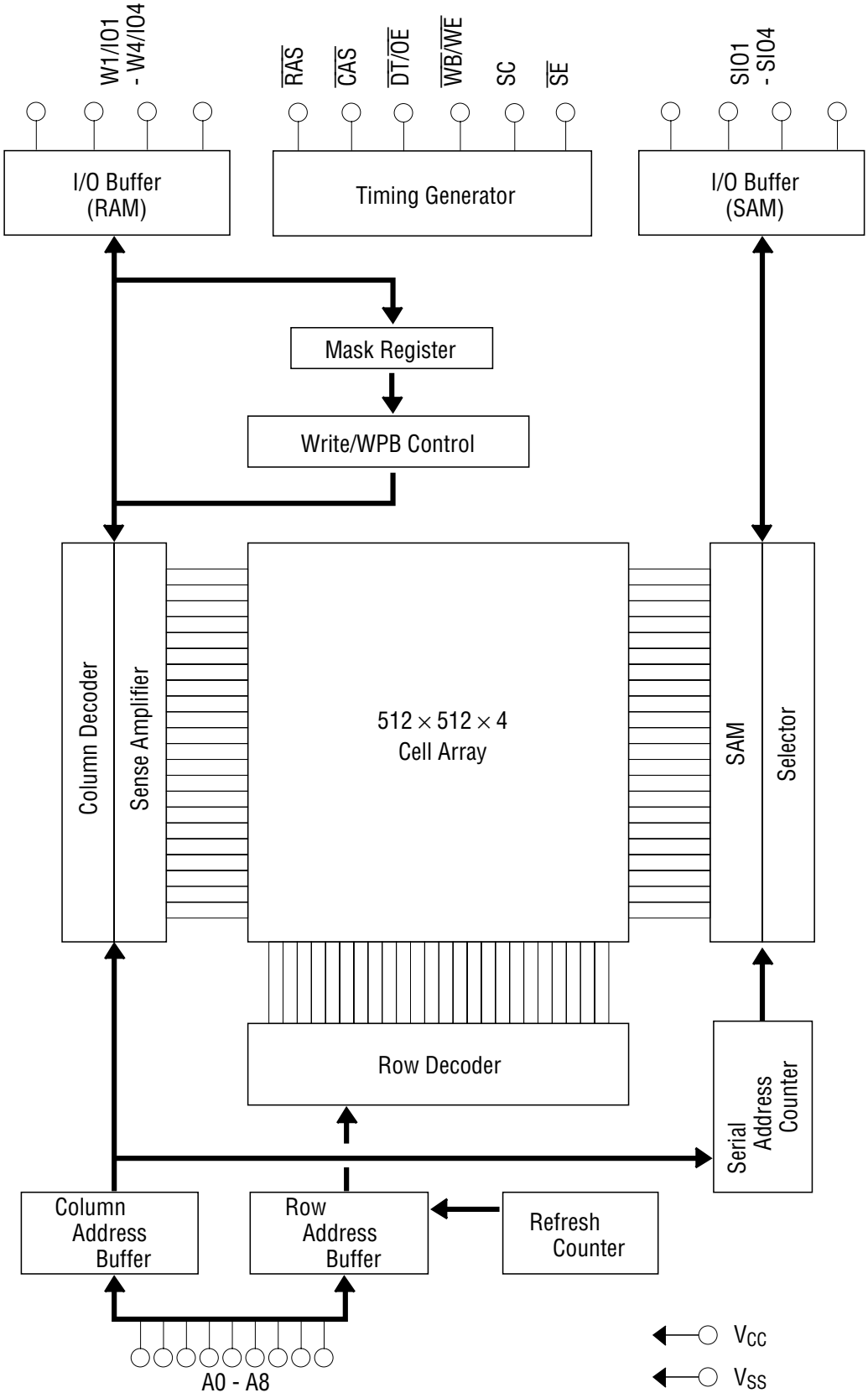
28-Pin Plastic ZIP



28-Pin Plastic SOJ

Pin Name	Function
A0 - A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
W1/IO1 - W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1 - SIO4	Serial Input/Output
V_{CC}/V_{SS}	Power Supply (5 V) /Ground (0 V)
NC	No Connection

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Note : 16)

Parameter	Symbol	Condition	Rating	Unit
Input Output Voltage	V_T	Ta = 25°C	–1.0 to 7.0	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 150	°C

Recommended Operating Conditions

(Ta = 0°C to 70°C) (Note : 17)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_I	—	7	pF
Input / Output Capacitance	$C_{I/O}$	—	9	pF

Note : This parameter is periodically sampled and is not 100% tested.

DC Characteristics 1

Parameter	Symbol	Condition	Min.	Max.	Unit
Output "H" Level Voltage	V_{OH}	I_{OH} = –2 mA	2.4	—	V
Output "L" Level Voltage	V_{OL}	I_{OL} = 2 mA	—	0.4	
Input Leakage Current	I_{LI}	$0 \le V_{IN} \le V_{CC}$ All other pins not under test = 0 V	–10	10	µA
Output Leakage Current	I_{LO}	$0 \le V_{OUT} \le 5.5$ V Output Disable	–10	10	

DC Characteristics 2

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Item (RAM)	SAM	Symbol	-70	-80	-10	Unit	Note
			Max.	Max.	Max.		
Operating Current	Standby	I_{CC1}	85	75	65	mA	1, 2
($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Active	I_{CC1A}	120	110	100		1, 2
Standby Current	Standby	I_{CC2}	8	8	8		3
($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Active	I_{CC2A}	50	45	40		1, 2
$\overline{RAS}$ Only Refresh Current	Standby	I_{CC3}	85	75	65		1, 2
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Active	I_{CC3A}	120	110	100		1, 2
Page Mode Current	Standby	I_{CC4}	70	65	60		1, 2
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Active	I_{CC4A}	120	110	100		1, 2
$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	Standby	I_{CC5}	85	75	65		1, 2
($\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Active	I_{CC5A}	120	110	100		1, 2
Data Transfer Current	Standby	I_{CC6}	85	75	65		1, 2
($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Active	I_{CC6A}	120	110	100		1, 2

AC Characteristics (1/3)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 4, 5, 6

Parameter	Symbol	-70		-80		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	140	—	150	—	180	—	ns	
Read Modify Write Cycle Time	t_{RWC}	195	—	195	—	235	—	ns	
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	90	—	90	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	7, 13
Access Time from Column Address	t_{AA}	—	35	—	40	—	50	ns	7, 13
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	—	25	ns	7, 14
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	40	—	45	—	50	ns	7, 14
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	20	0	20	ns	9
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	35	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10k	80	10k	100	10k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	t_{RASP}	70	100k	80	100k	100	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10k	25	10k	25	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	55	20	75	ns	13
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	50	ns	13
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	55	—	55	—	70	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	55	—	55	—	70	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	

AC Characteristics (2/3)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 4, 5, 6

Parameter	Symbol	-70		-80		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data Hold Time	t_{DH}	15	—	15	—	15	—	ns	11
Data Hold Time referenced to $\overline{RAS}$	t_{DHR}	55	—	55	—	70	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	100	—	100	—	130	—	ns	12
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	65	—	65	—	80	—	ns	12
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	ns	12
Data to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
Access Time from $\overline{OE}$	t_{OEA}	—	20	—	20	—	25	ns	7
Output Buffer Turn-off Delay from $\overline{OE}$	t_{OEZ}	0	10	0	10	0	20	ns	9
$\overline{OE}$ to Data Delay Time	t_{OED}	10	—	10	—	20	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	10	—	10	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	15	—	15	—	15	—	ns	
$\overline{CAS}$ Set-up Time for $\overline{CAS}$ before $\overline{RAS}$ Cycle	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Cycle	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{RPC}	0	—	0	—	0	—	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{WB}$ Set-up Time	t_{WSR}	0	—	0	—	0	—	ns	
$\overline{WB}$ Hold Time	t_{RWH}	15	—	15	—	15	—	ns	
Write Per Bit Mask Data Set-up Time	t_{MS}	0	—	0	—	0	—	ns	
Write Per Bit Mask Data Hold Time	t_{MH}	15	—	15	—	15	—	ns	
$\overline{DT}$ High Set-up Time	t_{THS}	0	—	0	—	0	—	ns	
$\overline{DT}$ High Hold Time	t_{THH}	15	—	15	—	15	—	ns	
$\overline{DT}$ Low Set-up Time	t_{TLS}	0	—	0	—	0	—	ns	
$\overline{DT}$ Low Hold Time	t_{TLH}	15	10k	15	10k	15	10k	ns	
$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	t_{RTH}	60	10k	65	10k	80	10k	ns	
$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	t_{ATH}	25	—	30	—	30	—	ns	
$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	t_{CTH}	20	—	25	—	25	—	ns	
$\overline{SE}$ Set-up Time referenced to $\overline{RAS}$	t_{ESR}	0	—	0	—	0	—	ns	
$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	t_{REH}	15	—	15	—	15	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Precharge Time	t_{TRP}	60	—	60	—	70	—	ns	
$\overline{DT}$ Precharge Time	t_{TP}	20	—	20	—	30	—	ns	
$\overline{RAS}$ to First SC Delay Time (Read Transfer)	t_{RSD}	70	—	80	—	100	—	ns	
Column Address to First SC Delay Time (Read Transfer)	t_{ASD}	45	—	45	—	50	—	ns	
$\overline{CAS}$ to First SC Delay Time (Read Transfer)	t_{CSD}	20	—	25	—	25	—	ns	
Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	t_{TSL}	5	—	5	—	5	—	ns	

AC Characteristics (3/3)

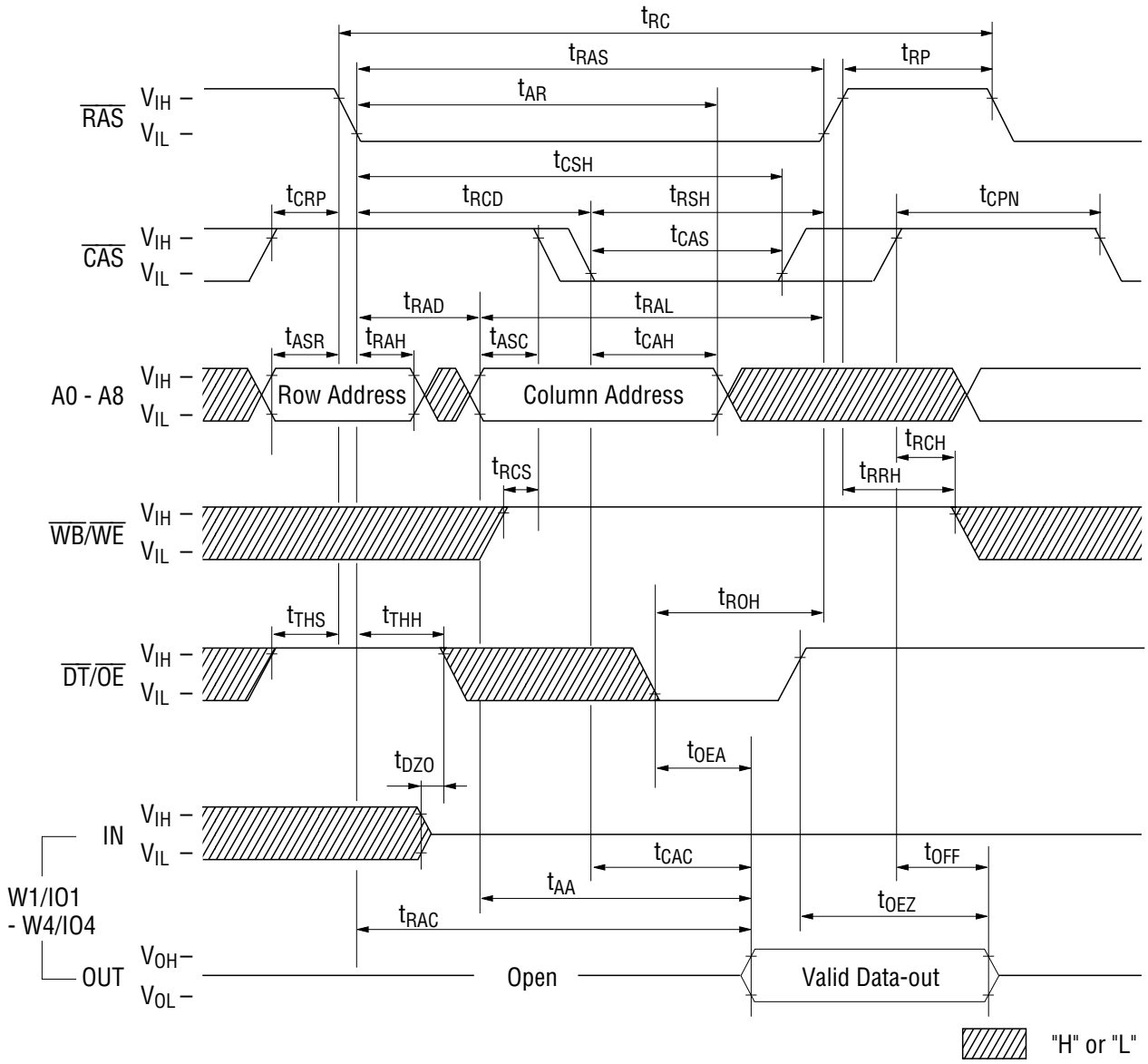
(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 4, 5, 6

Parameter	Symbol	-70		-80		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{DT}$ to First SC Delay Time (Read Transfer)	t_{TSD}	15	—	15	—	15	—	ns	
Last SC to $\overline{RAS}$ Set-up Time (Serial Input)	t_{SRS}	25	—	25	—	30	—	ns	
$\overline{RAS}$ to First SC Delay Time (Serial Input)	t_{SRD}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to Serial Input Delay Time	t_{SDD}	40	—	40	—	50	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	t_{SDZ}	10	40	10	40	10	50	ns	9
SC Cycle Time	t_{SCC}	30	—	30	—	30	—	ns	
SC Pulse Width (SC High Time)	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Time (SC Low Time)	t_{SCP}	10	—	10	—	10	—	ns	
Access Time from SC	t_{SCA}	—	25	—	25	—	25	ns	8
Serial Output Hold Time from SC	t_{SOH}	5	—	5	—	5	—	ns	
Serial Input Set-up Time	t_{SDS}	0	—	0	—	0	—	ns	
Serial Input Hold Time	t_{SDH}	15	—	15	—	15	—	ns	
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	25	—	25	ns	8
$\overline{SE}$ Pulse Width	t_{SE}	25	—	25	—	25	—	ns	
$\overline{SE}$ Precharge Time	t_{SEP}	25	—	25	—	25	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	0	20	0	20	0	20	ns	9
Serial Input to $\overline{SE}$ Delay Time	t_{SZE}	0	—	0	—	0	—	ns	
Serial Input to First SC Delay Time	t_{SZS}	0	—	0	—	0	—	ns	
Serial Write Enable Set-up Time	t_{SWS}	5	—	5	—	5	—	ns	
Serial Write Enable Hold Time	t_{SWH}	15	—	15	—	15	—	ns	
Serial Write Disable Set-up Time	t_{SWIS}	5	—	5	—	5	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	15	—	15	—	15	—	ns	

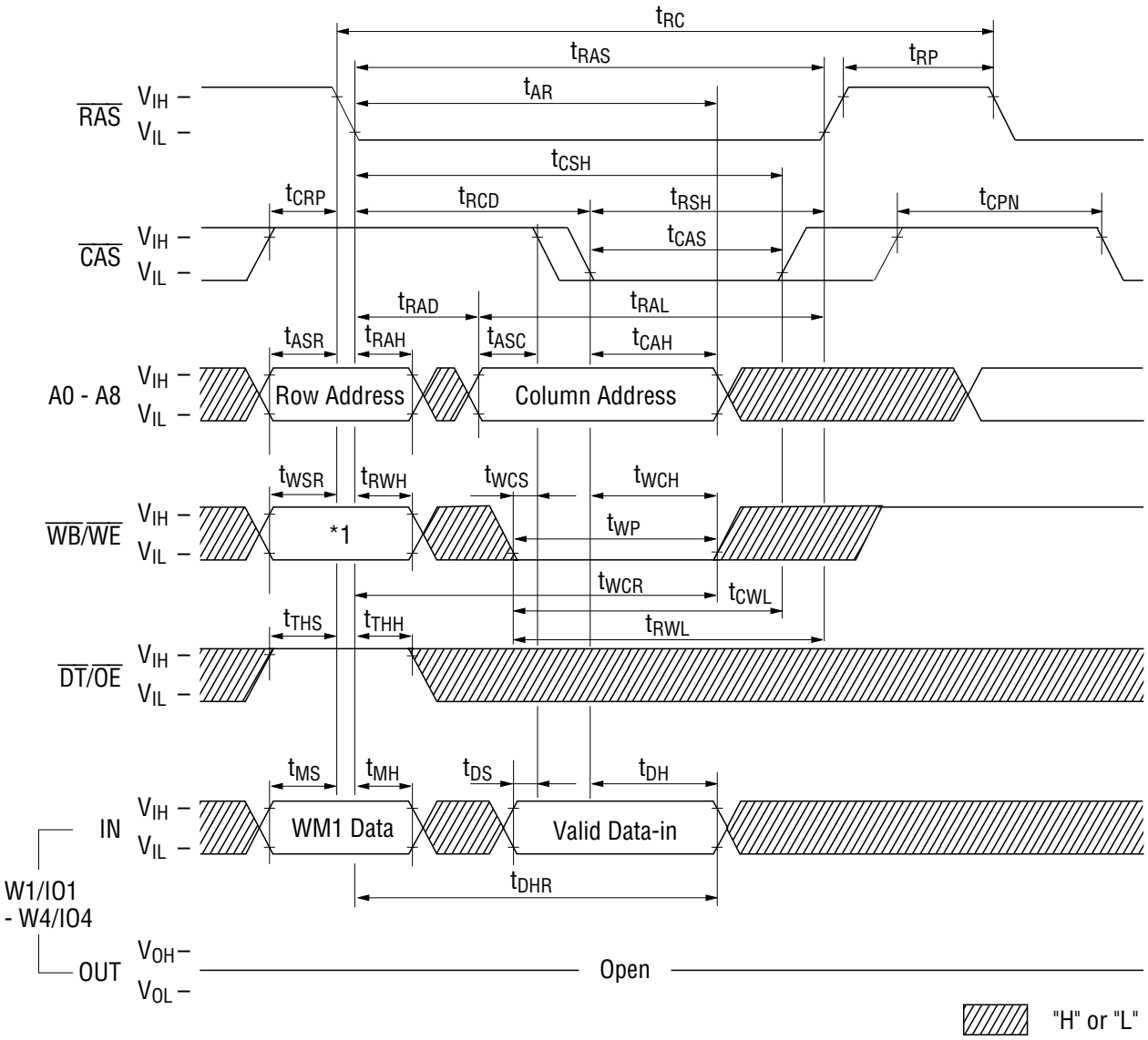
Notes:
1. These parameters depend on output loading. Specified values are obtained with the output open.
2. These parameters are masured at minimum cycle test.
3. I_{CC2} (Max.) are mesured under the condition of TTL input level.
4. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
5. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper divice operation is achieved. In the case of using an internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles in stead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. RAM port outputs are mesured with a load equivalent to 1 TTL load and 100 pF. Output reference levels are V_{OH}/V_{OL} = 2.4 V/0.8 V.
8. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. Output reference levels are V_{OH}/V_{OL} = 2.0 V/0.8 V.
9. t_{OFF} (Max.), t_{OEZ} (Max.), t_{SDZ} (Max.) and t_{SEZ} (Max.) difine the time at which the outputs achieve the open circuit condition and are not reference to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$ controlled write cycles and read modify write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.
    If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout the entire cycle : If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.) the cycle is a read-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indterminate.
13. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
15. Input levels at the AC parameter measurement are 3.0 V/0 V.
16. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permenent damege to the device.
17. All voltages are referenced to V_{SS}.

TIMING WAVEFORM

Read Cycle



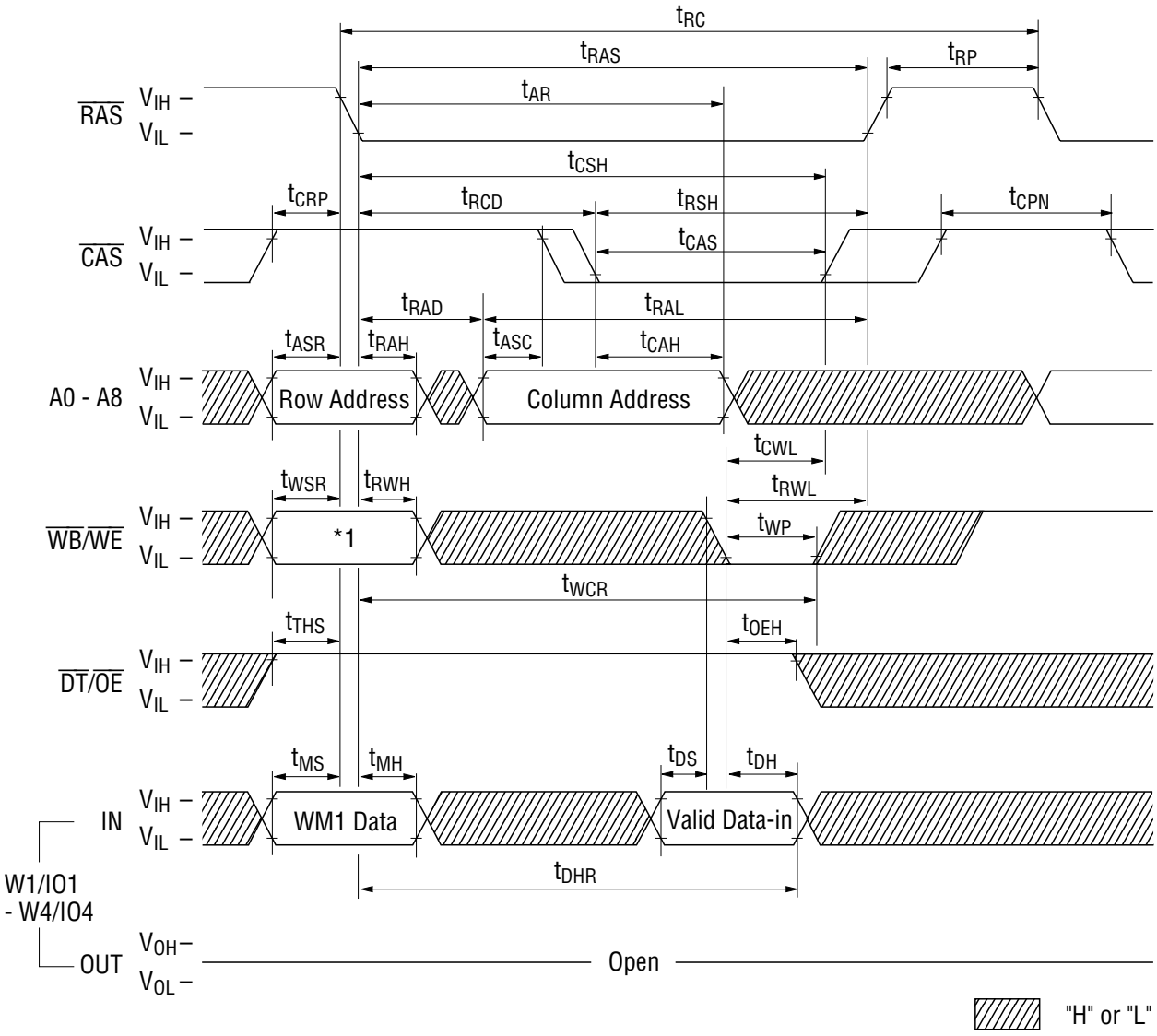
Write Cycle (Early Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1 - W4/IO4	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

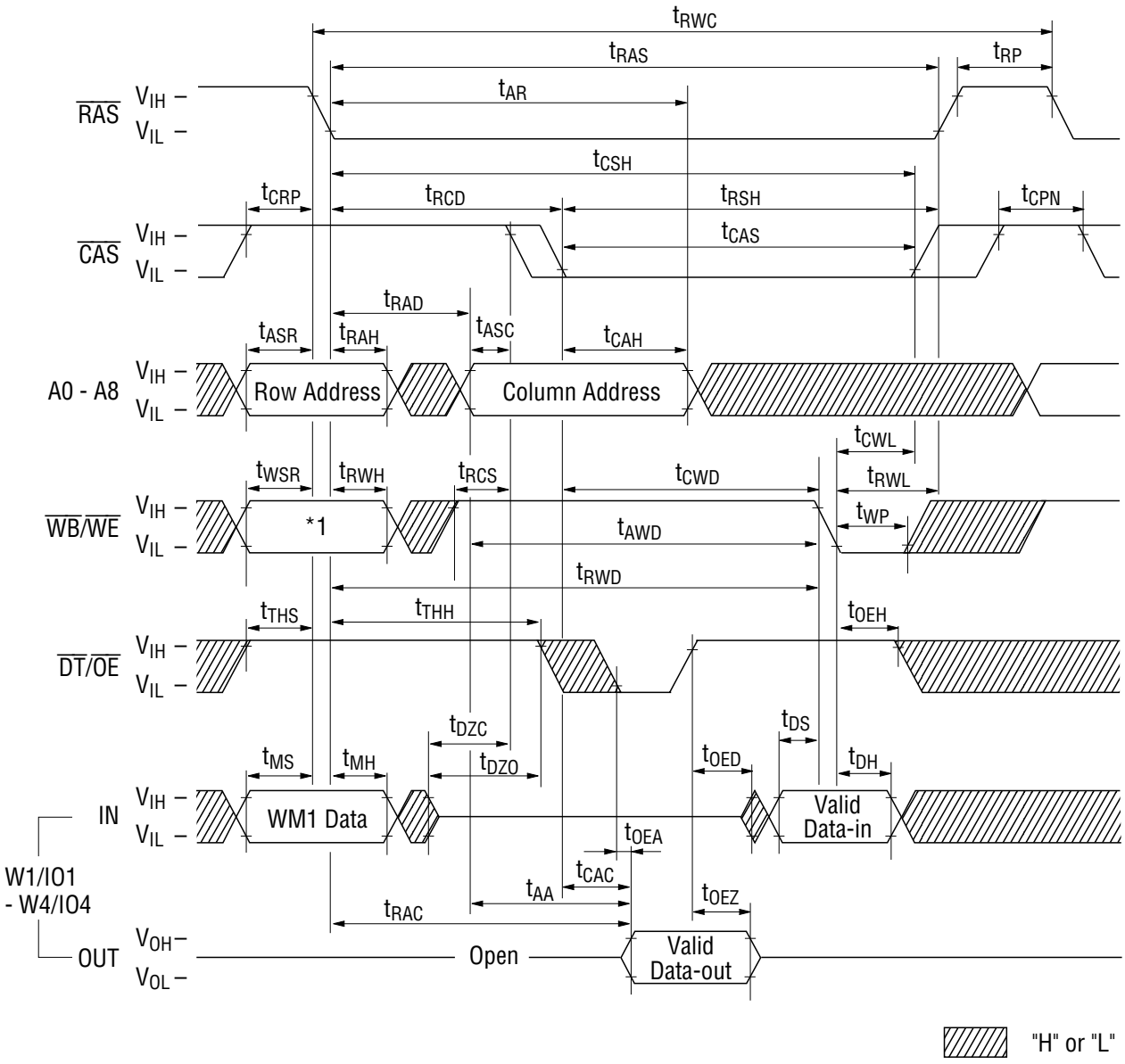
Write Cycle ($\overline{OE}$ Controlled Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1 - W4/IO4	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

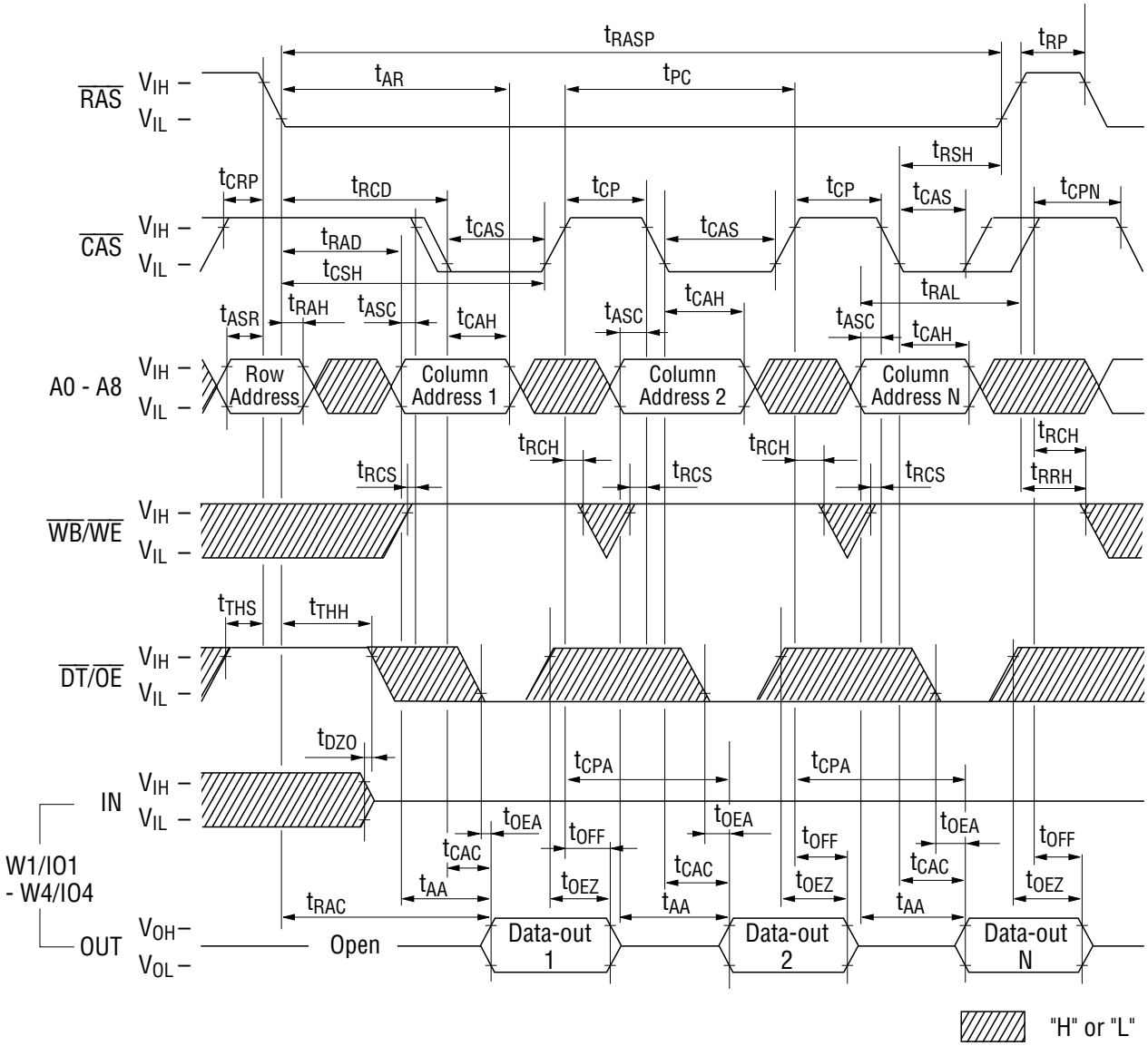
Read Modify Write Cycle



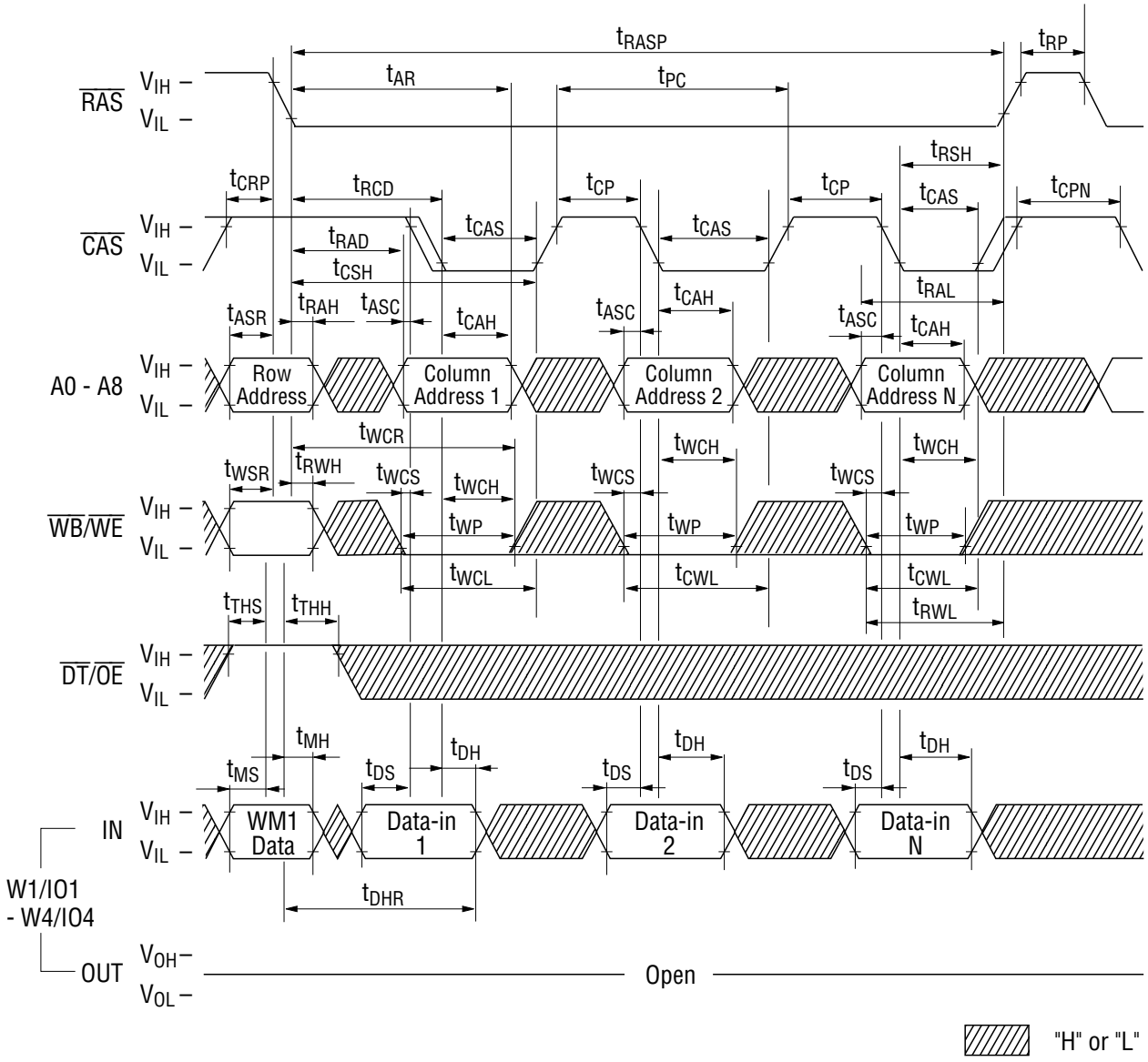
*1 $\overline{WB}/\overline{WE}$	W1/IO1 - W4/IO4	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

Fast Page Mode Read Cycle



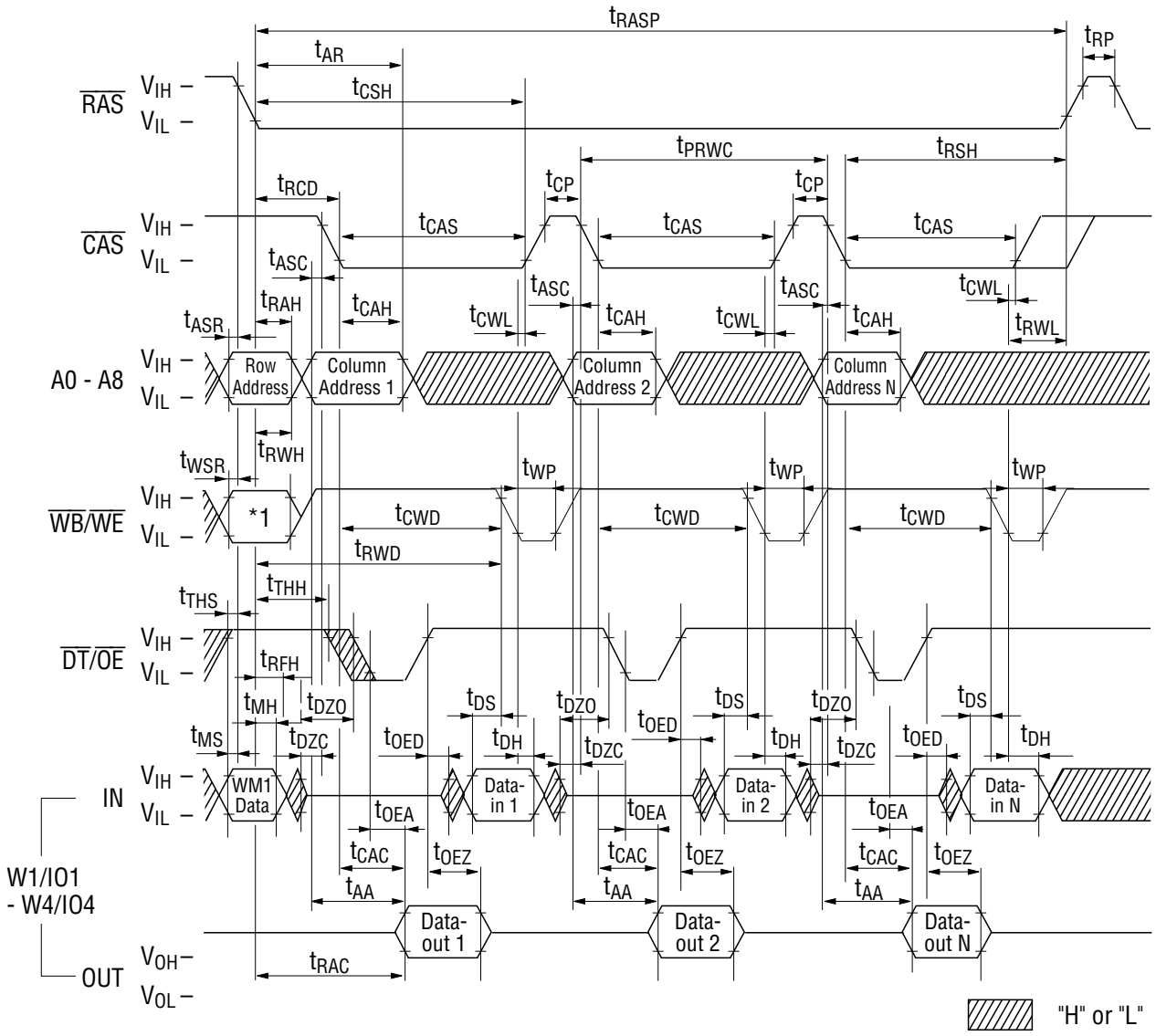
Fast Page Mode Write Cycle (Early Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1 - W4/IO4	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

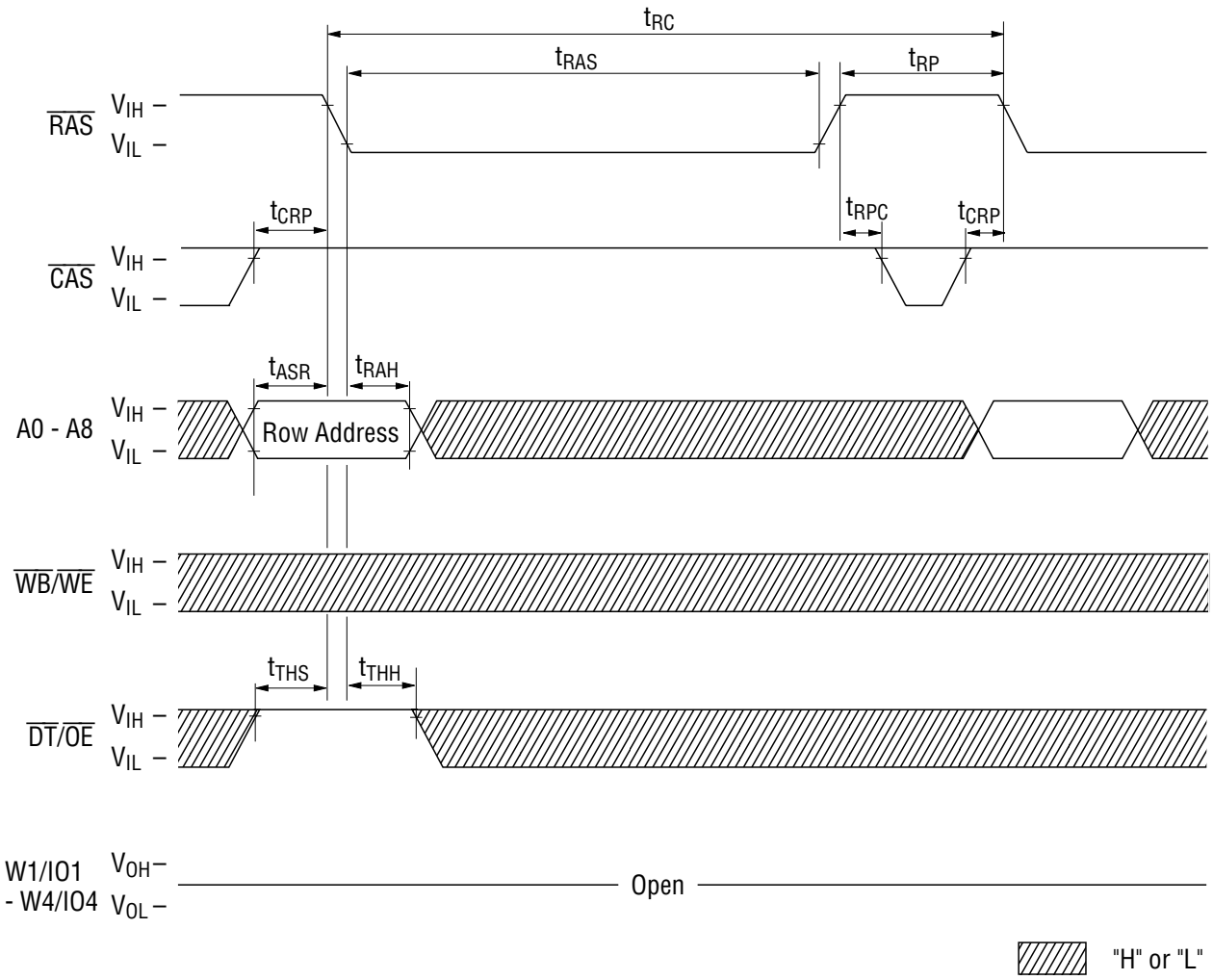
Fast Page Mode Read Modify Write Cycle



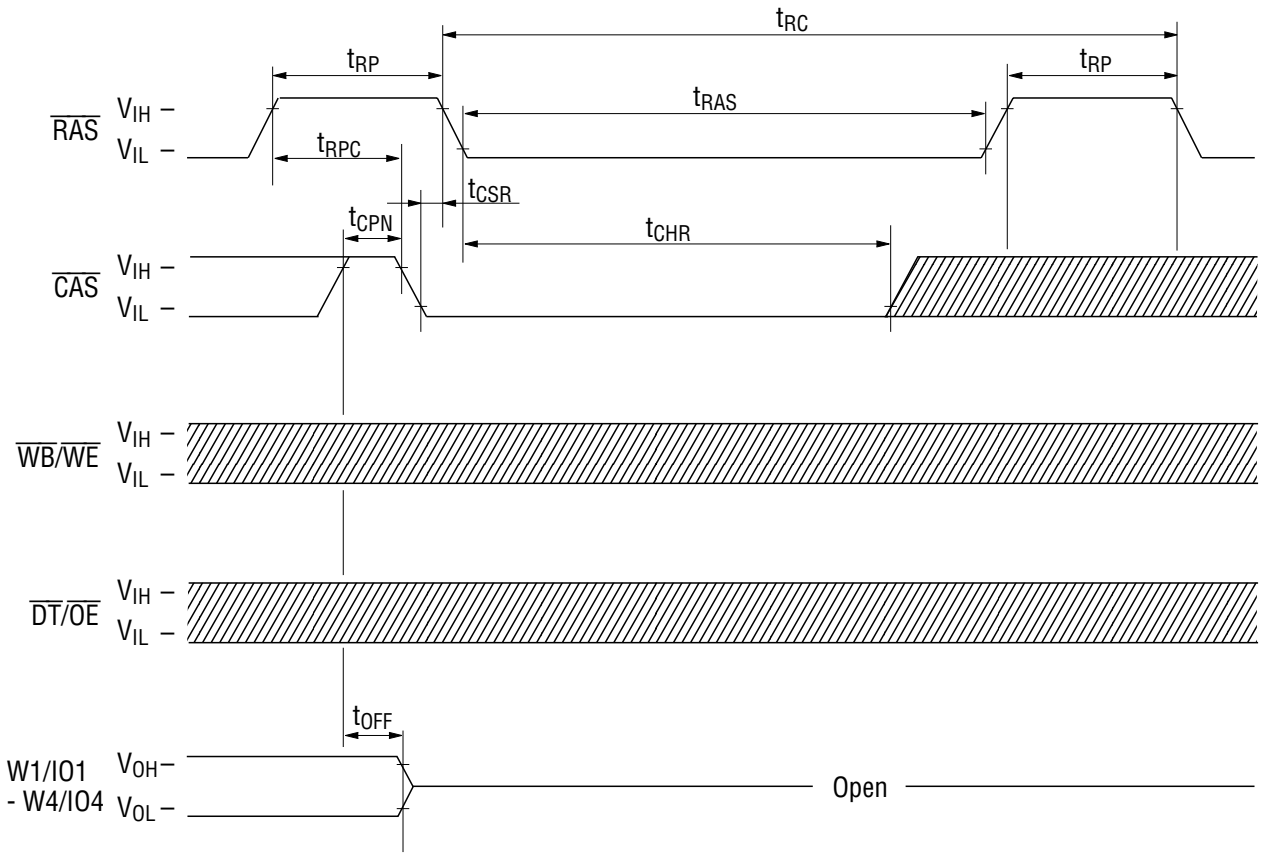
*1 $\overline{WB}/\overline{WE}$	W1/IO1 - W4/IO4	Cycle
0	WM1 data	Write per Bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

$\overline{RAS}$-Only Refresh Cycle

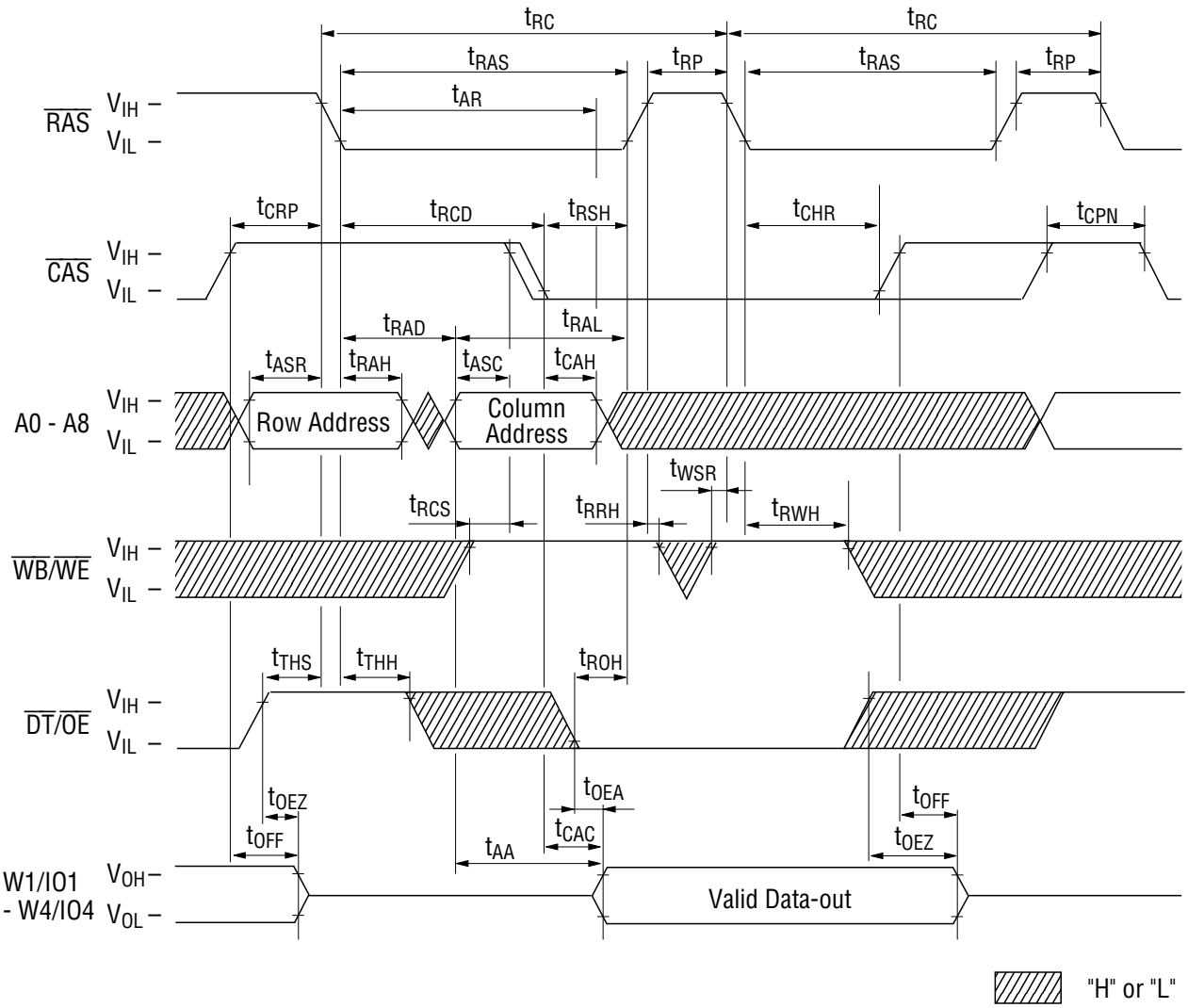


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

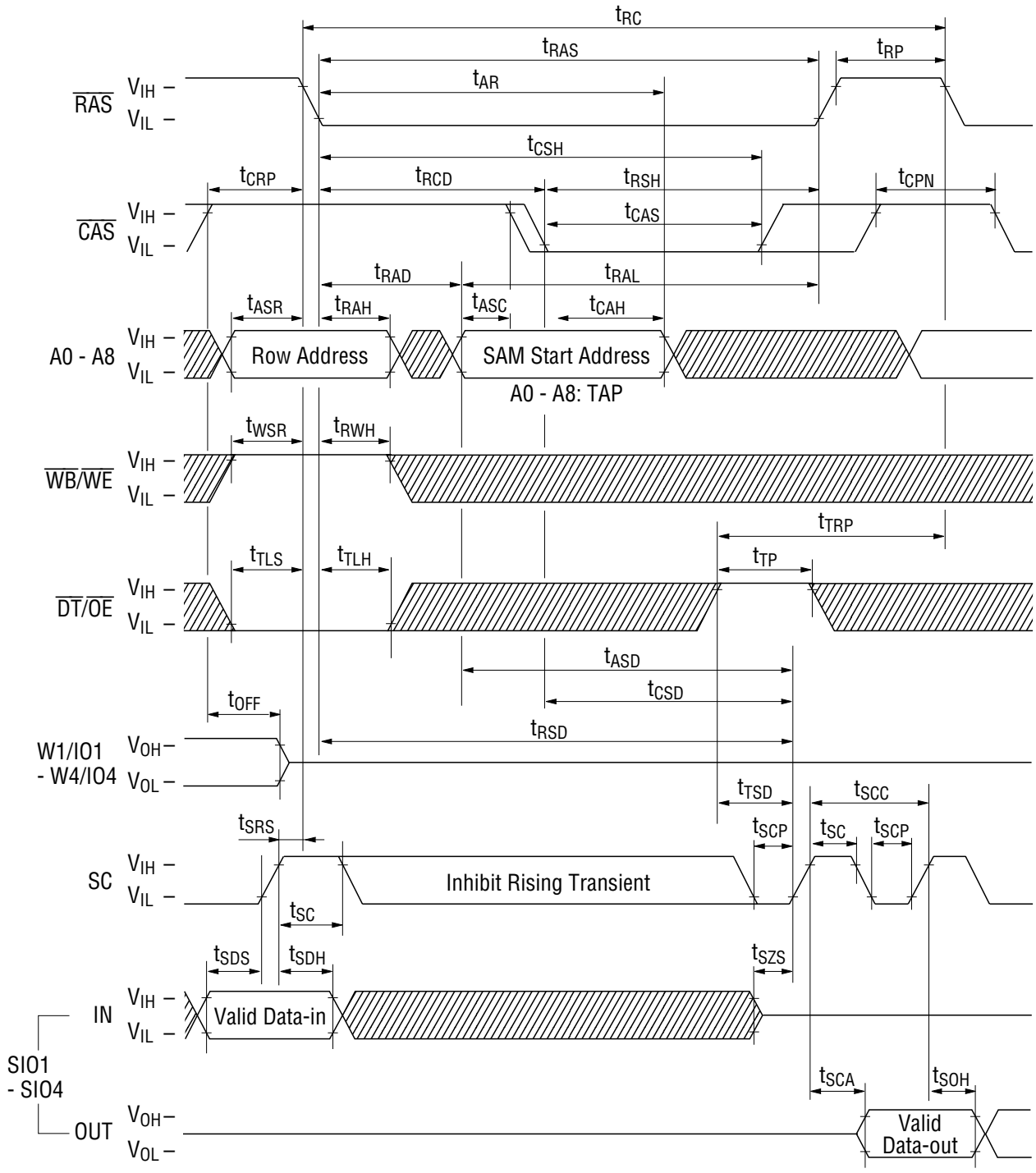


Note: A0 - A8 = Don't Care ("H" or "L") "H" or "L"

Hidden Refresh Cycle

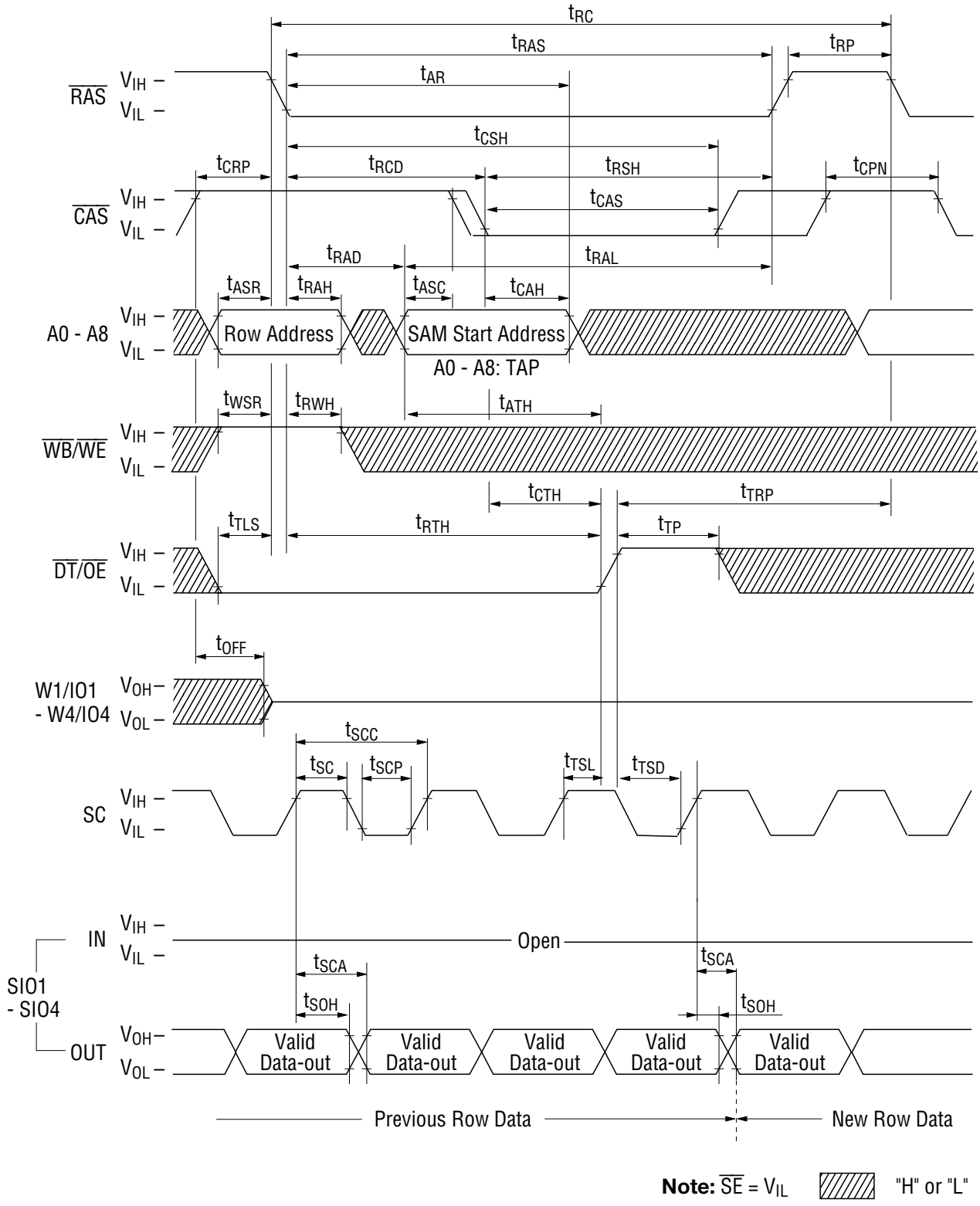


Read Transfer Cycle (Previous Transfer is Write Transfer Cycle)



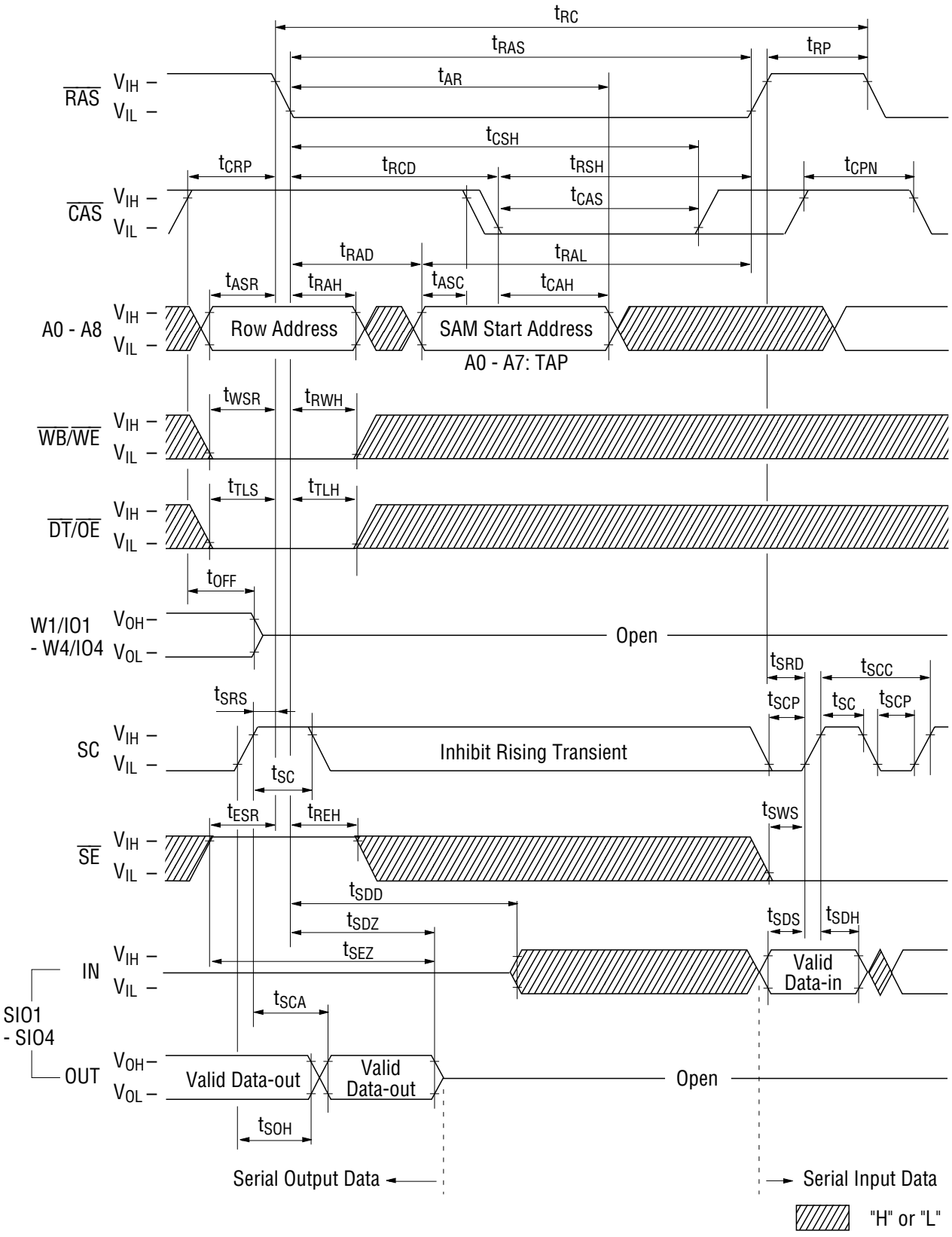
Note: $\overline{SE}$ = V_{IL} "H" or "L"

Real Time Read Transfer Cycle

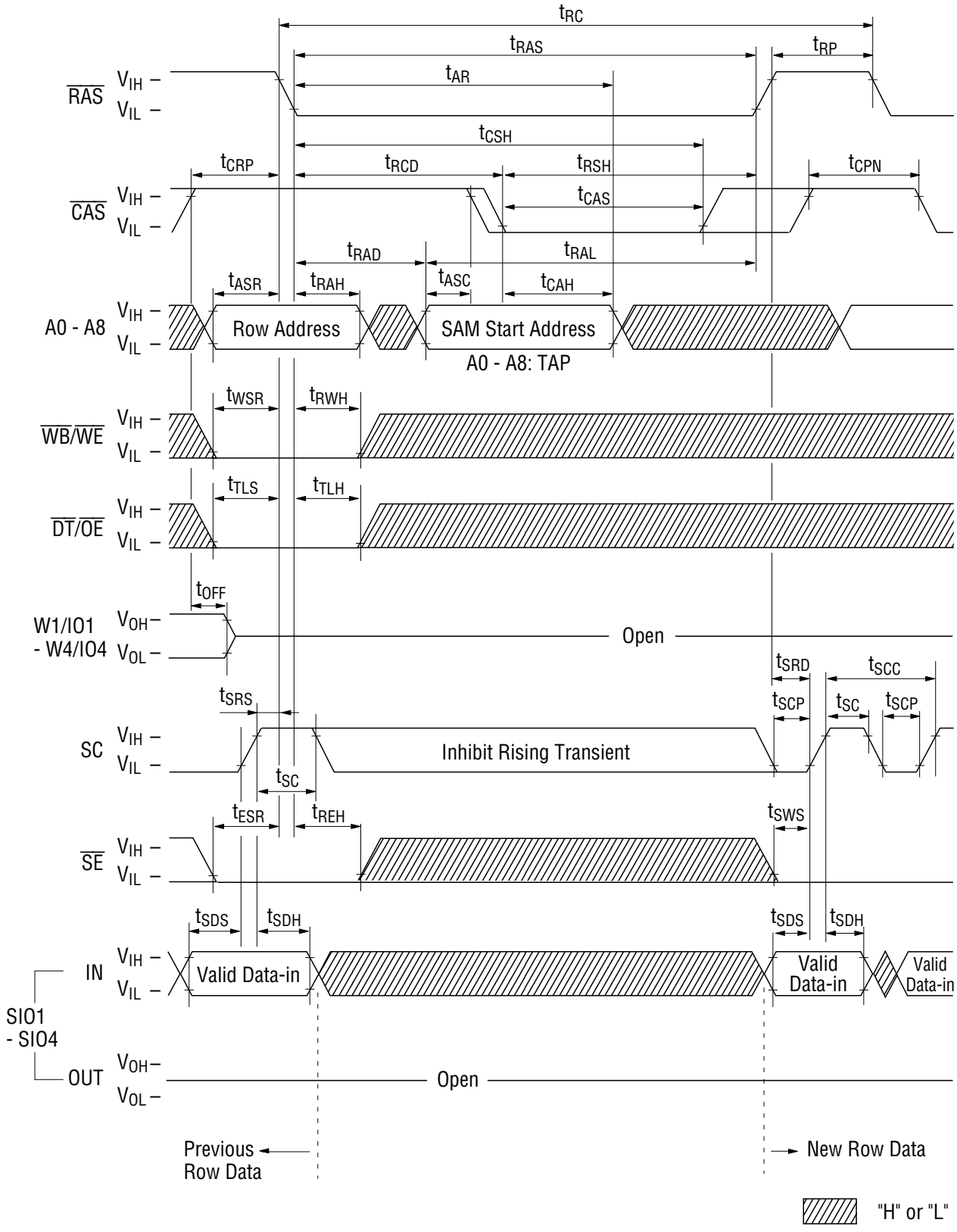


Note: $\overline{SE}$ = V_{IL} "H" or "L"

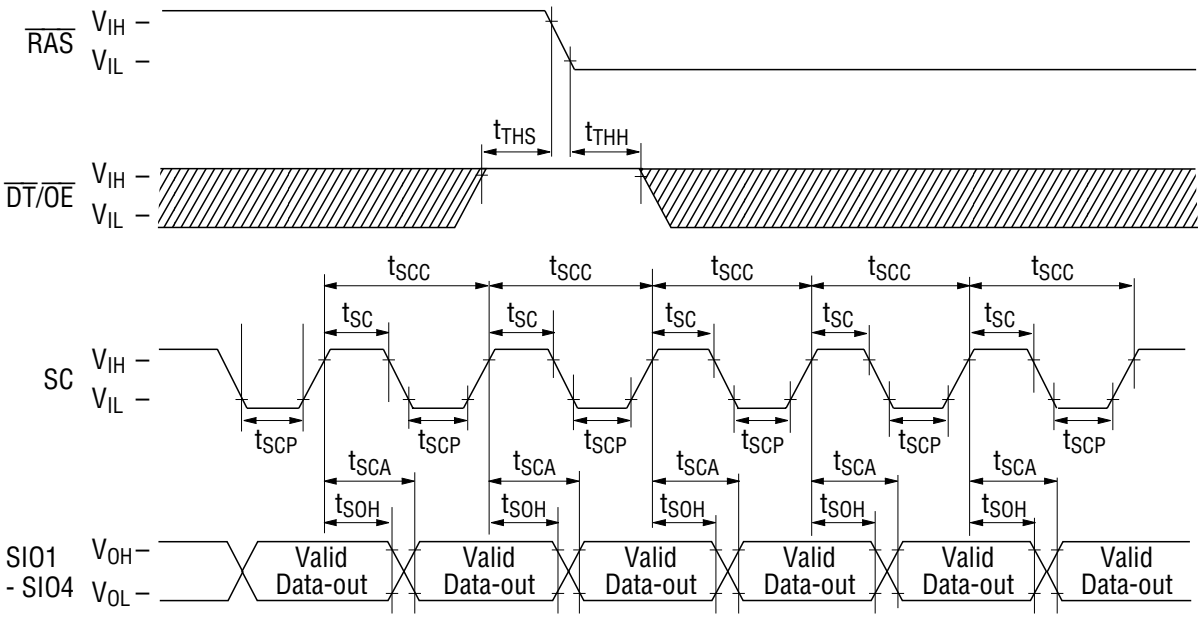
Pseudo Write Transfer Cycle



Write Transfer Cycle

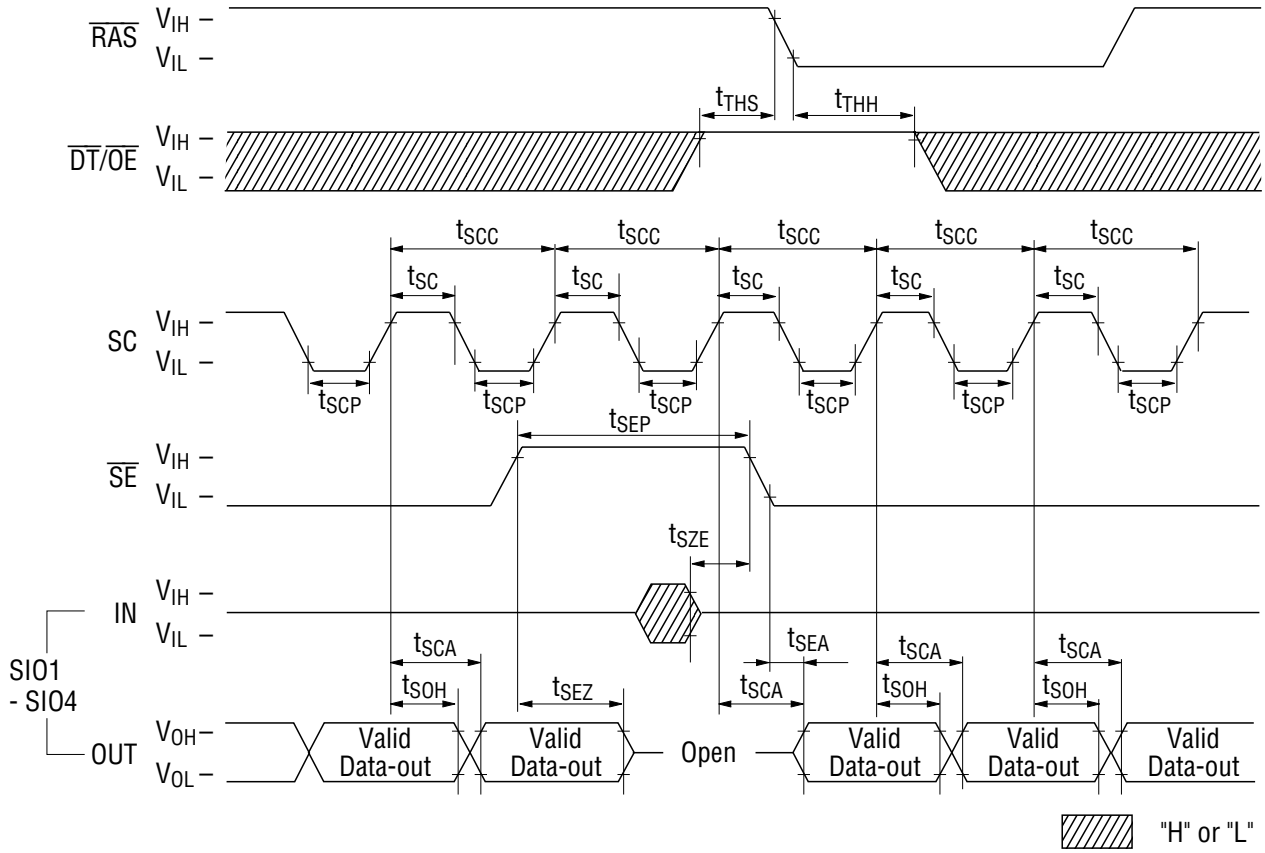


Serial Read Cycle ($\overline{SE}$ = V_{IL})

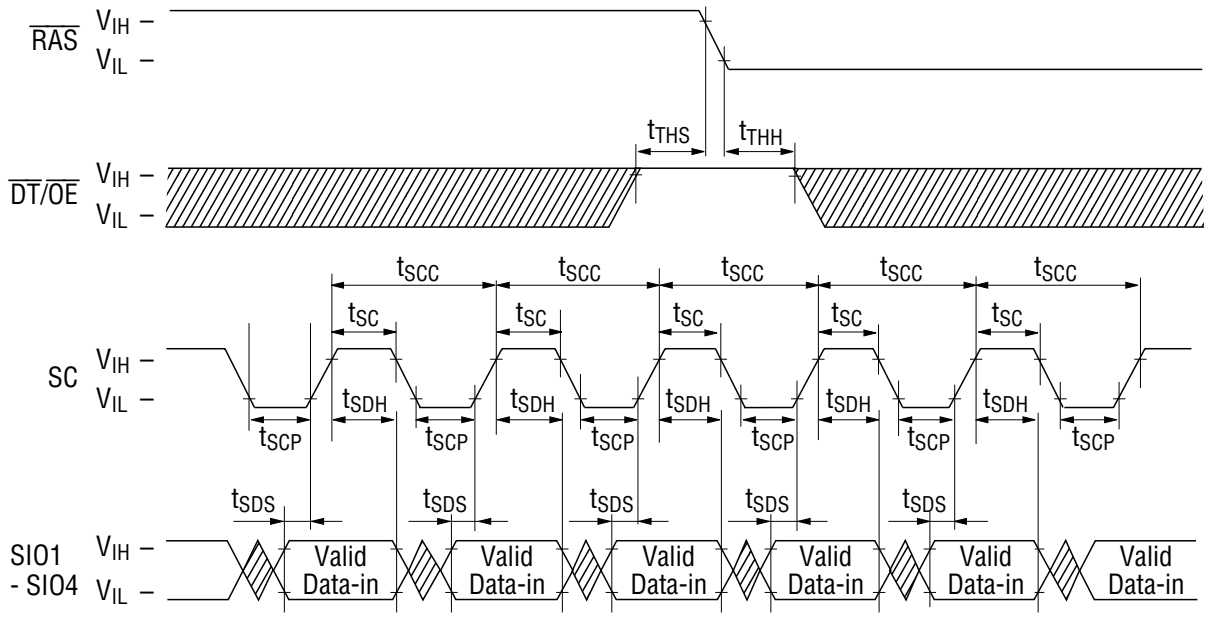


Note: $\overline{SE}$ = V_{IL} "H" or "L"

Serial Read Cycle ($\overline{SE}$ Controlled Outputs)

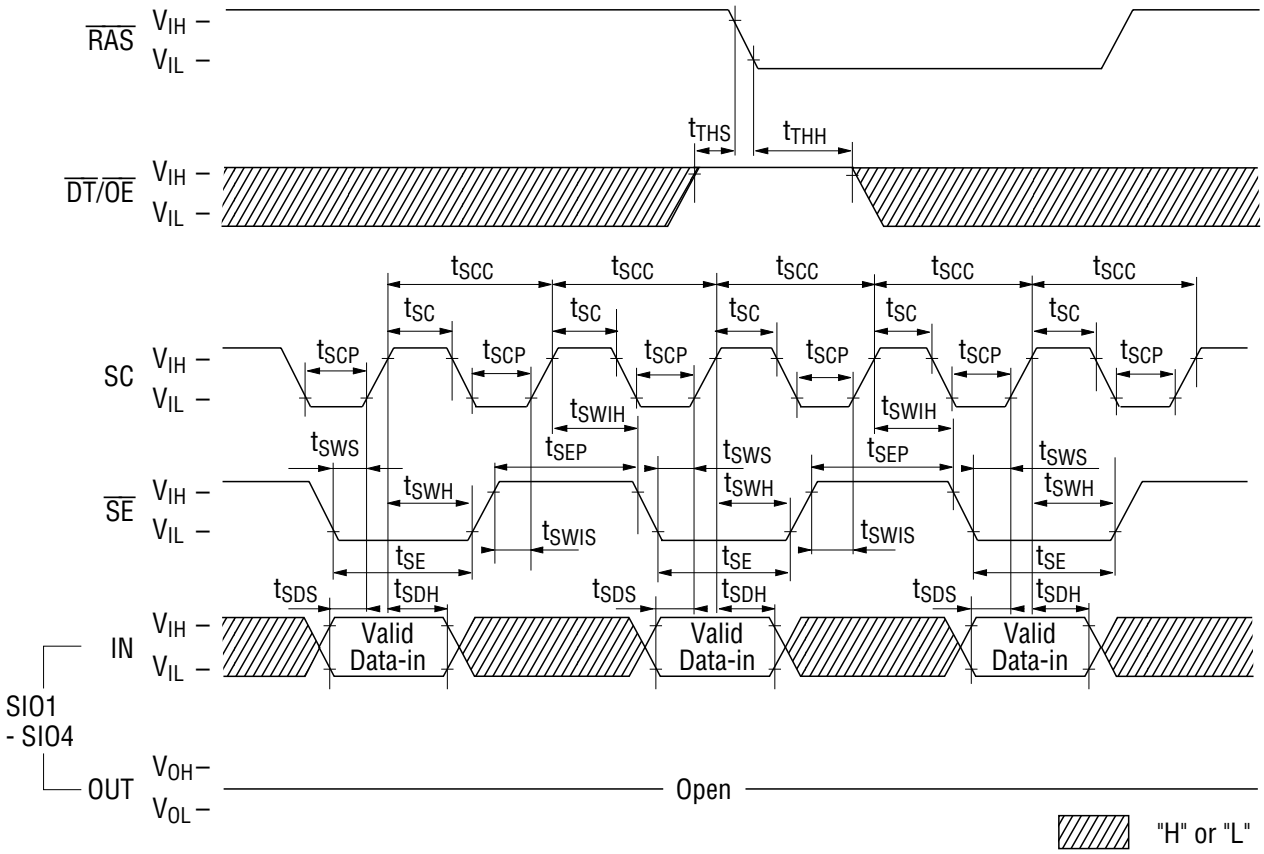


Serial Write Cycle ($\overline{SE}$ = V_{IL})



Note: $\overline{SE}$ = V_{IL} "H" or "L"

Serial Write Cycle ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

Address Input: A0 - A8

The 18 address bits decode an 8-bit location out of the 262,144 locations in the MSM514252A memory array. The address bits are multiplexed to 9 address input pins (A0 - A8) as standard DRAM. Nine row address bits are latched at the falling edge of $\overline{RAS}$. The following nine column address bits are latched at the falling edge of $\overline{CAS}$.

Row Addres Strobe: $\overline{RAS}$

$\overline{RAS}$ is a basic RAM control input signal. The RAM port is in standby mode when the $\overline{RAS}$ level is "high". As the standard DRAM's $\overline{RAS}$ signal function, $\overline{RAS}$ is the control input that latches the row address bits and a random access cycle begins at the falling edge of $\overline{RAS}$.
In addition to the conventional RAM signal functions, the level of the input signals, $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$, and $\overline{SE}$, at the falling edge of $\overline{RAS}$, determines the MSM514252A operation modes.

Column Address Strobe: $\overline{CAS}$

As the standard DRAM's $\overline{CAS}$ signal function, $\overline{CAS}$ is the control input signal that latches the column address input and acts as an RAM port output enable signal.

Data Transfer/Output Enable: $\overline{DT}/\overline{OE}$

$\overline{DT}/\overline{OE}$ is also a control input signal having multiple functions. As the standard DRAM's $\overline{OE}$ signal function, $\overline{DT}/\overline{OE}$ is used as an output enable control when $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$.
In addition to the conventional $\overline{OE}$ signal function, a data transfer operation is started between the RAM port and the SAM port when the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$.

Write per Bit/Write Enable: $\overline{WB}/\overline{WE}$

$\overline{WB}/\overline{WE}$ is a control input signal having multiple functions. As the standard DRAM's $\overline{WE}$ signal function, it is used to write data into the memory array on the RAM port when $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$.
In addition to the conventional $\overline{WE}$ signal function, the $\overline{WB}/\overline{WE}$ determines the write-per-bit function when $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations. The $\overline{WB}/\overline{WE}$ also determines the direction of data transfer between the RAM and SAM. When $\overline{WB}$/$\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

Write Mask Data/Data Input and Output: W1/IO1 - W4/IO4

W1/IO1 - W4/IO4 have the functions of both Input/Output and a control input signal. As the standard DRAM's I/O pins, input data on the W1/IO1 - W4/IO4 are written into the RAM port during the write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs later. The RAM data out buffers, which will output read data from the W1/IO1-W4/IO4 pins, become low impedance state after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and the output data will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs earlier.
In addition to the conventional I/O functions, the W1/IO1 - W4/IO4 have the function to set the mask data, which select mask input pins out of four inputs pins, W1/IO1 - W4/IO4, at the falling edge of $\overline{RAS}$. Data is written in to the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle.

Serial Clock: SC

SC is a main serial cycle control input signal. All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC.
The serial clock SC also increments the 9 bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the setting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held data constant V_{IH} or V_{IL} level during read/pseudo write/write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ is a serial access enable control and serial read/write control input signal. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disable, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Serial Input/Output: SIO1 - SIO4

Serial input/output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode.

RAM PORT OPERATION

Fast Page Mode Cycle

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle.
During a fast page cycle, the $\overline{RAS}$ signal may be maintained activity for a period up to 100μ seconds.
For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$.
For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or Read-Modify-Write cycle.

$\overline{RAS}$-Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8 ms refresh period.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$ before $\overline{RAS}$ Refresh

The MSM514252A also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place.
When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

Hidden Refresh

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the out put data from the previous memory cycle to remain valid while performing a refresh.
The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period.

Write-per-Bit Function

The Write-Per-Bit selectively controls the internal write-enable circuits of the RAM port. Write-Per-Bit is enabled when $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$ in a random write operation. Also, at the falling edge of $\overline{RAS}$, the mask data on the Wi/IOi pins are latched into a write mask register. The write mask data must be presented at the Wi/IOi pins at every falling edge of $\overline{RAS}$. A "0" on any of the Wi/IOi pins will disable the corresponding write circuits and new data will not be written into the RAM. A "1" on any of the Wi/IOi pins will enable the corresponding write circuits and new data will be written into the RAM.

DATA TRANSFER OPERATION

The MSM514252A features an internal data transfer capability between RAM and the SAM. During a transfer cycle, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer).
The MSM514252A supports three types of transfer operations: Read transfer, Write Transfer and pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$, the type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ latched at the falling edge of $\overline{RAS}$.
During data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer/pseudo write transfer).
During a data transfer cycle, the row A0-A8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A0-A8 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle.

Read Transfer Cycle

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" and $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row tho by transferred into the SAM.
The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode.
In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.
In a read transfer cycle preceded by a write transfer cycle, the SC clock must be held at a constant VIL or VIH, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$.
In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied.
This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible , the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied). The timing restriction t_{TSL}/t_{TSD} are 5 ns min./10 ns min..

Write Transfer Cycle

A write transfer cycle transfers the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles.
However, if the SAM data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer cycle.
A write transfer is invoked by holding $\overline{CAS}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "low" at the falling edge of $\overline{RAS}$.
The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM.
After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.
When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed.
Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

Pseudo Write Transfer Cycle

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur).
After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high" $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "high" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Transfer Operation Without $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column addresses are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed.

Normal Read Transfer Cycle After Normal Read Transfer Cycle

Another read transfer may be performed following the read transfer provided that a minimum delay of 30 ns from the rising edge of the first clock SC is satisfied.

POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200µ seconds (minimum) is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high".
After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

Initial State After Power-up

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high" the internal state of the MSM514252A is automatically set as follows.

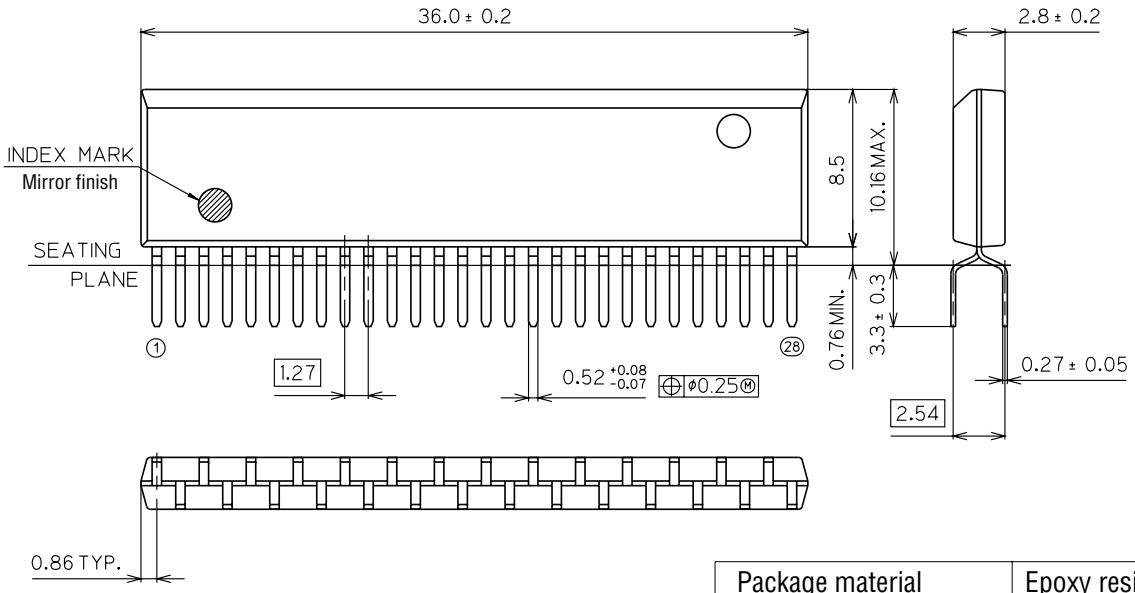
SAM port ---------- → Input mode
Write mask register ------ → Write mode
TAP pointer ---------- → Invalid

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200µ seconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

PACKAGE DIMENSIONS

(Unit : mm)

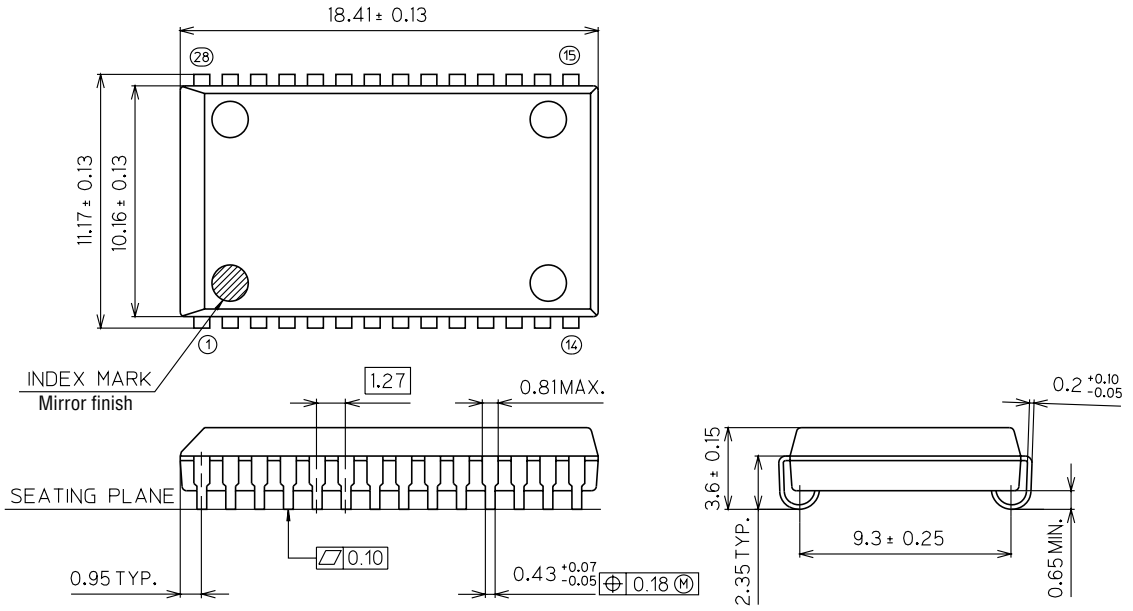
ZIP28-P-400-1.27



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.85 TYP.

(Unit : mm)

SOJ28-P-400-1.27



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.30 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).