Preliminary

# OKI Semiconductor

# MSM51V4400/L/SL

**1,048,576-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE**

## DESCRIPTION

The MSM51V4400/L/SL is a 1,048,576-word×4-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM51V4400/L/SL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon single metal CMOS. The MSM51V4400/L/SL is available in a 26/20-pin plastic SOJ or 26/20-pin plastic TSOP. The MSM51V4400L (the low-power version) and the MSM51V4400SL (the self-refresh version) are specially designed for lower-power applications.

## FEATURES

- 1,048,576-word × 4-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTL compatible, low input capacitance
- Output : LVTTL compatible, 3-state
- Refresh : 1024 cycles/16 ms, 1024 cycles/128 ms (L/SL version)
- Fast page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- $\overline{CAS}$ before $\overline{RAS}$ self-refresh capability (SL version)
- Package options:

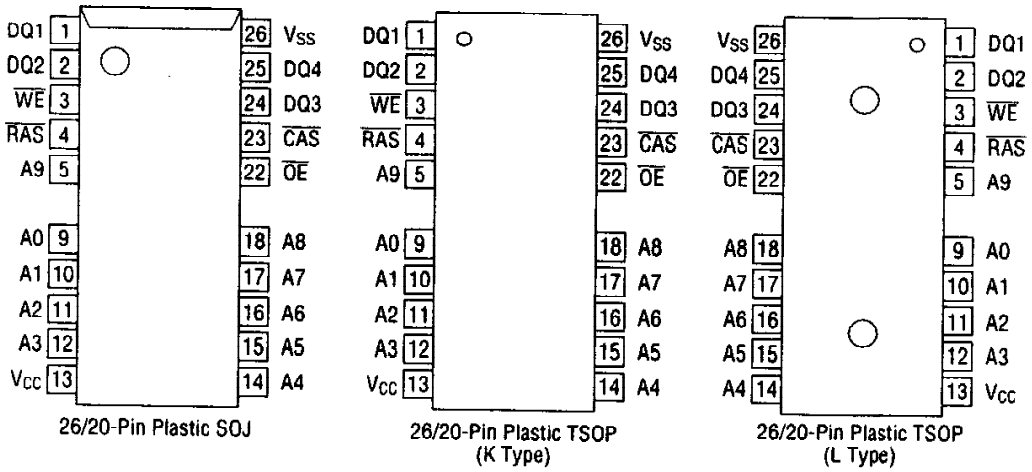
| | | |
|---|---|---|
| 26/20-Pin 300 mil plastic SOJ | (SOJ26/20-P-300) | (Product : MSM51V4400/L/SL-xxSJ) |
| 26/20-Pin 300 mil plastic TSOP | (TSOP26/20-P-300-K) | (Product : MSM51V4400/L/SL-xxTS-K) |
| | (TSOP26/20-P-300-L) | (Product : MSM51V4400/L/SL-xxTS-L) |

xx indicates speed rank.

## PRODUCT FAMILY

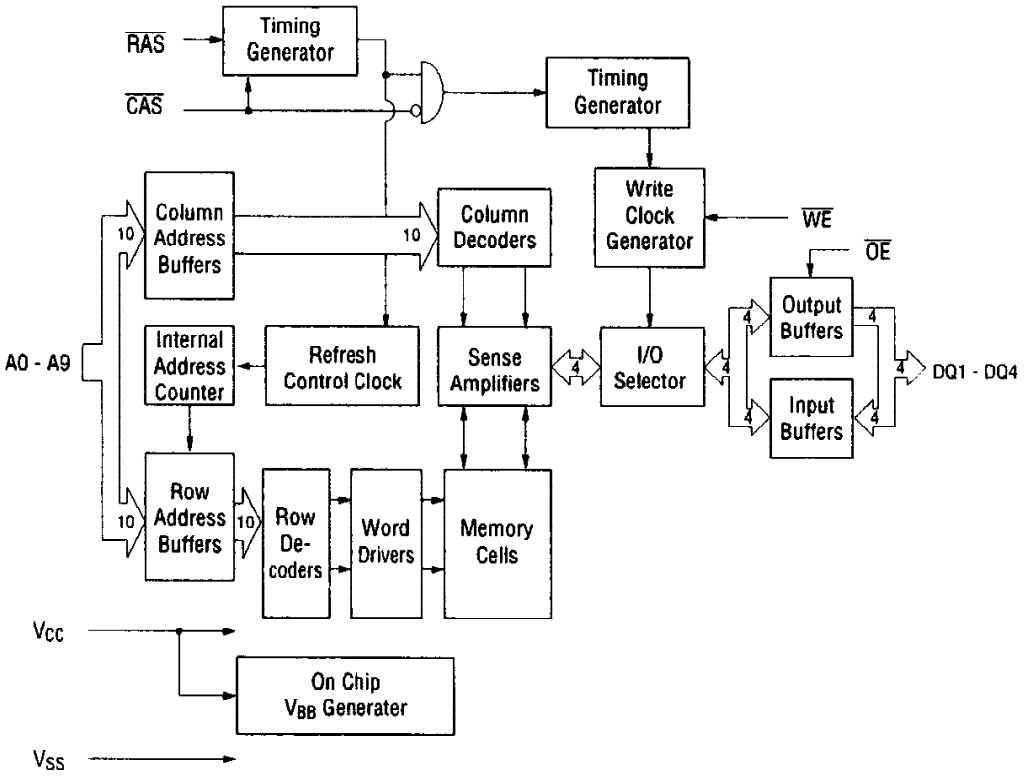
| Family | Access Time (Max.) | | | | Cycle Time (Min.) | Power Dissipation | |
|---|---|---|---|---|---|---|---|
| | $t_{RAC}$ | $t_{AA}$ | $t_{CAC}$ | $t_{OEA}$ | | Operating (Max.) | Standby (Max.) |
| MSM51V4400/L/SL-60 | 60 ns | 30 ns | 15 ns | 15 ns | 110 ns | 252 mW | 1.8 mW/ 0.54 mW (L/SL version) |
| MSM51V4400/L/SL-70 | 70 ns | 35 ns | 20 ns | 20 ns | 130 ns | 234 mW | |
| MSM51V4400/L/SL-80 | 80 ns | 40 ns | 20 ns | 20 ns | 150 ns | 216 mW | |
| MSM51V4400/L/SL-10 | 100 ns | 50 ns | 25 ns | 25 ns | 180 ns | 198 mW | |

## PIN CONFIGURATION (TOP VIEW)




| Pin Name | Function |
|---|---|
| A0 - A9 | Address Input |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| DQ1 - DQ4 | Data Input/Data Output |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power Supply (3.3 V) |
| $V_{SS}$ | Ground (0 V) |

## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$ | −0.5 to 4.6 | V |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |
| Power Dissipation | $P_D$* | 1 | W |
| Operating Temperature | $T_{opr}$ | 0 to 70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to 150 | °C |

*: Ta = 25°C

### Recommended Operating Conditions

(Ta = 0°C to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | −0.3 | — | 0.8 | V |

### Capacitance

($V_{CC}$ = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance (A0 - A9) | $C_{IN1}$ | — | 6 | pF |
| Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) | $C_{IN2}$ | — | 7 | pF |
| Output Capacitance (DQ1 - DQ4) | $C_{I/O}$ | — | 7 | pF |

## DC Characteristics

($V_{CC}$ = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

| Parameter | Symbol | Condition | MSM51V4400 /L/SL-60 | | MSM51V4400 /L/SL-70 | | MSM51V4400 /L/SL-80 | | MSM51V4400 /L/SL-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = −2.0 mA | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2.0 mA | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | |
| Input Leakage Current | $I_{LI}$ | 0 V ≤ $V_I$ ≤ $V_{CC}$ + 0.3 V; All other pins not under test = 0 V | −10 | 10 | −10 | 10 | −10 | 10 | −10 | 10 | µA | |
| Output Leakage Current | $I_{LO}$ | DQ disable 0 V ≤ $V_O$ ≤ $V_{CC}$ | −10 | 10 | −10 | 10 | −10 | 10 | −10 | 10 | µA | |
| Average Power Supply Current (Operating) | $I_{CC1}$ | $\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC}$ = Min. | — | 70 | — | 65 | — | 60 | — | 55 | mA | 1, 2 |
| Power Supply Current (Standby) | $I_{CC2}$ | $\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$ | — | 2 | — | 2 | — | 2 | — | 2 | mA | 1 |
| | | $\overline{RAS}$, $\overline{CAS}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | | |
| | | ≥ $V_{CC}$ −0.2 V | — | 150 | — | 150 | — | 150 | — | 150 | µA | 1, 5 |
| Average Power Supply Current ($\overline{RAS}$-only Refresh) | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{CAS}$ = $V_{IH}$, $t_{RC}$ = Min. | — | 70 | — | 65 | — | 60 | — | 55 | mA | 1, 2 |
| Power Supply Current (Standby) | $I_{CC5}$ | $\overline{RAS}$ = $V_{IH}$, $\overline{CAS}$ = $V_{IL}$, DQ = enable | — | 2 | — | 2 | — | 2 | — | 2 | mA | 1 |
| Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $I_{CC6}$ | $\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$ | — | 70 | — | 65 | — | 60 | — | 55 | mA | 1, 2 |
| Average Power Supply Current (Fast Page Mode) | $I_{CC7}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ cycling, $t_{PC}$ = Min. | — | 55 | — | 50 | — | 45 | — | 40 | mA | 1, 3 |
| Average Power Supply Current (Battery Backup) | $I_{CC10}$ | $t_{RC}$ = 125 µs, $\overline{CAS}$ before $\overline{RAS}$, $t_{RAS}$ ≤ 1 µs | — | 250 | — | 250 | — | 250 | — | 250 | µA | 1, 2, 4, 5 |
| Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $I_{CC9}$ | $\overline{RAS}$ ≤ 0.2 V $\overline{CAS}$ ≤ 0.2 V | — | 200 | — | 200 | — | 200 | — | 200 | µA | 1, 5 |

Notes : 1. $I_{CC}$ Max. is specified as $I_{CC}$ for output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.
4. $V_{CC}$ − 0.2 V ≤ $V_{IH}$ ≤ 4.6 V, −0.3 V ≤ $V_{IL}$ ≤ 0.2 V.
5. L/SL version.

## AC Characteristics (1/2)

($V_{CC}$ = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1, 2, 3, 11, 12

| Parameter | Symbol | MSM51V4400 /L/SL-60 | | MSM51V4400 /L/SL-70 | | MSM51V4400 /L/SL-80 | | MSM51V4400 /L/SL-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 110 | — | 130 | — | 150 | — | 180 | — | ns | |
| Read Modify Write Cycle Time | $t_{RWC}$ | 150 | — | 180 | — | 200 | — | 240 | — | ns | |
| Fast Page Mode Cycle Time | $t_{PC}$ | 40 | — | 45 | — | 50 | — | 60 | — | ns | |
| Fast Page Mode Read Modify Write Cycle Time | $t_{PRWC}$ | 80 | — | 95 | — | 100 | — | 120 | — | ns | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | — | 100 | ns | 4, 5, 6 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | — | 15 | — | 20 | — | 20 | — | 25 | ns | 4, 5 |
| Access Time from Column Address | $t_{AA}$ | — | 30 | — | 35 | — | 40 | — | 50 | ns | 4, 6 |
| Access Time from $\overline{CAS}$ Precharge | $t_{CPA}$ | — | 35 | — | 40 | — | 45 | — | 55 | ns | 4 |
| Access Time from $\overline{OE}$ | $t_{OEA}$ | — | 15 | — | 20 | — | 20 | — | 25 | ns | 4 |
| Output Low Impedance Time from $\overline{CAS}$ | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 4 |
| $\overline{CAS}$ to Data Output Buffer Turn-off Delay Time | $t_{OFF}$ | 0 | 15 | 0 | 20 | 0 | 20 | 0 | 25 | ns | 7 |
| $\overline{OE}$ to Data Output Buffer Turn-off Delay Time | $t_{OEZ}$ | 0 | 15 | 0 | 20 | 0 | 20 | 0 | 25 | ns | 7 |
| Transition Time | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | $t_{REF}$ | — | 16 | — | 16 | — | 16 | — | 16 | ms | |
| Refresh Period (L/SL version) | $t_{REF}$ | — | 128 | — | 128 | — | 128 | — | 128 | ms | |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | 70 | — | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | 100 | 10,000 | ns | |
| $\overline{RAS}$ Pulse Width (Fast Page Mode) | $t_{RASP}$ | 60 | 100,000 | 70 | 100,000 | 80 | 100,000 | 100 | 100,000 | ns | |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 15 | — | 20 | — | 20 | — | 25 | — | ns | |
| $\overline{RAS}$ Hold Time referenced to $\overline{OE}$ | $t_{ROH}$ | 15 | — | 20 | — | 20 | — | 25 | — | ns | |
| $\overline{CAS}$ Precharge Time (Fast Page Mode) | $t_{CP}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 15 | 10,000 | 20 | 10,000 | 20 | 10,000 | 25 | 10,000 | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 60 | — | 70 | — | 80 | — | 100 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{RHCP}$ | 35 | — | 40 | — | 45 | — | 50 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 20 | 45 | 20 | 50 | 20 | 60 | 25 | 75 | ns | 5 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | 20 | 50 | ns | 6 |
| Row Address Set-up Time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | 15 | — | ns | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CAH}$ | 15 | — | 15 | — | 15 | — | 20 | — | ns | |
| Column Address Hold Time from $\overline{RAS}$ | $t_{AR}$ | 50 | — | 55 | — | 60 | — | 75 | — | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | 50 | — | ns | |

## AC Characteristics (2/2)

($V_{CC}$ = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1, 2, 3, 11, 12

| Parameter | Symbol | MSM51V4400 /L/SL-60 | | MSM51V4400 /L/SL-70 | | MSM51V4400 /L/SL-80 | | MSM51V4400 /L/SL-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Read Command Set-up Time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | |
| Read Command Hold Time | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 8 |
| Write Command Set-up Time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 9 |
| Write Command Hold Time | $t_{WCH}$ | 10 | — | 10 | — | 10 | — | 15 | — | ns | |
| Write Command Hold Time from $\overline{RAS}$ | $t_{WCR}$ | 45 | — | 50 | — | 60 | — | 75 | — | ns | |
| Write Command Pulse Width | $t_{WP}$ | 10 | — | 10 | — | 10 | — | 15 | — | ns | |
| $\overline{OE}$ Command Hold Time | $t_{OEH}$ | 15 | — | 20 | — | 20 | — | 25 | — | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 15 | — | 20 | — | 20 | — | 25 | — | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 15 | — | 20 | — | 20 | — | 25 | — | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns | 10 |
| Data-in Hold Time | $t_{DH}$ | 15 | — | 15 | — | 15 | — | 20 | — | ns | 10 |
| Data-in Hold Time from $\overline{RAS}$ | $t_{DHR}$ | 50 | — | 55 | — | 60 | — | 75 | — | ns | |
| $\overline{OE}$ to Data-in Delay Time | $t_{OED}$ | 15 | — | 20 | — | 20 | — | 25 | — | ns | |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 35 | — | 45 | — | 45 | — | 55 | — | ns | 9 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 50 | — | 60 | — | 65 | — | 80 | — | ns | 9 |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 80 | — | 95 | — | 105 | — | 130 | — | ns | 9 |
| $\overline{CAS}$ Precharge $\overline{WE}$ Delay Time | $t_{CPWD}$ | 60 | — | 70 | — | 75 | — | 85 | — | ns | 9 |
| $\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge | $t_{RPC}$ | 5 | — | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CHR}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ Precharge Time (Refresh Counter Test) | $t_{CPT}$ | 30 | — | 35 | — | 40 | — | 50 | — | ns | |
| $\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{WRP}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode) | $t_{WTS}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode) | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $t_{RASS}$ | 100 | — | 100 | — | 100 | — | 100 | — | µs | 13 |
| $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $t_{RPS}$ | 110 | — | 130 | — | 150 | — | 180 | — | ns | 13 |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $t_{CHS}$ | 40 | — | 50 | — | 60 | — | 70 | — | ns | 13 |

Notes:

1. A start-up delay of 200 μs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume $t_T$ = 5 ns.

3. $V_{IH}$ (Min.) and $V_{IL}$ (Max.) are reference levels for measuring input timing signals. Transition times ($t_T$) are measured between $V_{IH}$ and $V_{IL}$.

4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. Output timing reference levels are $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.

5. Operation within the $t_{RCD}$ (Max.) limit ensures that $t_{RAC}$ (Max.) can be met. $t_{RCD}$ (Max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (Max.) limit, access time is controlled by $t_{CAC}$.

6. Operation within the $t_{RAD}$ (Max.) limit ensures that $t_{RAC}$ (Max.) can be met. $t_{RAD}$ (Max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (Max.) limit, access time is controlled by $t_{AA}$.

7. $t_{OFF}$ (Max.) and $t_{OEZ}$ (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

9. $t_{WCS}$, $t_{CWD}$, $t_{RWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle, and to $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle or a read modify write cycle.

11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

13. Only SL version.

**See ADDENDUM K for AC Timing Waveforms**