

# OKI Semiconductor

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## MSM534052E

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262,144-Words x 16-bit or 524,288-Bytes x 8-bit MaskROM

8Words x 16-Bit or 16Bytes x 8-Bit/Page Mode MASKROM

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### ■ DESCRIPTION

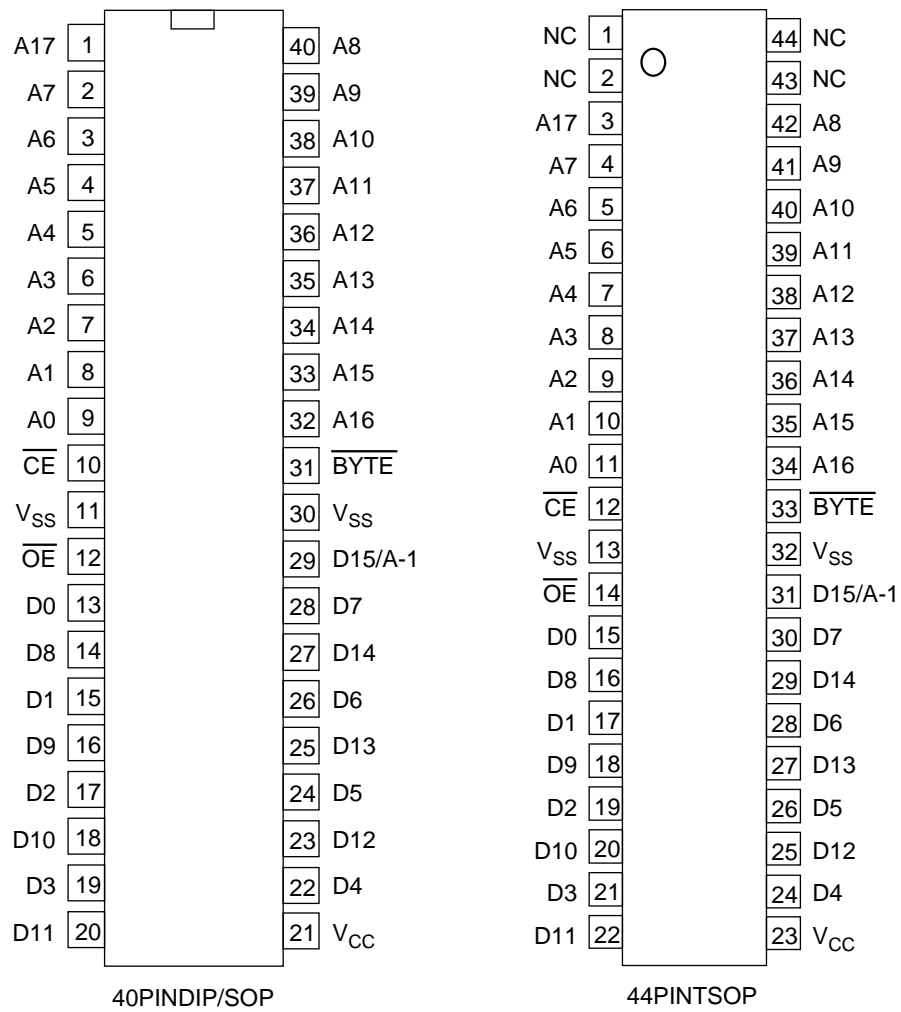
The OKI MSM534052E is a 262,144-words x 16-bit or 1,048,576-Bytes x 8-bit CMOS Mask ROM with an asynchronous page read mode. Each page is organized 8 words x 16-bit or 16 words x 8-bit. It operates on a single 5.0V power supply and is TTL compatible. The chip's asynchronous I/O requires no external clock assuring easy operation. A power-down mode provides low power dissipation when the chip is not selected. The CE and OE pins are provided as control signals that permit three-stated output allowing easy memory expansion on a system bus. The MSM534052E is suited for use as large capacity fixed memory for microcomputers and data terminals.

### ■ FEATURES

- Single 5.0V power supply
- 262,144-words x 16-bit / 524,288-Bytes x 8-bit
- 8-words(A2,A1,A0) or 16-Bytes(A2,A1,A0,A-1) / Page
- Access time
  - 80ns Max (Normal access)
  - 50ns Max (Page access)
- Input/Output TTL compatible
- Tri-State output configurations
- Internal powerdown function
- Packages:

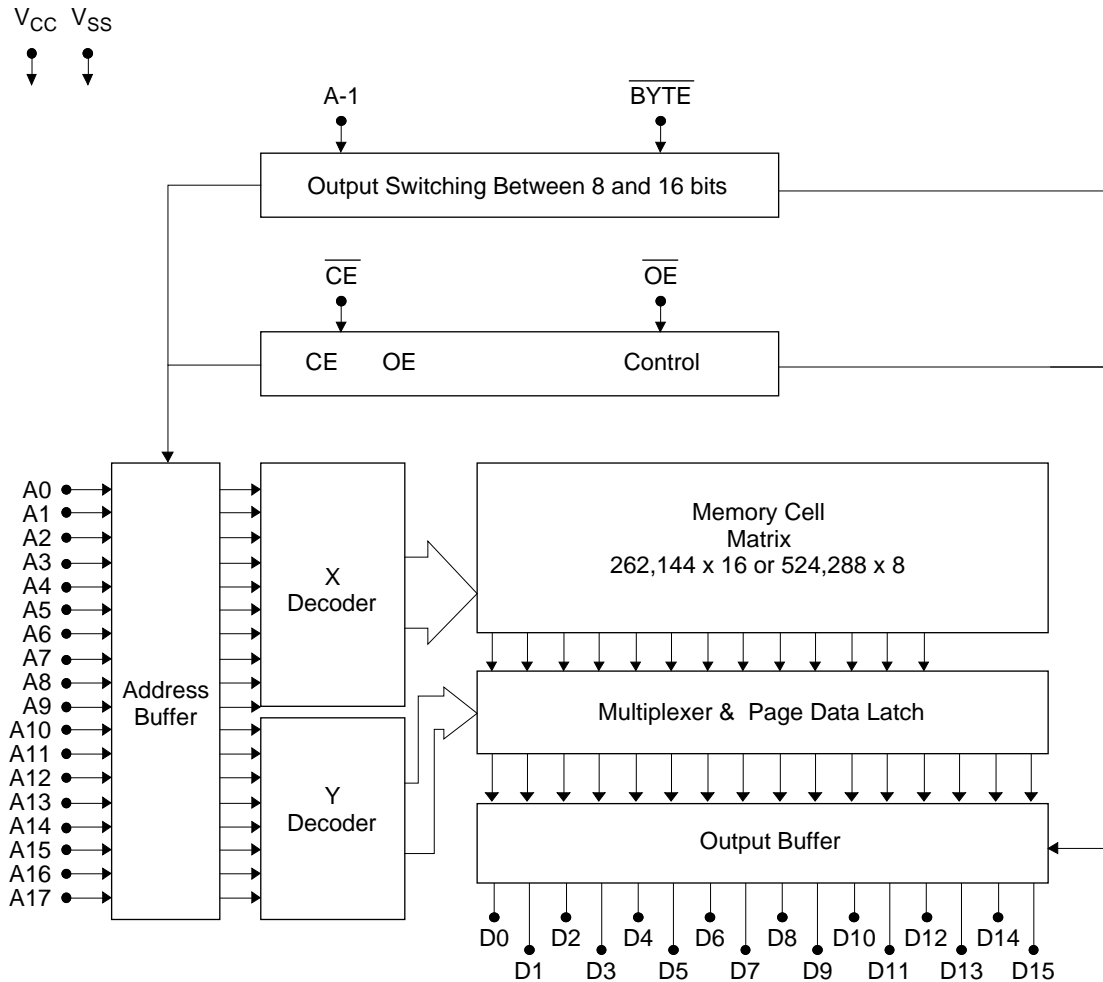
40-PIN PLASTIC DIP	(DIP40-P-600-2.54)	(MSM534052E-xxRS)
40-PIN PLASTIC SOP	(SOP40-P-525-1.27-K)	(MSM534052E-xxGS-AK)
44-PIN PLASTIC TSOP	(TSOPII44-P-400-0.80-K)	(MSM534052E-xxTS-AK)
- Pin compatible OTP available

## PIN CONFIGURATION



Pin Name	Function
D15/A-1	Data output / address input
A0 to A17	Address input
D0 to D15	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{BYTE}$	Mode switch
$V_{CC}, V_{SS}$	Power supply

## BLOCK DIAGRAM



## FUNCTION TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A-1/D15	D0—D7	D8—D15	$D_{OUT}$ Mode	LSB	MSB
H	X	X	X	Hi-Z	Hi-Z	Hi-Z	—	—
L	H	X	X	Hi-Z	Hi-Z		—	—
L	L	H	Input Inhibited (D15)	D0 to D7	D8 to D15	16 bit	A0	A17
L	L	H	Input Inhibited (D15)	D0 to D7	D8 to D15	16 bit(Page Mode)	A0	A2
L	L	L	L	D0 to D7	Hi-Z	8 bit	A-1	A17
L	L	L	H	D8 to D15	Hi-Z		A-1	A17
L	L	L	L	D0 to D7	Hi-Z	8 bit(Page Mode)	A-1	A2
L	L	L	H	D8 to D15	Hi-Z		A-1	A2

## ABSOLUTE MAXIMUM LIMITS

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	$V_{CC}$	to $V_{SS}$	-0.3 to 7	V
Input Voltage	$V_I$		-0.3 to $V_{CC} + 0.5$	V
Output Voltage	$V_O$		-0.3 to $V_{CC} + 0.5$	V
Power Dissipation	$P_D$	Per Package $T_{opr} = 25^\circ\text{C}$	1.0	W
Operating Temperature	$T_{opr}$	—	0 to 70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	—	-55 to 150	$^\circ\text{C}$

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	$V_{CC}$	—	4.5	5.0	5.5	V
	$V_{SS}$	—	0.0	0.0	0.0	V
"H" Input Voltage	$V_{IH}$	—	2.2	5.0	5.5	V
"L" Input Voltage	$V_{IL}$	—	-0.3	0.0	0.8	V
Operating Temperature	$T_{opr}$	—	0	—	70	$^\circ\text{C}$

## DC CHARACTERISTICS

 $(V_{CC} = 5V \pm 10\%, T_a = 0 \text{ to } 70^\circ\text{C})$ 

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
"H" Output Voltage	$V_{OH}$	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
"L" Output Voltage	$V_{OL}$	$I_{OH} = 2.1\text{mA}$	—	—	0.4	V
Input Leakage Current	$I_{LI}$	$V_I = 0 \text{ to } V_{CC}$	-10	—	10	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$V_O = 0 \text{ to } V_{CC}$ $\overline{CE} = V_{IH\text{MIN}}$	-10	—	10	$\mu\text{A}$
Power Supply Current (Operating)	$I_{CC}$	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}, t_C = 100\text{ns}$	—	—	80	mA
Power Supply Current (Standby)	$I_{CCS1}$	$\overline{CE} = V_{CC} - 0.2\text{V}$	—	—	50	$\mu\text{A}$
	$I_{CCS}$	$\overline{CE} = V_{IH\text{MIN}}$	—	—	500	$\mu\text{A}$

## AC CHARACTERISTICS

Test conditions

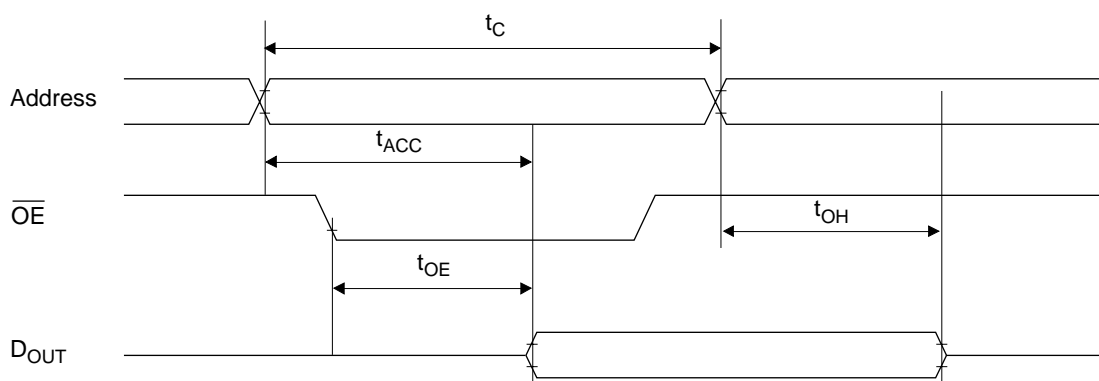
Parameter	Conditions
Input Signal Level	$V_{IH}=3.0V, V_{IL}=0.0V$
Transition Time	$t_r=t_f=5ns$
Timing Reference Level	Input Voltage=1.5V Output Voltage=0.8V&2.0V
Load Condition	CL=100pF+1TTL

## Read Cycle

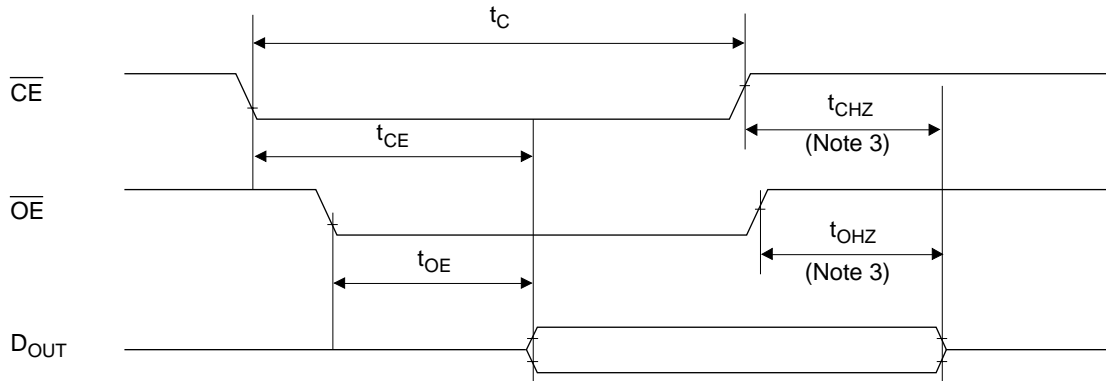
(Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Random Access Cycle time	$t_C$	—	80	—	—	ns
Random Address Access time	$t_{ACC}$	—	—	—	80	ns
Page Set up time	$t_{PSET}$	—	100	—	—	ns
Page Access Cycle time	$t_{PC}$	—	50	—	—	ns
Page Access time	$t_{PAC}$	—	—	—	50	ns
CE Access time	$t_{CE}$	—	—	—	80	ns
OE Access time	$t_{OE}$	—	—	—	80	ns
CE Output Disable time	$t_{CHZ}$	—	0	—	35	ns
OE Output Disable time	$t_{OHZ}$	—	0	—	30	ns
Output Hold time	$t_{OH}$	—	0	—	—	ns

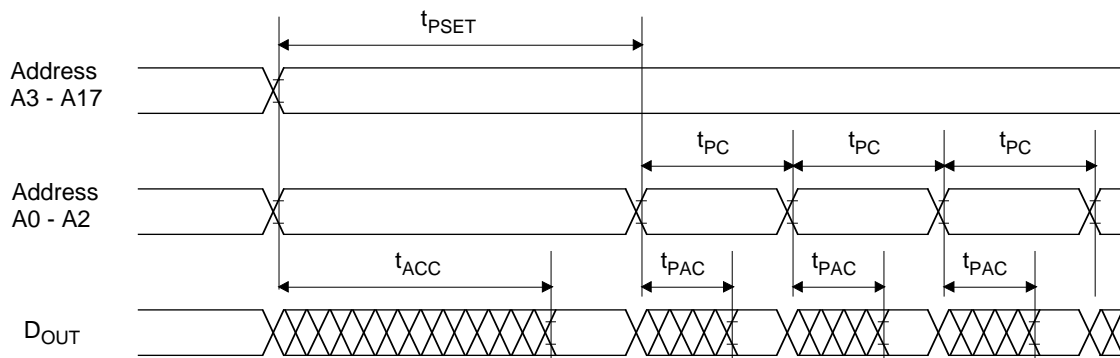
## Read Cycle (Note1)



## Read Cycle (Note2)



## Page Mode Read Cycle (Note4)



- Note)
1.  $\overline{CE}$  is low level.
  2. Address is fixed before or at the same time when  $\overline{CE}$  level falls.
  3.  $t_{CHZ}$  &  $t_{OHZ}$  indicate the time until floating. They are not determined by the output level.
  4.  $\overline{CE}$  is low level and  $\overline{OE}$  is low level.

## I/O CAPACITANCE

Parameter	Symbol	Conditions	Rated Value			Unit
			Min.	Typ.	Max.	
Input Capacitance	$C_I$	$V_I=0V$	—	—	8	pF
Output Capacitance	$C_O$	$V_O=0V$	—	—	10	pF

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