OKI Semiconductor

Technical Information

MSM5416250 - OKI SUPER HIGH SPEED GRAPHICS DRAM -

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5416250 is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5416250 is especially designed for high performance PC graphics. The MSM5416250 is not developed for medical use or long time data-storage applications. The MSM5416250 achieves high integration, high-speed operation,and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5416250 is available in a40-pin plastic SOJ.

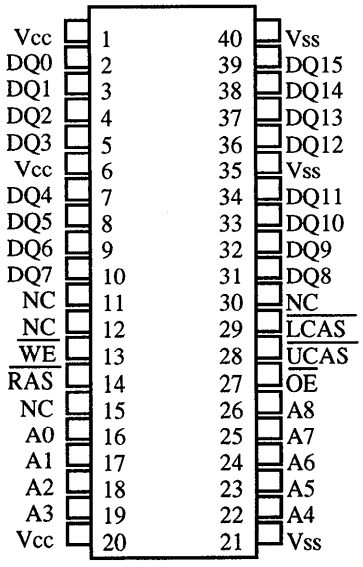
FEATURES

- 262,144-word by 16-bit configuration
- Single 5V power supply, ±10% tolerance
- Input :TTL compatible
- Output :TTL compatible, 3-state
- Refresh : 512 cycles/8ms
- Fast page mode with EDO,read modify write capability
- Byte wide control: 2 CAS control
- CAS before RAS refresh, Hidden refresh, RAS only refresh capability
- Pachage : 40-Pin 400 mil plastic SOJ (SOJ40-P-400)
  (Product : MSM5416250-xxJS) xx : indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	t_{RC}	t_{HPC}	
MSM5416250-25	25ns	12ns	8ns	8ns	45ns	10ns	1485mW
MSM5416250-27	27ns	15ns	9ns	9ns	48ns	10.5ns	1485mW

PIN CONFIGURATION (TOP VIEW)



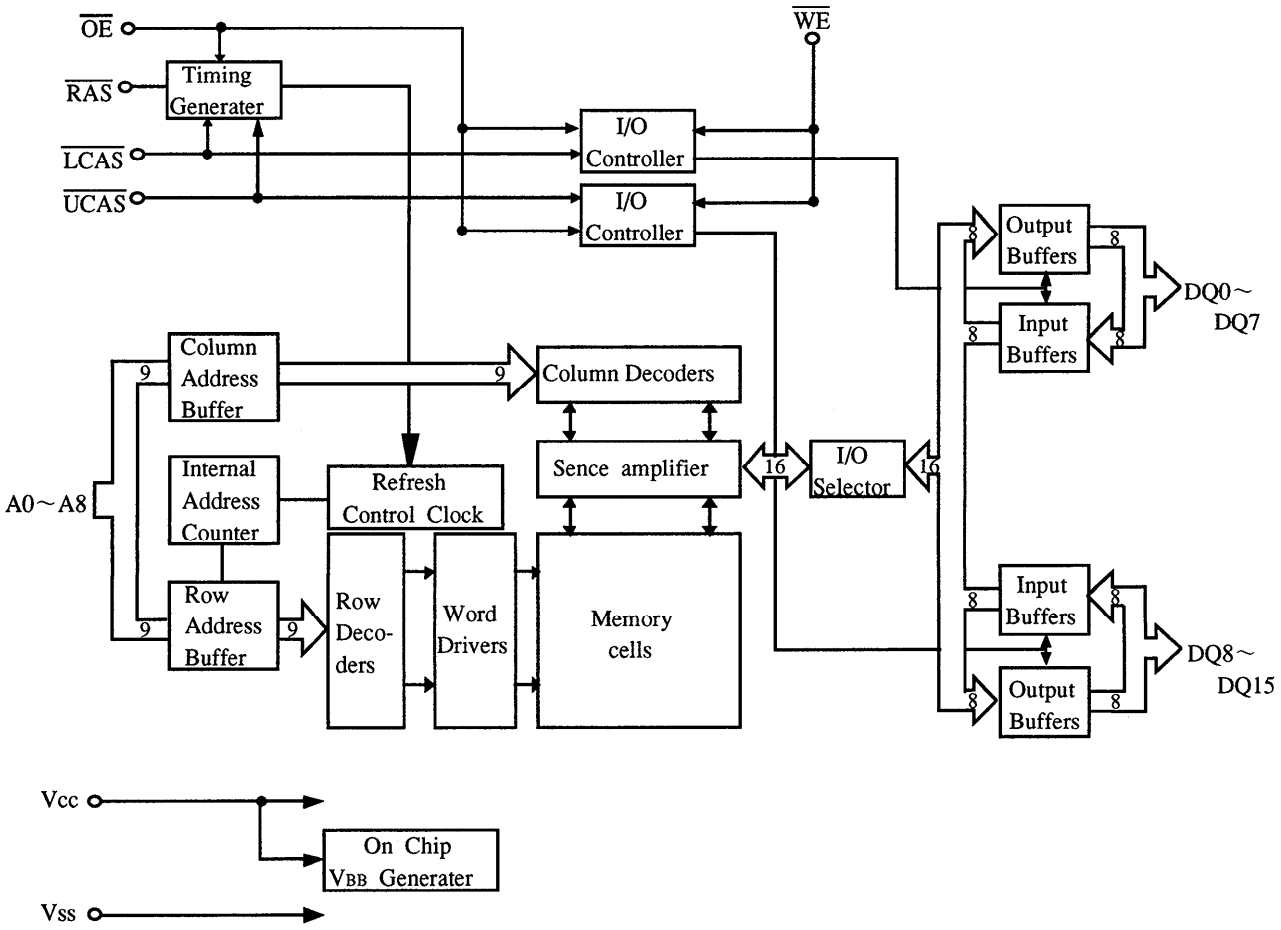
40Pin 400mil SOJ

Pin Names	Function
A0-A8	Address Input
RAS	Row Address Strobe
LCAS,UCAS	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
WE	Write Enable
OE	Output Enable
Vcc	Power Supply (+5V)
Vss	Ground (0V)
NC	No Connection

Note1 : The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must beprovideded to every Vss pin.

REVISION-4 1998. 5.21

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functinal Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	DOUT	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	DOUT	Upper Byte Read
L	L	L	H	L	DOUT	DOUT	Word Read
L	L	H	L	H	DIN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DIN	Upper Byte Write
L	L	L	L	H	DIN	DIN	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25℃	-1.0～+7.0	V
Short circuit output current	Ios	Ta=25℃	50	mA
Power dissipation	P_D	Ta=25℃	1.5	W
Operrating temperrature	Topr	—	0～+70	℃
Storage temperature	Tstg	—	-55～+150	℃

Recommended Operating Conditions

(Ta=0℃ to 70℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	4.5	5.0	5.5	V
	Vss	—	0	0	0	V
Input high voltage	V_{IH}	—	3.0	—	Vcc+1	V
Input low voltage	V_{IL}	—	0.5	—	0	V

Capacitance

(Vcc=5V±10%,Ta=25℃,f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0～A8)	C_{IN1}	—	—	5	pf
Input capacitance ($\overline{RAS}$,$\overline{LCAS}$,$\overline{UCAS}$,$\overline{WE}$,$\overline{OE}$)	C_{IN2}	—	—	5	pf
Input / output capacitance (DQ0～DQ15)	$C_{I/O}$	—	—	7	pf

DC CHARACTERISTICS

(Vcc=5V±10% , Ta=0 to 70℃)

Parameter	Symbol	Condition	MSM5416250 -25		MSM5416250 -27		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH}= - 1.0mA	2.4	V_{cc}	2.4	V_{cc}	V	
Output Low Voltage	V_{OL}	I_{OL}= 2.0mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V≦V_{IN}≦Vcc	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQi Disable 0V≦V_o≦5.5V	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=Min.	-	270	-	270	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	-	3	-	3	mA	1
Average Power Supply Current ($\overline{RAS}$ only Refresh)	I_{CC3}	$\overline{RAS}$=Cycling $\overline{CAS}$=V_{IH} t_{RC}=Min.	-	270	-	270	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$=V_{IL} $\overline{CAS}$ Cycling t_{HPC}=Min.	-	270	-	270	mA	1,3
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$=Cycling $\overline{CAS}$ Befor $\overline{RAS}$	-	270	-	270	mA	1,2

Notes : 1. Icc Max. is specified as Icc for the output open cindition.
2. Address can be changed once or less while RAS = VIL.
3. Address can be changed once or less while CAS = VIH.

AC CHARACTERISTICS (1/2)

(Vcc = 5V ± 10%, Ta = 0~70℃)

Parameter	Symbol	MSM5416250 -25		MSM5416250 -27		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	tRC	45	—	48	—	ns	
Read/Write cycle time	tRMW	65	—	70	—	ns	
Hyper page mode cycle time	tHPC	10	—	10.5	—	ns	
Fast page mode read/write cycle time	tPRMW	32	—	34	—	ns	
Access time from $\overline{RAS}$	tRAC	—	25	—	27	ns	7,12,13
Access time from $\overline{CAS}$	tCAC	—	8	—	9	ns	7,12
Access time from column address	tAA	—	12	—	15	ns	7,13
Access time from $\overline{OE}$	tOEA	—	8	—	9	ns	
Access time from $\overline{CAS}$ precharge	tCPA	—	14	—	17	ns	7,12
Data hold after $\overline{CAS}$ low	tCOH	3	—	5	—	ns	17
Output buffer turn-off delay time	tOFF	3	6	3	7	ns	8
$\overline{OE}$ to data output buffer turn-off delay time	tOEZ	3	6	3	7	ns	8
$\overline{RAS}$ to data output buffer turn-off delay time	tREZ	3	6	3	7	ns	8
$\overline{WE}$ to data output buffer turn-off delay time	tWEZ	3	8	3	10	ns	8
Transition time	tT	0.5	35	0.5	35	ns	
Refresh preiod	tREF	—	8	—	8	ms	
$\overline{RAS}$ precharge time	tRP	15	—	17	—	ns	
$\overline{RAS}$ pulse width	tRAS	25	10,000	27	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	tRASP	25	100,000	27	100,000	ns	
$\overline{RAS}$ hold time	tRSH	7	—	7	—	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	tROH	7	—	7	—	ns	
$\overline{CAS}$ precharge time	tCP	4	—	5	—	ns	
$\overline{CAS}$ pulse width	tCAS	4	10,000	5	10,000	ns	
$\overline{CAS}$ hold time	tCSH	20	—	22	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	10	17	10	19	ns	12
$\overline{RAS}$ to column address delay time	tRAD	8	13	8	13	ns	
Row address set-up time	tASR	0	—	0	—	ns	13
Row address hold time	tRAH	6	—	6	—	ns	
Column address set-up time	tASC	0	—	0	—	ns	
Column address hold time	tCAH	5	—	5	—	ns	
Column address hold time from $\overline{RAS}$	tAR	19	—	21	—	ns	
Column address to $\overline{RAS}$ lead time	tRAL	12	—	15	—	ns	
Read command set-up time	tRCS	0	—	0	—	ns	9
Read command hold time	tRCH	0	—	0	—	ns	
Read command hold time reference to $\overline{RAS}$	tRRH	0	—	0	—	ns	9
$\overline{WE}$ pulse width	tWEP	10	—	10	—	ns	

AC CHARACTERISTICS (2/2)

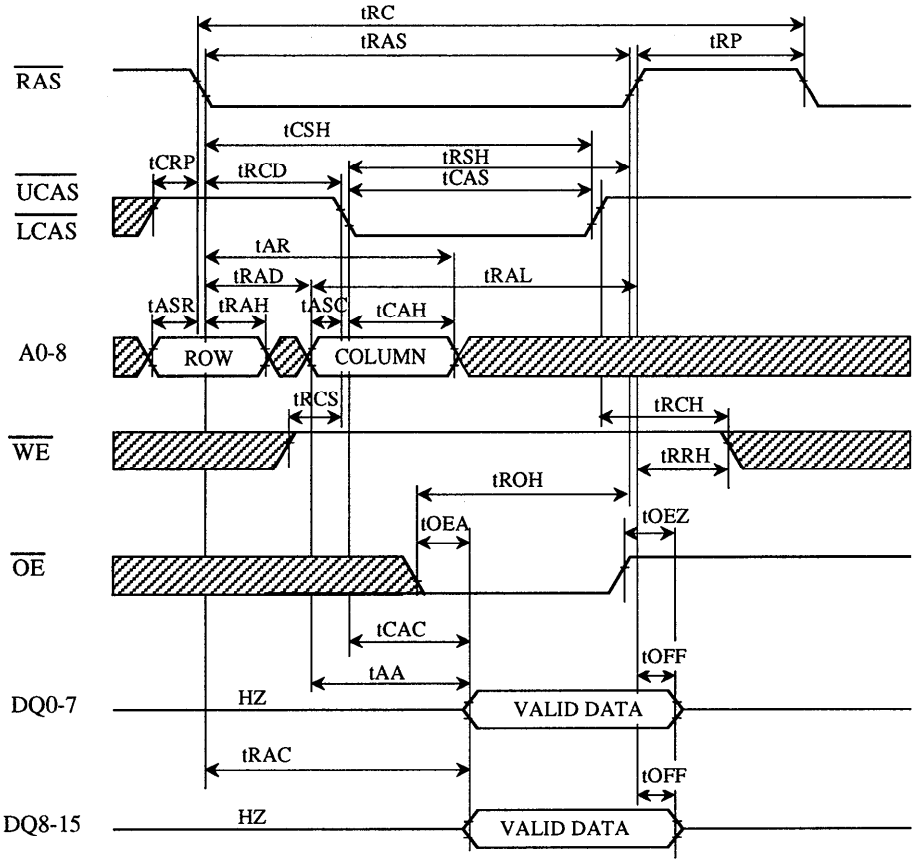
(Vcc = 5V ± 10%, Ta = 0~70℃)

Parameter	Symbol	MSM5416250 -25		MSM5416250 -27		Unit	Note
		MIN	MAX	MIN	MAX		
Write command set-up time	tWCS	0	–	0	–	ns	
Write command hold time	tWCH	5	–	5	–	ns	
Write command pulse width	tWP	5	–	5	–	ns	
Write command hold time from $\overline{RAS}$	tWCR	19	–	21	–	ns	
$\overline{OE}$ command hold time	tOEH	5	–	5	–	ns	
Write command to $\overline{CAS}$ lead time	tCWL	5	–	5	–	ns	
Write command to $\overline{RAS}$ lead time	tRWL	7	–	7	–	ns	
Data to $\overline{CAS}$ delay time	tDZC	0	–	0	–	ns	
Data to $\overline{OE}$ delay time	tDZO	0	–	0	–	ns	
Data-in set-up time	tDS	0	–	0	–	ns	10
Data-in hold time	tDH	5	–	5	–	ns	10
Data-in hold time referenced to $\overline{RAS}$	tDHR	19	–	21	–	ns	
$\overline{OE}$ to Data-in delay time	tOED	7	–	7	–	ns	
$\overline{OE}$ "L" to $\overline{CAS}$ "H" lead time	tOCH	5	–	5	–	ns	
$\overline{CAS}$ "H" to $\overline{OE}$ "L" lead time	tCHO	5	–	5	–	ns	
Hi-Z command pulse width	tOEP	5	–	5	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	17	–	18	–	ns	11
Column address to $\overline{WE}$ delay time	tAWD	21	–	24	–	ns	11
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	34	–	37	–	ns	11
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	tRPC	0	–	0	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	tCSR	5	–	5	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	tCHR	7	–	7	–	ns	

Notes:

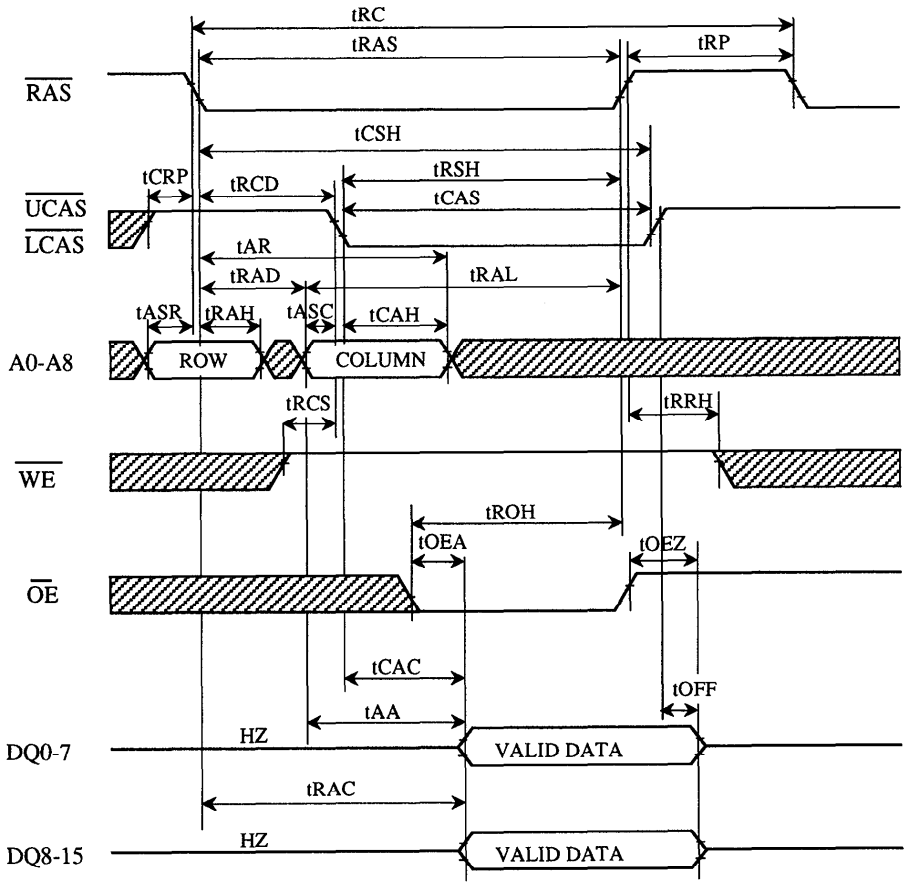
1. All voltages are referenced to Vss.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200 μ s is required after power-up, followed by any 8$\overline{RAS}$ cycles. (Example: $\overline{RAS}$-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8$\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8$\overline{RAS}$ cycles are required.
5. The AC characteristics assume t_T=5ns.
6. V_{IH} (Min.)and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 30 pF. DOUT reference levels: V_{OH}/V_{OL}=1.8V/1.4V.
8. t_{REZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referebced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leadind edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (Min.), $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{AWD} \geqq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indetermunate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CDC}.
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS}$ =V_{IL}.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS}$ =V_{IH} and $\overline{RAS}$ =V_{IL}.
17. This is guaranteed by design. (t_{COH}=t_{CAC} - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

READ CYCLE ($\overline{RAS}$ output control)



: "H" or "L"

READ CYCLE ($\overline{\text{CAS}}$ output control)



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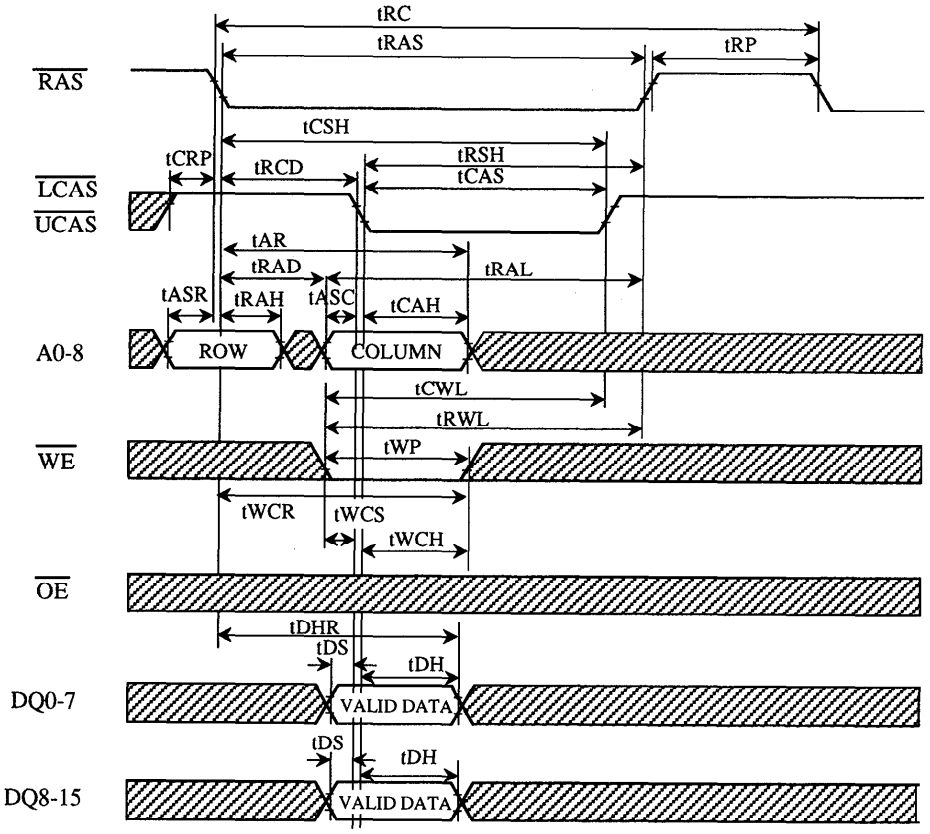
EARLY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



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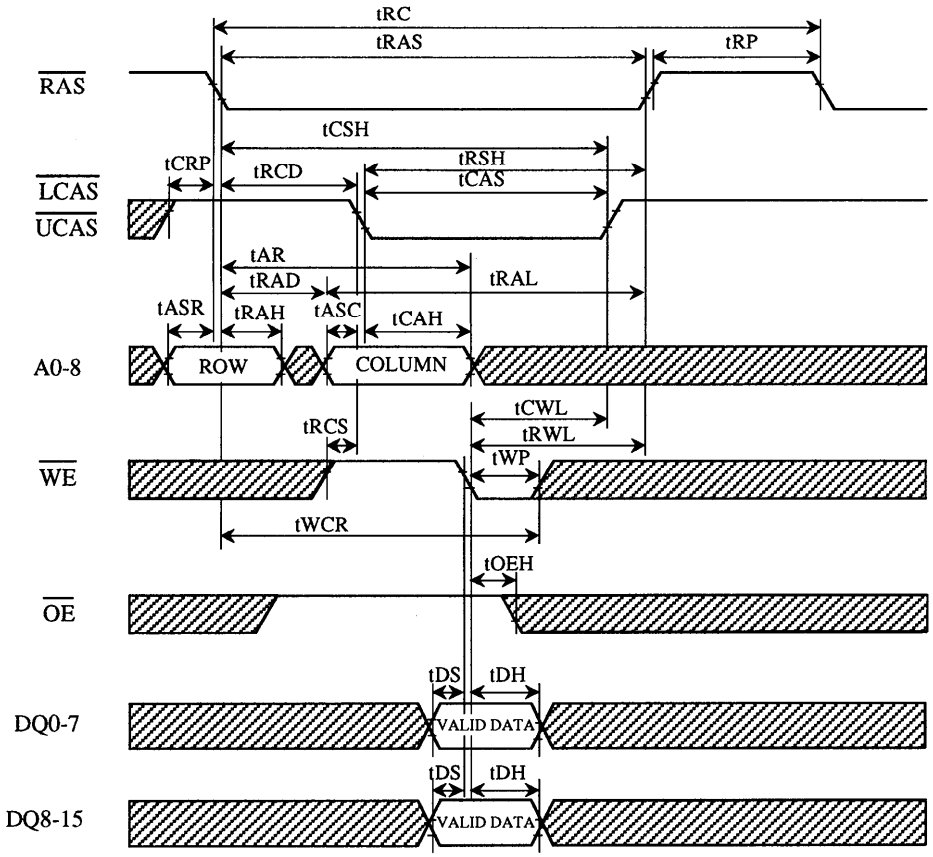
LATE WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



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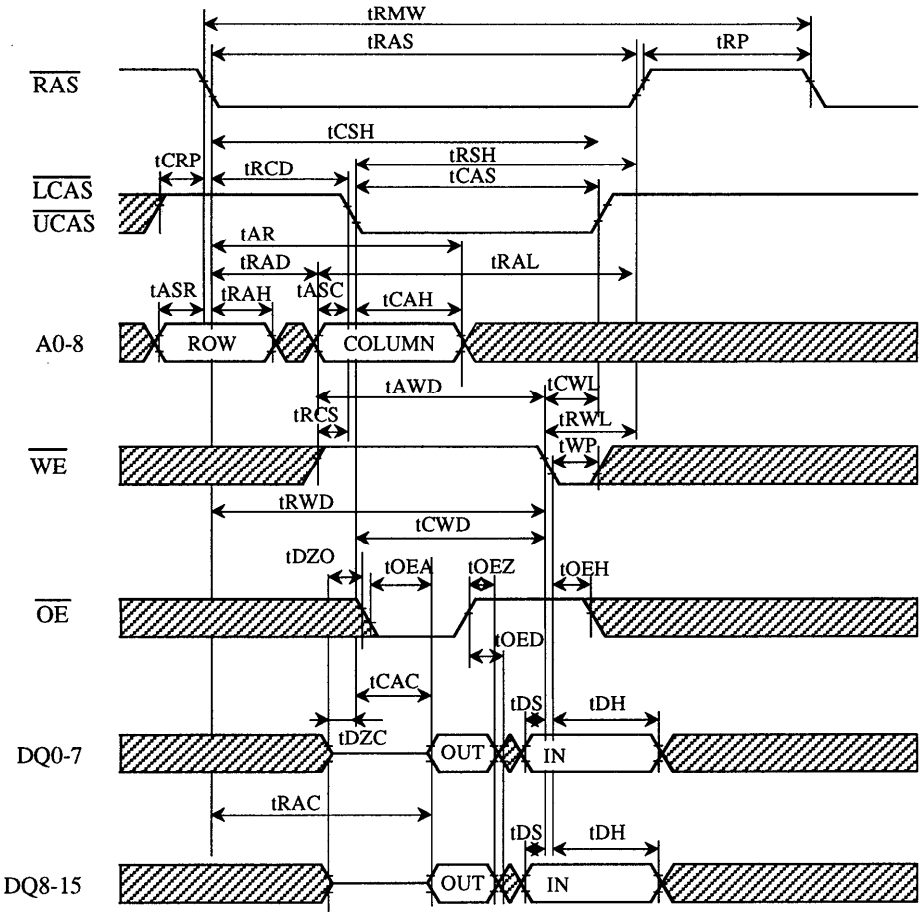
READ MODIFY WRITE CYCLE (LCAS and UCAS active)



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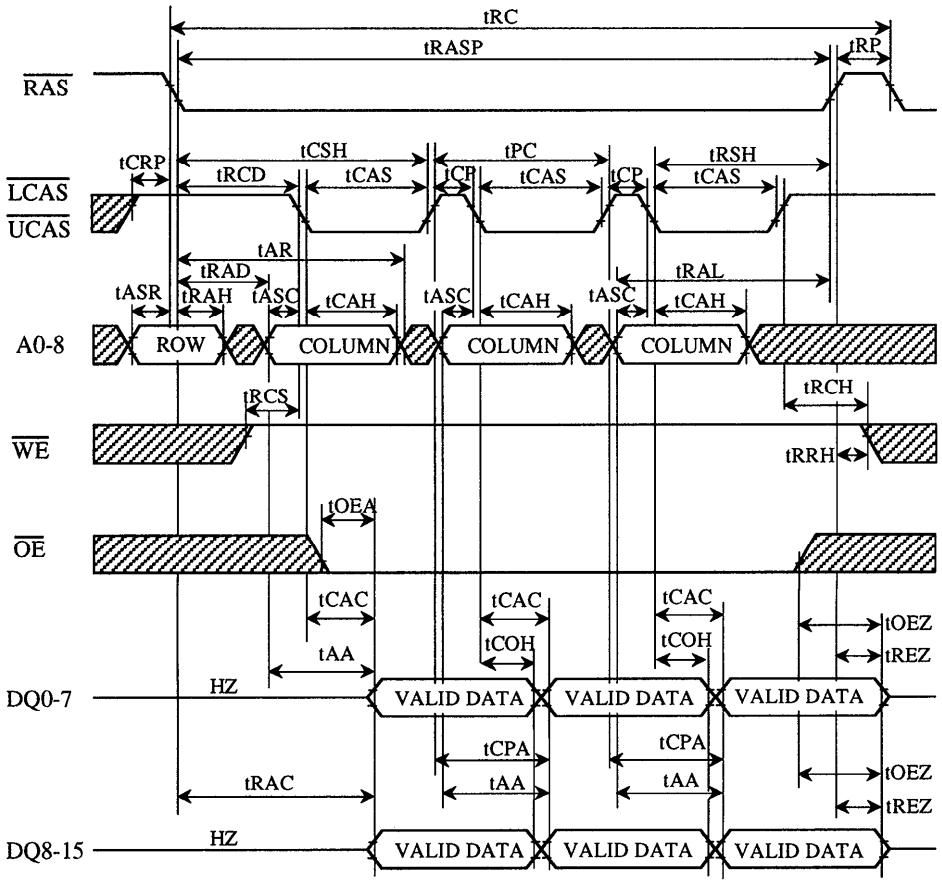
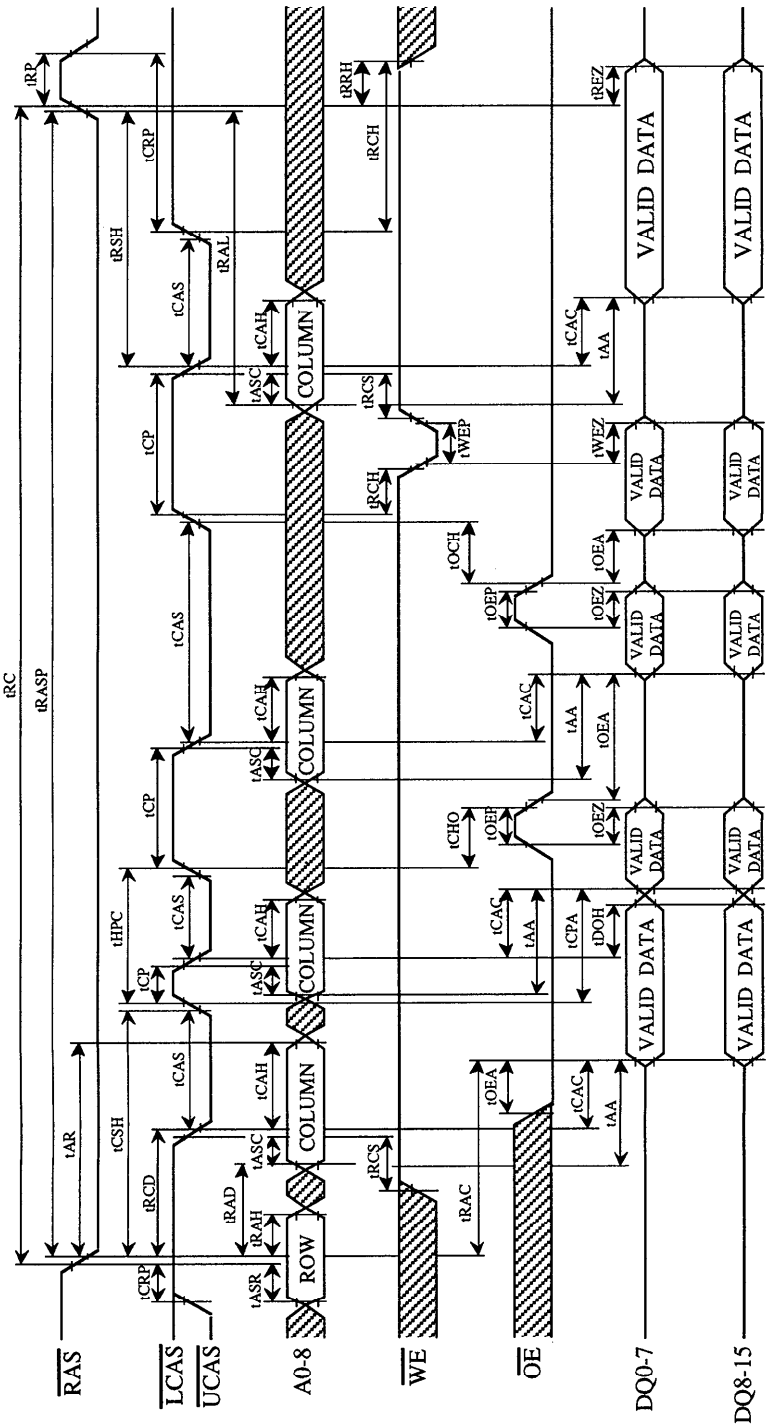
FAST PAGE MODE READ CYCLE with Extended Data Out



FAST PAGE MODE READ Hi-Z OPERATION



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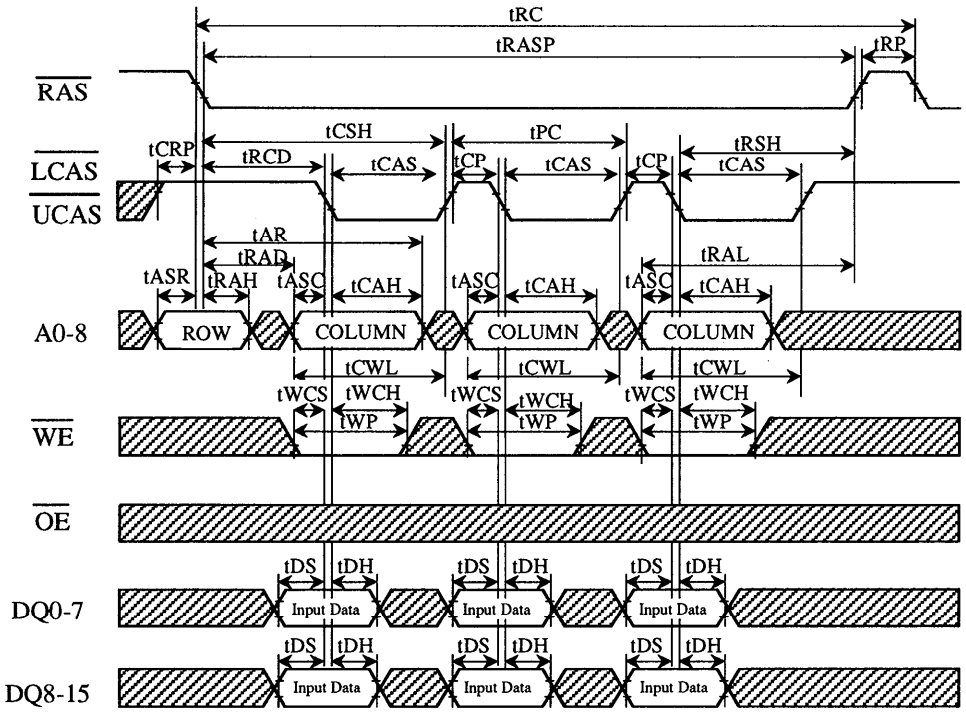
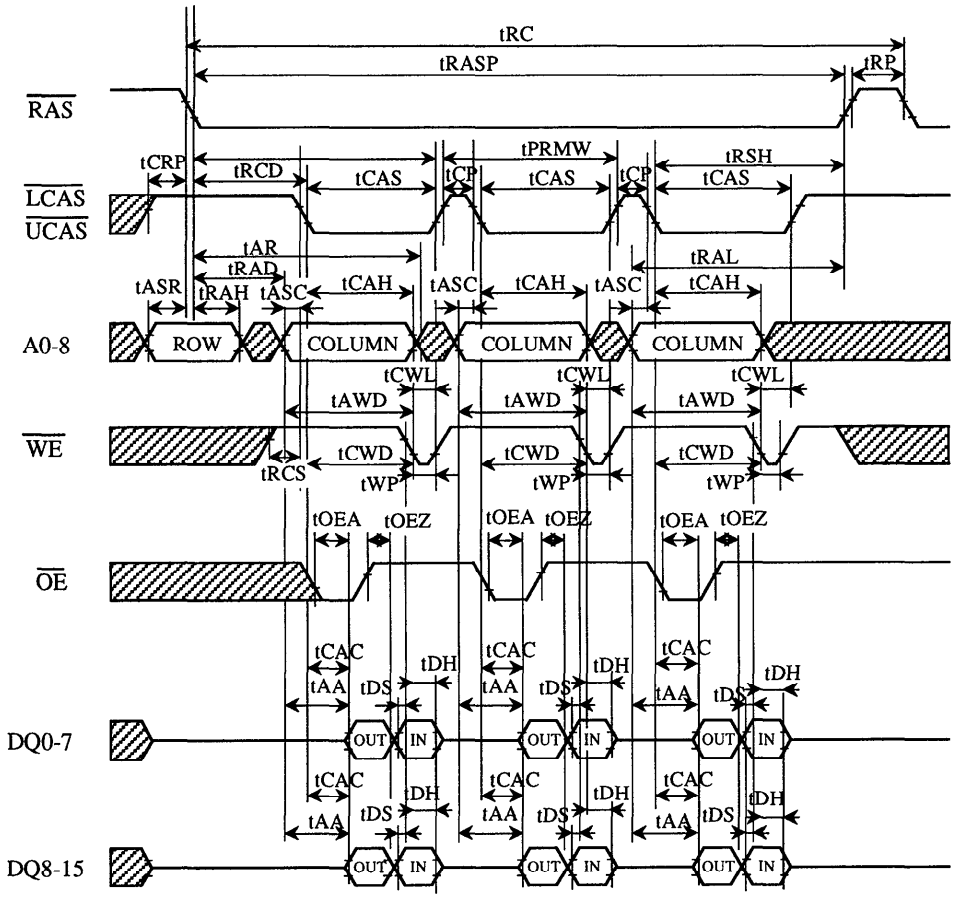
FAST PAGE MODE EARLY WRITE CYCLE



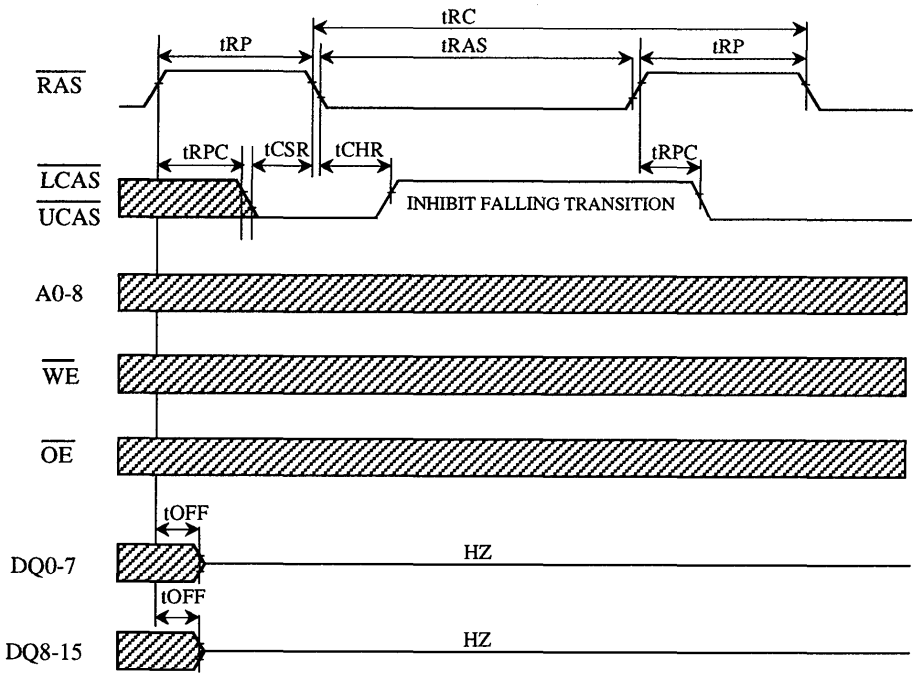
▨ : "H" or "L"

FAST PAGE MODE READ MODIFY WRITE CYCLE



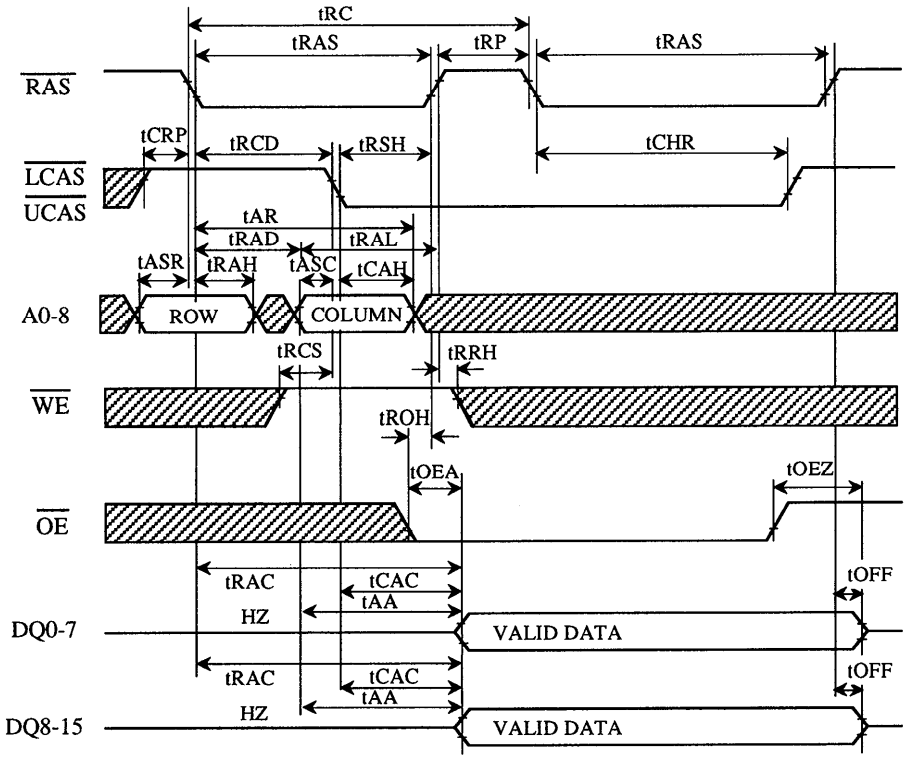
: "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



: "H" or "L"

HIDDEN REFRESH CYCLE



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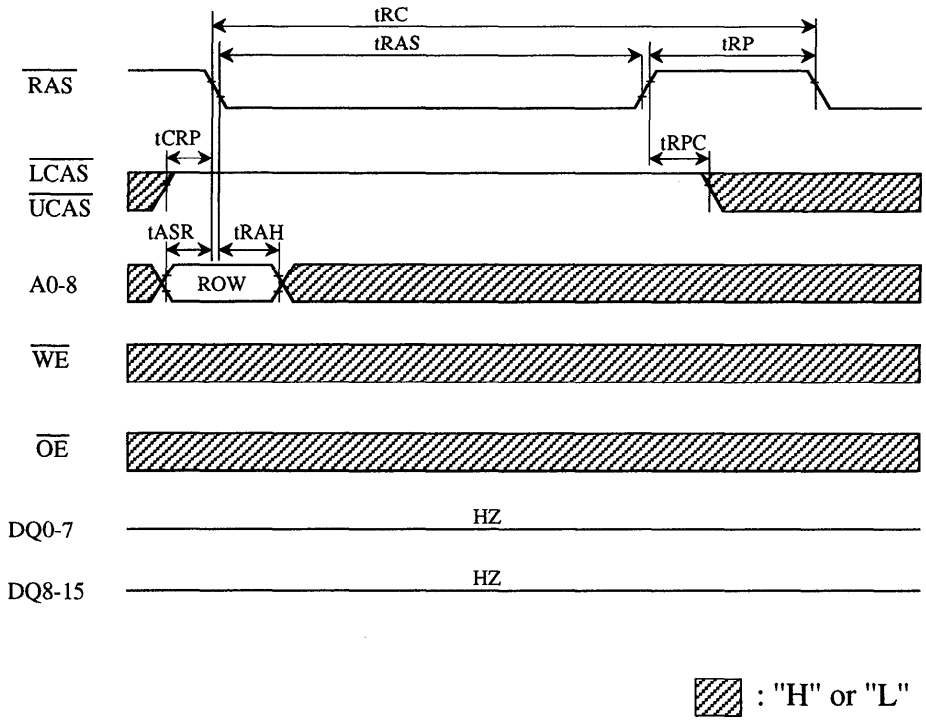
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



: "H" or "L"