PRELIMINARY

OKI Semiconductor

REVISION-2 1996.11.2

MSM54V16255A/SL

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM54V16255A/SL is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM54V16255A/SL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM54V16255A/SL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

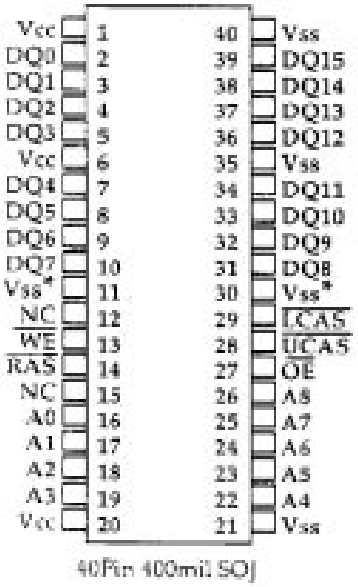
FEATURES

- 262,144-word × 16-bit configuration
- Single 3.3V power supply, ±0.3V tolerance
- Input :LVTTL compatible, low input capacitance
- Output :LVTTL compatible, 3-state
- Refresh : 512 cycles/8ms
- Fast page mode ,read modify write capability
- Byte wide control: 2 $\overline{CAS}$ control
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- $\overline{CAS}$ before $\overline{RAS}$ self-refresh capability (SL version)
- Pachage options:
  40-Pin 400 mil plastic SOJ (SOJ40-P-400) (Product : MSM54V16255A/SL-xx[S)
  44/40-Pin 400 mil plastic TSOP (TSOP44/40-P-400/0.8-K) (Product : MSM54V16255A/SL-xxTS-K)
  xx indicates speed rank.

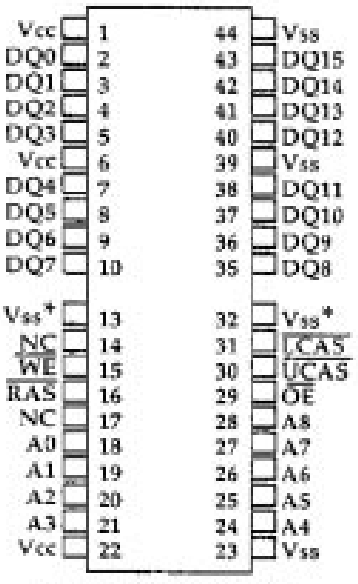
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	tRAC	tAA	tCAC	tOEA	tRC	tPC	
MSM54V16255A/SL-40	40ns	22ns	10ns	10ns	80ns	25ns	504mW
MSM54V16255A/SL-45	45ns	24ns	12ns	12ns	90ns	27ns	450mW

PIN CONFIGURATION (TOP VIEW)



40Pin 400mil SOJ



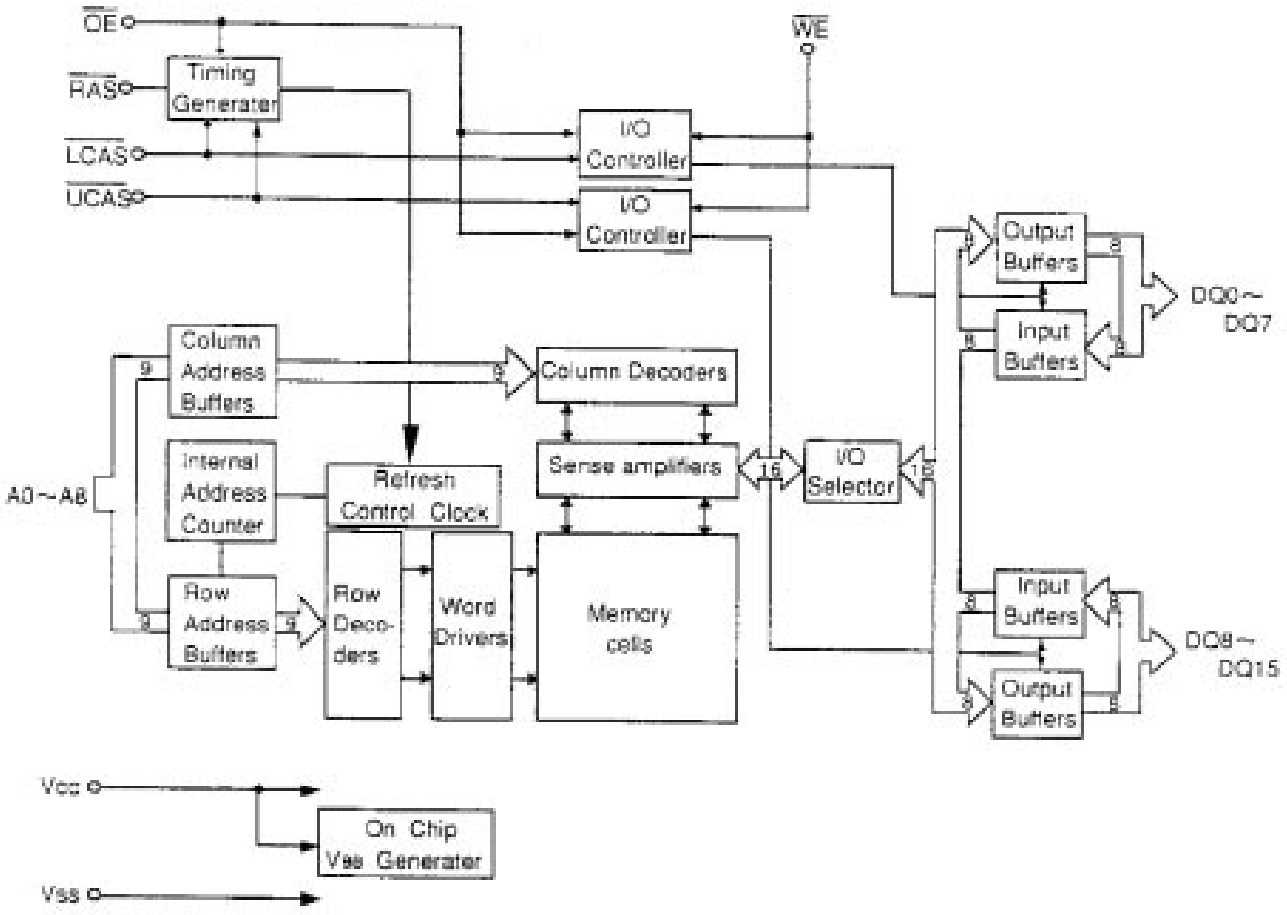
44/40Pin 400mil TSOP

Pin Names	Function
A0-A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply (3.3V)
Vss	Ground (0V)
NC	No Connection
Vss*	Ground (0V) : see Note2

Note1 :
The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must beprovideded to every Vss pin.

Note2 :
For improved signal integrity, it is recommended to connect the Vss* pins, pin 11 and 31(SOJ) or pin 13 and 32(TSOP) to GND : the pins are electrically connected to internal GND.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functinal Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresn
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25℃	-0.5~+4.6	V
Short circuit output current	Ios	Ta=25℃	50	mA
Power dissipation	Po	Ta=25℃	1	W
Operating temperature	Topr	—	0~+70	℃
Storage temperature	Tstg	—	-55~+150	℃

Recommended Operating Conditions

(Ta=0℃ to 70℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	3.0	3.3	3.6	V
	Vss	—	0	0	0	V
Input high voltage	V_{IH}	—	2.0	—	Vcc+0.3	V
Input low voltage	V_{IL}	—	-0.3	—	0.8	V

Capacitance

(Vcc=3.3V±0.3V, Ta=25℃, f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	C_{IN1}	—	—	8	pf
Input capacitance ($\overline{RAS}$,$\overline{LCAS}$,$\overline{UCAS}$,$\overline{WE}$,$\overline{OE}$)	C_{IN2}	—	—	8	pf
Input / output capacitance (DQ0~DQ15)	C_{IO}	—	—	9	pf

DC CHARACTERISTICS

(V_{CC}=3.3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	MSM54V16255A /SL-40		MSM54V18255A /SL-45		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH}= - 1.0mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL}= 2.0mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V≦V_{IN}≦Vcc	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQi Disable 0V≦V_O≦3.6V	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=Min.	—	140	—	125	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	—	3	—	3	mA	1
Average Power Supply Current ($\overline{RAS}$ only Refresh)	I_{CC3}	$\overline{RAS}$=Cycling $\overline{CAS}$=V_{IH} t_{RC}=Min.	—	140	—	125	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$=V_{IL} $\overline{CAS}$ Cycling t_{PC}=Min.	—	140	—	125	mA	1,3
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$=Cycling $\overline{CAS}$ Befor $\overline{RAS}$	—	140	—	125	mA	1,2
Average Power Supply Current (Battery Backup)	I_{CC6}	tRC = 125 μs $\overline{CAS}$ Befor $\overline{RAS}$ tRAS ≦ 1 μs	—	300	—	300	μA	1,2,4,5
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Self-refresh)	I_{CC7}	$\overline{RAS}$ ≦ 0.2V $\overline{CAS}$ ≦ 0.2V	—	200	—	200	μA	1,2,4,5

Notes : 1. Icc Max. is specified as Icc for the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = VIL.
3. Address can be changed once or less while $\overline{CAS}$ = VIH.
4. Vcc - 0.2V ≦ VIH ≦ 6.5V, -1.0V ≦ VIL ≦ 0.2V.
5. SL version.

AC CHARACTERISTICS (1/2)

(Vcc = 3.3V ± 0.3V, Ta = 0~70°C)

Parameter	Symbol	MSM54V16255A/SJ-40		MSM54V16255A/SL-45		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	80	—	90	—	ns	
Read/Write cycle time	t_{RMW}	115	—	130	—	ns	
Hyper page mode cycle time	t_{PC}	25	—	27	—	ns	
Fast page mode read/write cycle time	t_{PRMW}	55	—	60	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	40	—	45	ns	7,12,13
Access time from $\overline{CAS}$	t_{CAC}	—	10	—	12	ns	7,12
Access time from column address	t_{AA}	—	22	—	24	ns	7,13
Access time from $\overline{OE}$	t_{OEA}	—	10	—	12	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	24	—	26	ns	7,12
Output buffer turn-off delay time	t_{OFF}	3	8	3	8	ns	8
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	3	8	3	8	ns	8
Transition time	t_T	2	35	2	35	ns	
Refresh period	t_{REF}	—	8	—	8	ms	
$\overline{RAS}$ precharge time	t_{RP}	30	—	35	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	40	10,000	45	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	40	100,000	45	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	8	—	10	—	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	8	—	8	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	8	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	30	18	33	ns	12
$\overline{RAS}$ to column address delay time	t_{RAD}	13	18	13	21	ns	
Row address set-up time	t_{ASR}	0	—	0	—	ns	13
Row address hold time	t_{RAH}	8	—	8	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	5	—	6	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	30	—	30	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	22	—	24	—	ns	
Read command set-up time	t_{RCS}	0	—	0	—	ns	9
Read command hold time	t_{RCH}	0	—	0	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	9

AC CHARACTERISTICS (2/2)

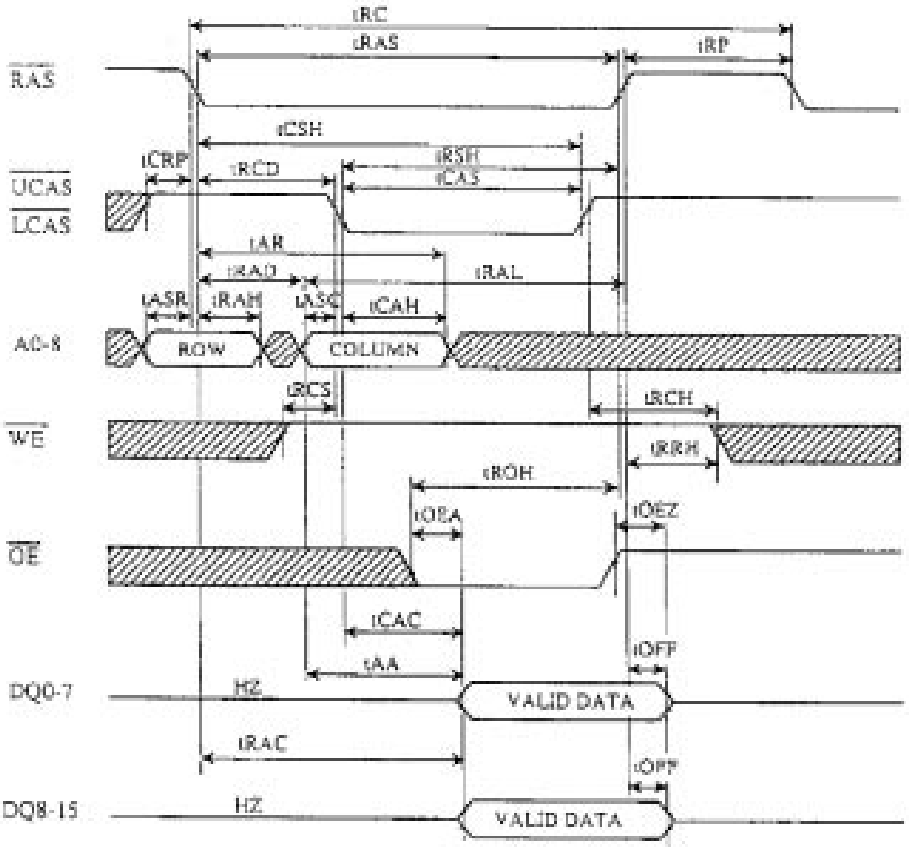
(Vcc = 3.3V ± 0.3V, Ta = 0~70°C)

Parameter	Symbol	MSM54V16255A /SL-40		MSM54V16255A /SL-45		Unit	Note
		MIN	MAX	MIN	MAX		
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	7	–	8	–	ns	
Write command pulse width	t_{WP}	7	–	8	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	30	–	30	–	ns	
$\overline{OE}$ command hold time	t_{OEH}	7	–	8	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7	–	8	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	–	12	–	ns	
Data to $\overline{CAS}$ delay time	t_{DZC}	0	–	0	–	ns	
Data to $\overline{OE}$ delay time	t_{DZO}	0	–	0	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	10
Data-in hold time	t_{DH}	6	–	7	–	ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	20	–	20	–	ns	
$\overline{OE}$ to Data-in delay time	t_{ODD}	8	–	8	–	ns	
Hi-Z command pulse width	t_{OEP}	10	–	10	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	28	–	30	–	ns	11
Column address to $\overline{WE}$ delay time	t_{AWD}	38	–	40	–	ns	11
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60	–	65	–	ns	11
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	0	–	0	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{RASS}	100	–	100	–	ns	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{RPS}	100	–	100	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{CHS}	-40	–	-40	–	ns	

Notes:

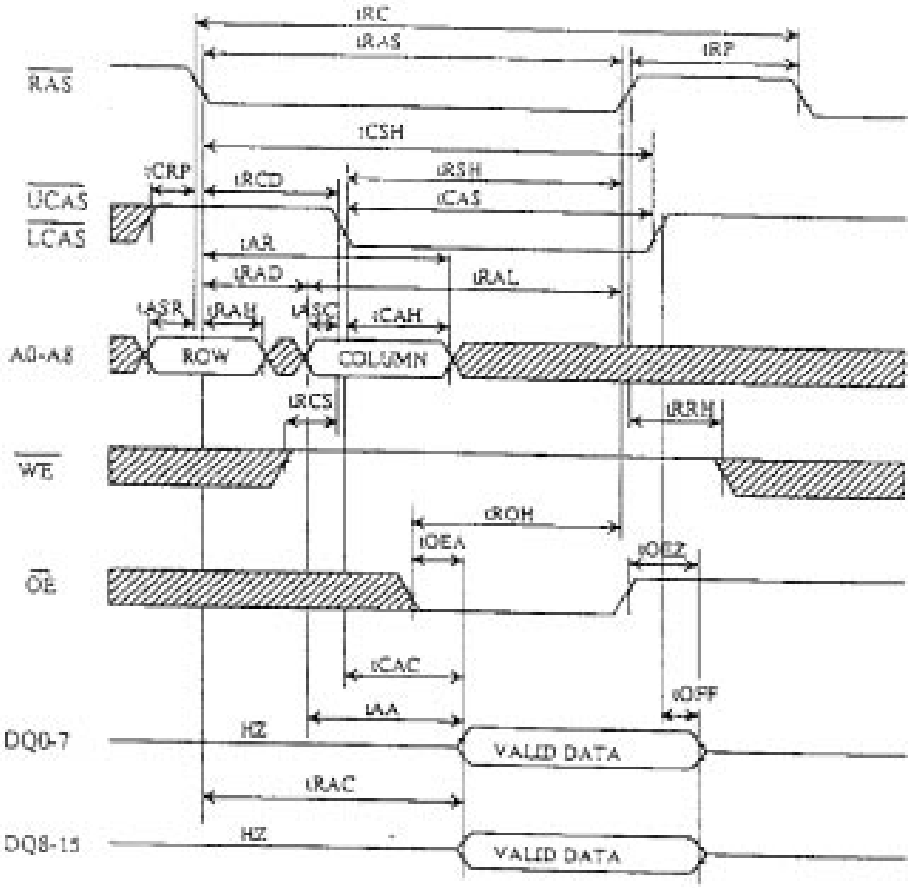
1. All voltages are referenced to V_{SS}.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles. (Example: $\overline{RAS}$-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8 $\overline{RAS}$ cycles are required.
5. The AC characteristics assume t_T=5ns.
6. V_{IH}(Min.)and V_{IL} (Max.) are reference levels for mensuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 50 pF. DOUT reference levels: V_{OH}/V_{OL}=2.0 V/1.4V. Note that V_{OL} is defined as 1.4V when Vss* pins, pin 11 and pin 30, were open. The data output measurements under V_{OH}/V_{OL}=2.0V/0.8V are guaranteed when Vss* pins, pin 11 and 30(SOJ) or pin 13 and 32(TSOP) were connected to GND.
8. t_{OEZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CPC}.
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS}$ =V_{IL}.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS}$ =V_{IH} and $\overline{RAS}$ =V_{IL}.
17. This is guaranteed by design. (t_{COH}=t_{CAC} - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

READ CYCLE ($\overline{RAS}$ output control)



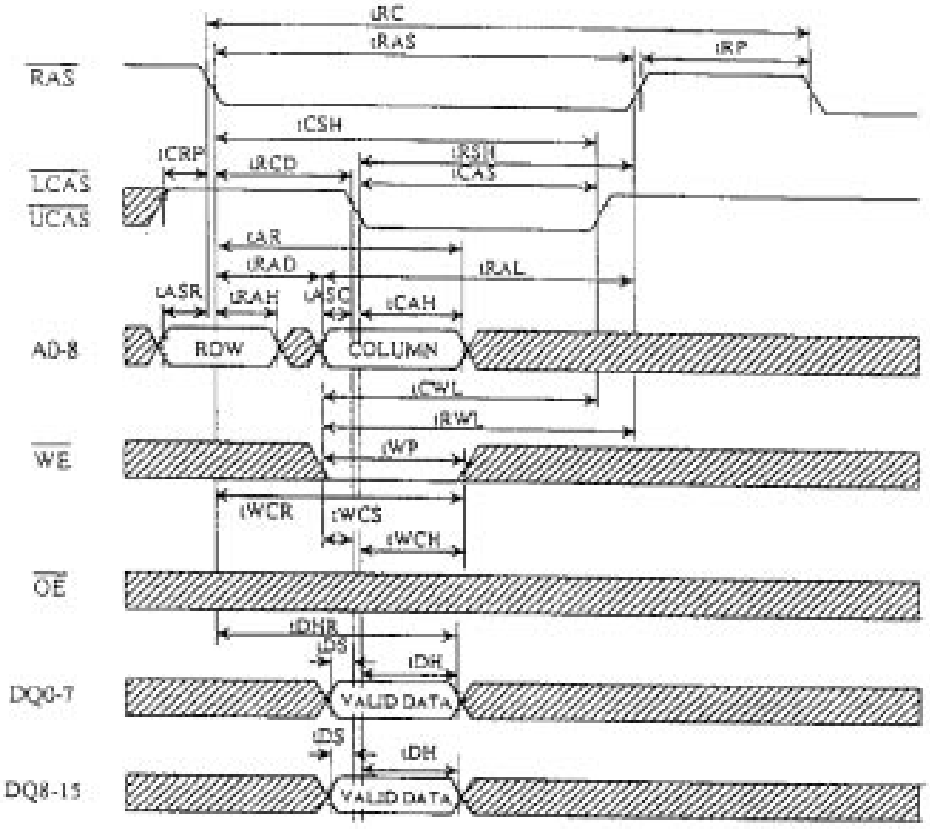
: "H" or "L"

READ CYCLE ($\overline{CAS}$ output control)



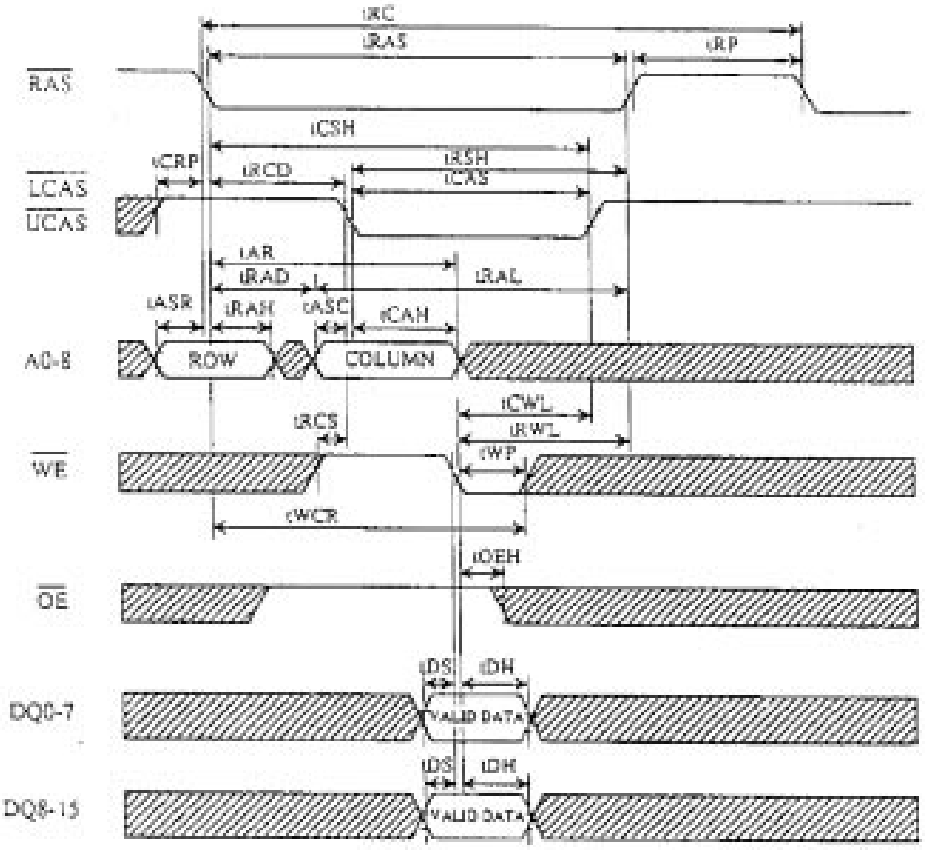
▨ : "H" or "L"

EARLY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)

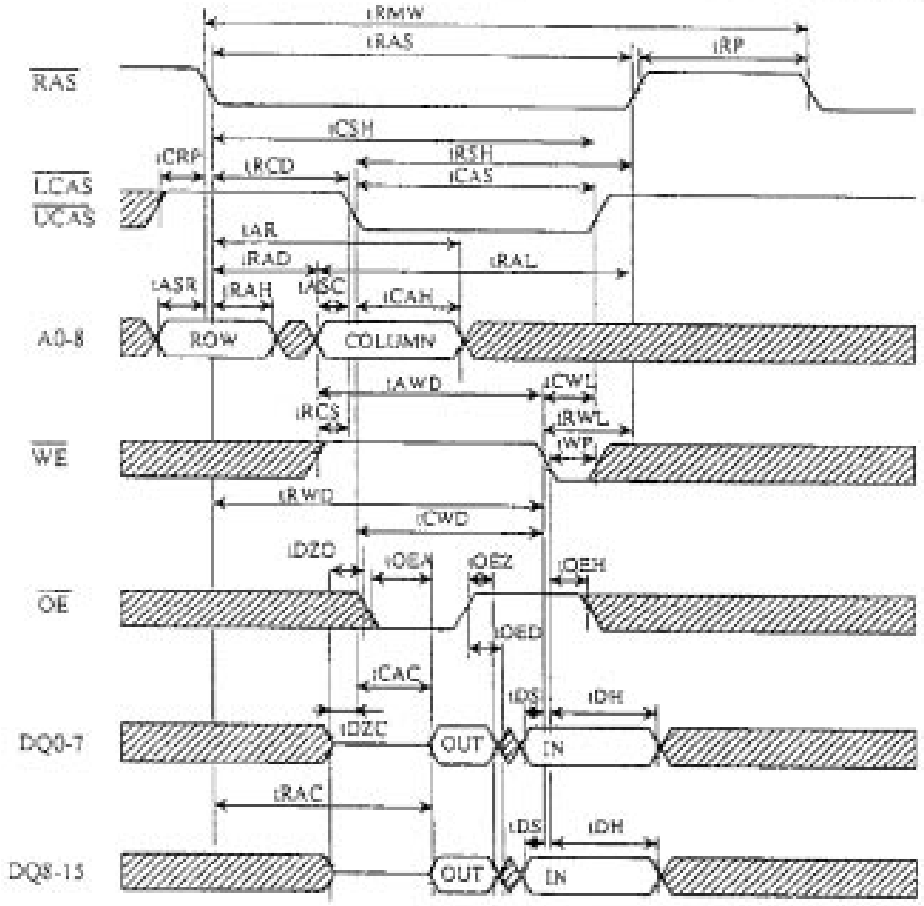


▨ : "H" or "L"

LATE WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)

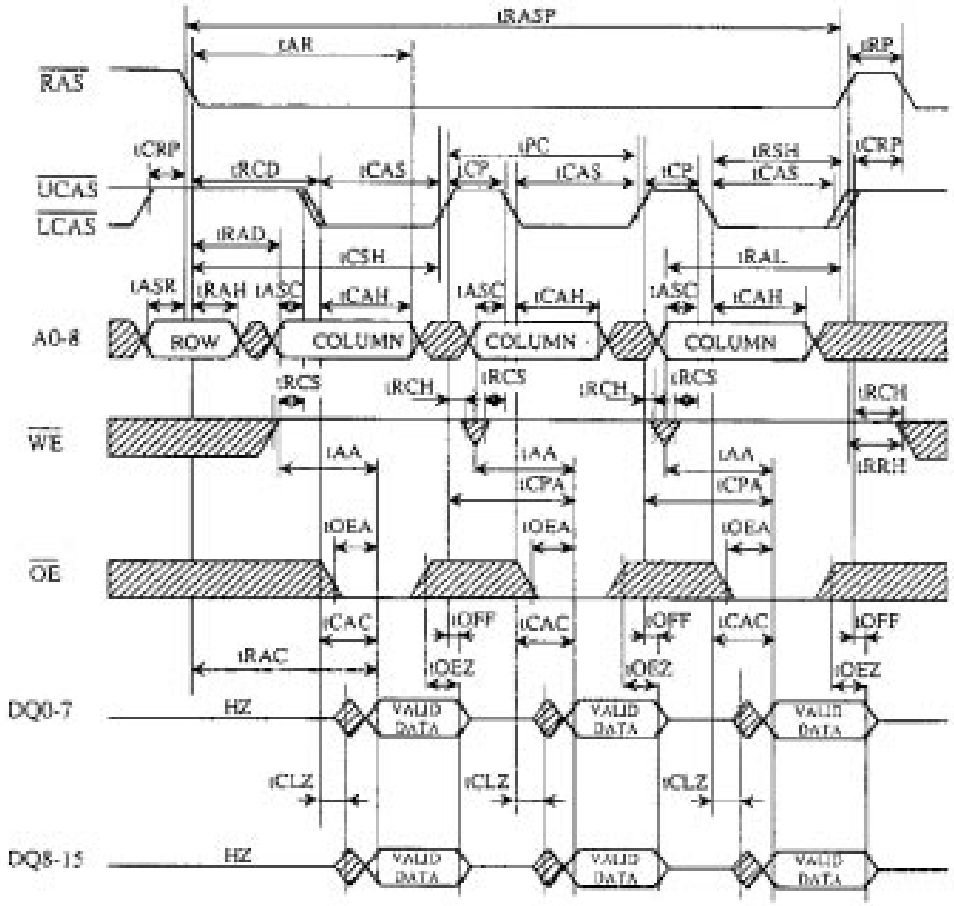


READ MODIFY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



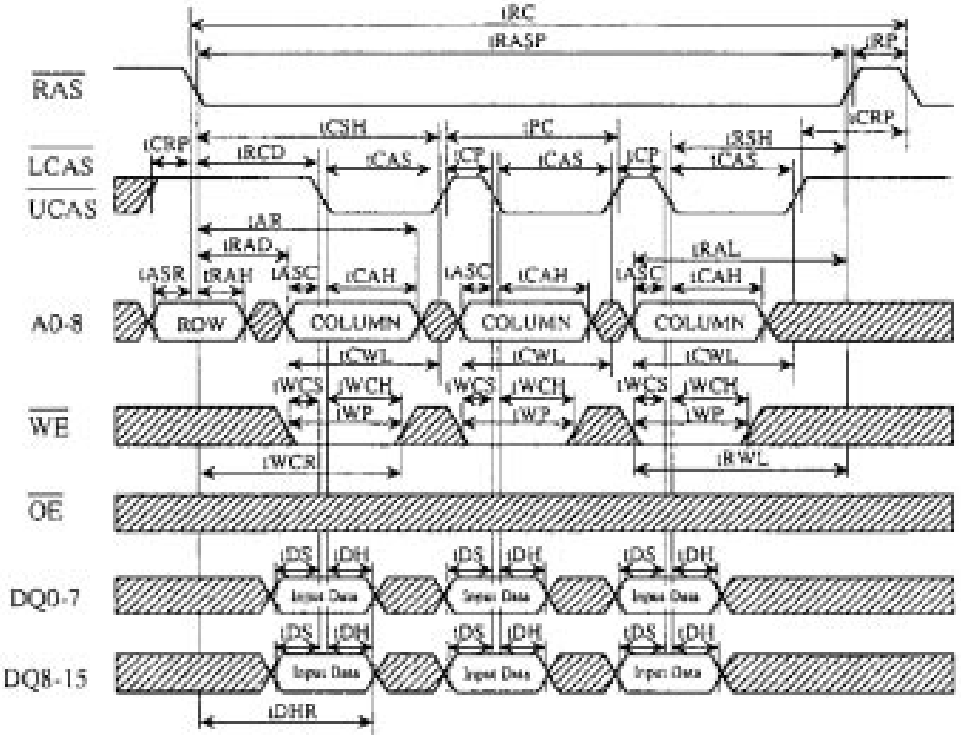
▨ : "H" or "L"

FAST PAGE MODE READ CYCLE



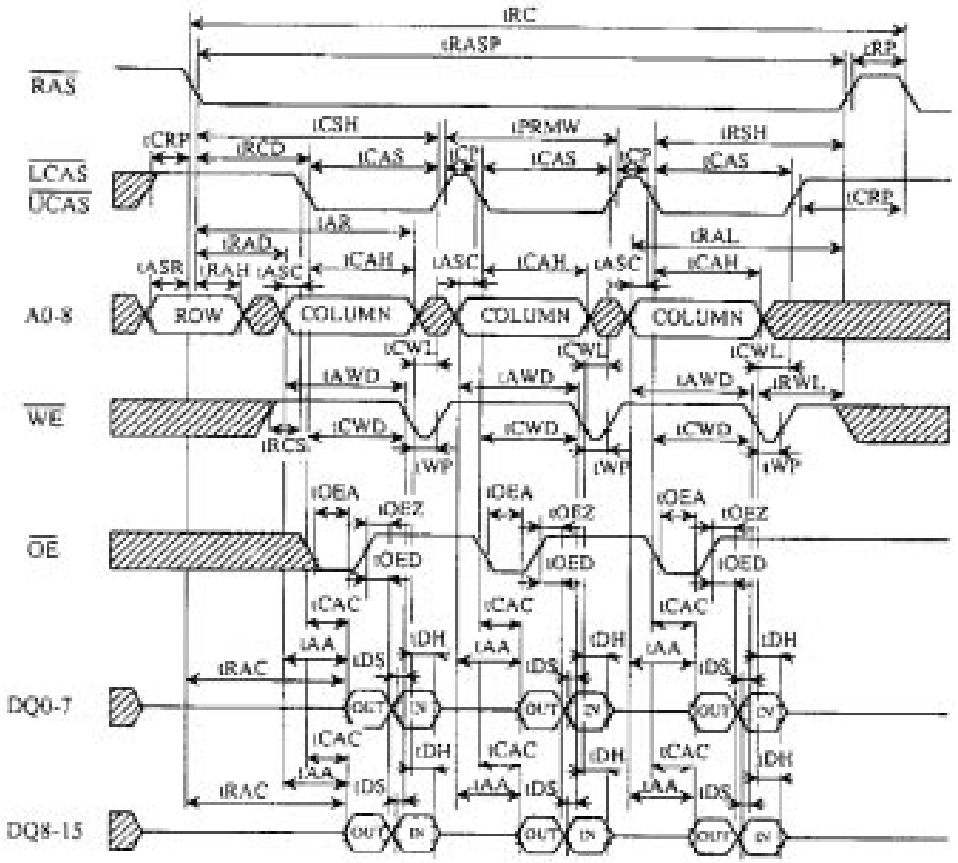
: "H" or "L"

FAST PAGE MODE EARLY WRITE CYCLE



: "H" or "L"

FAST PAGE MODE READ MODIFY WRITE CYCLE



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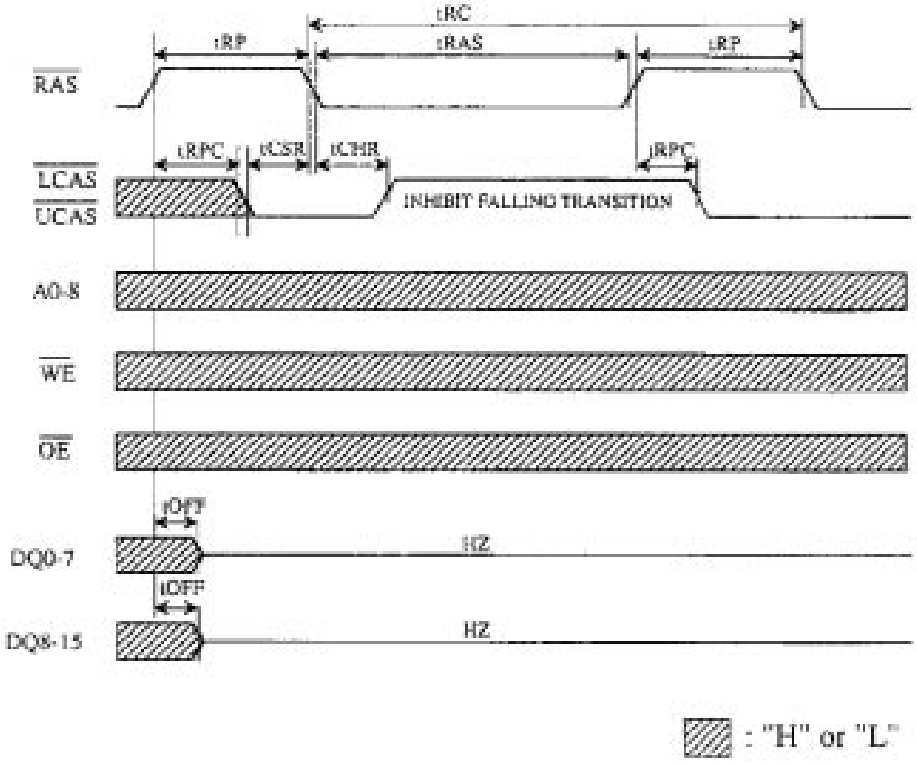
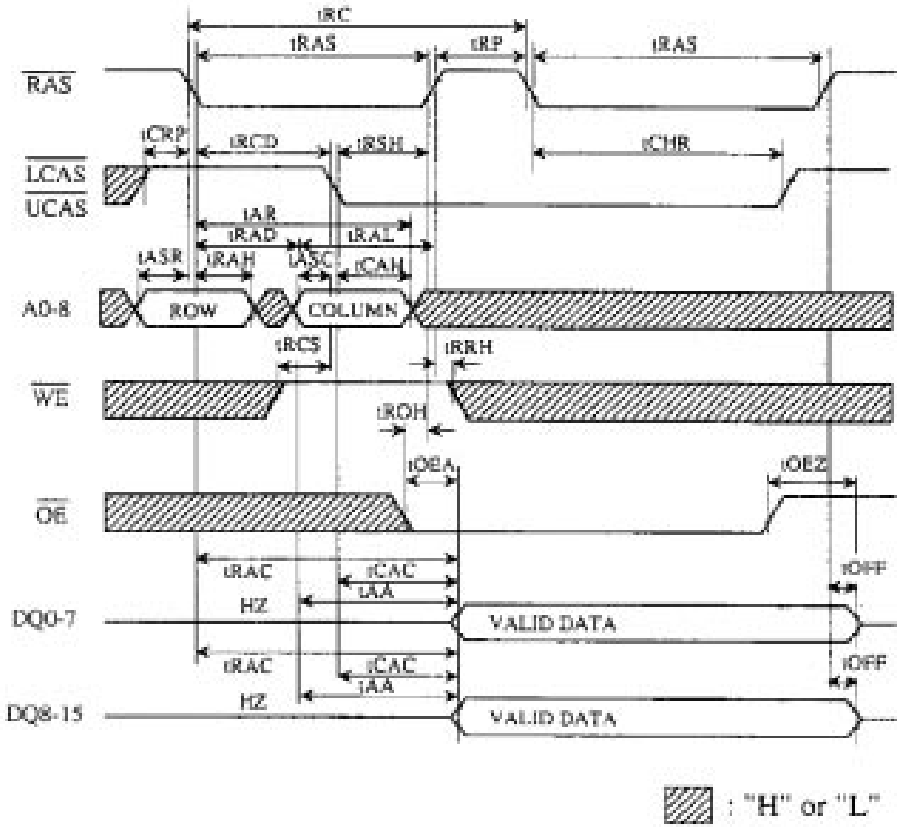
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



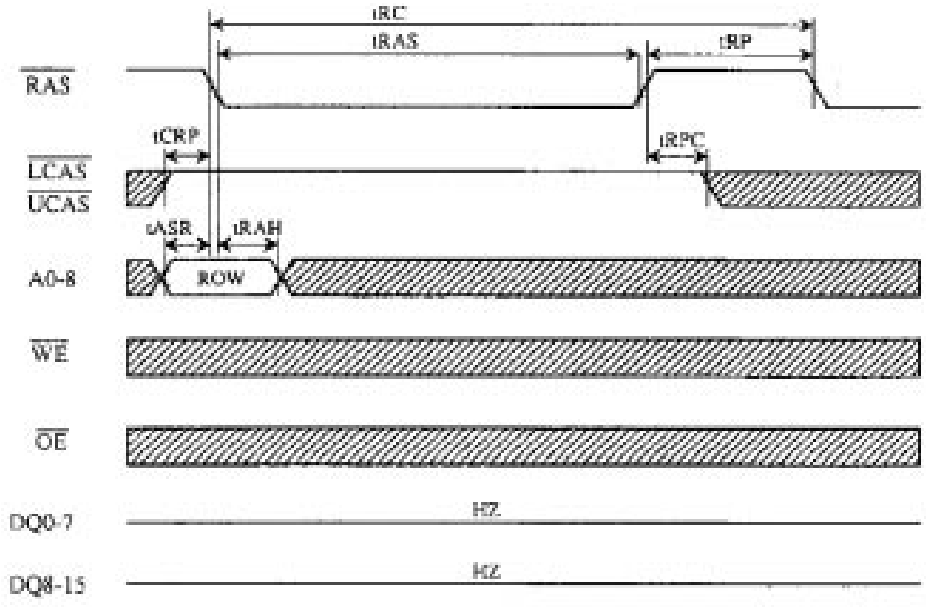
: "H" or "L"

HIDDEN REFRESH CYCLE



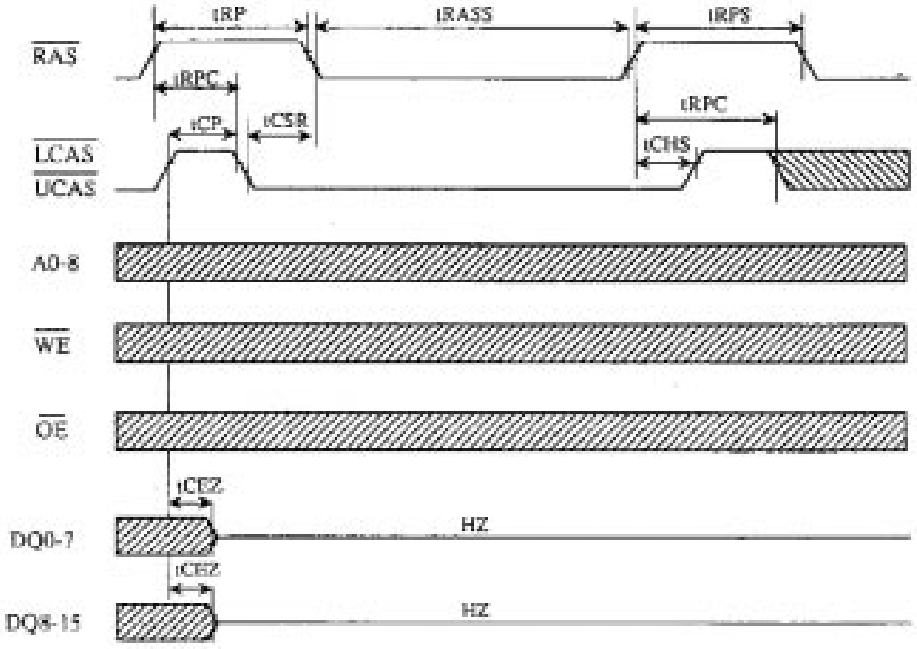
: "H" or "L"

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



▨ : "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ SELFREFRESH CYCLE



: "H" or "L"