OKI Semiconductor

This version: Jan. 1998
Previous version: Dec. 1996

MSM54V16273

262,144-Word × 16-Bit Multiport DRAM

DESCRIPTION

The MSM54V16273 is a 4-Mbit CMOS multiport DRAM composed of a 262,144-word by 16-bit dynamic RAM, and a 512-word by 16-bit SAM. Its RAM and SAM operate independently and asynchronously.

It supports three types of operations: random access to RAM port, high speed serial access to SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. In addition to the conventional multiport DRAM operating modes, the MSM54V16273 features block write, flash write functions, extended page mode on the RAM port, a split data transfer capability, and programmable stops on the SAM port. The SAM port requires no refresh operation because it uses static CMOS flip-flops.

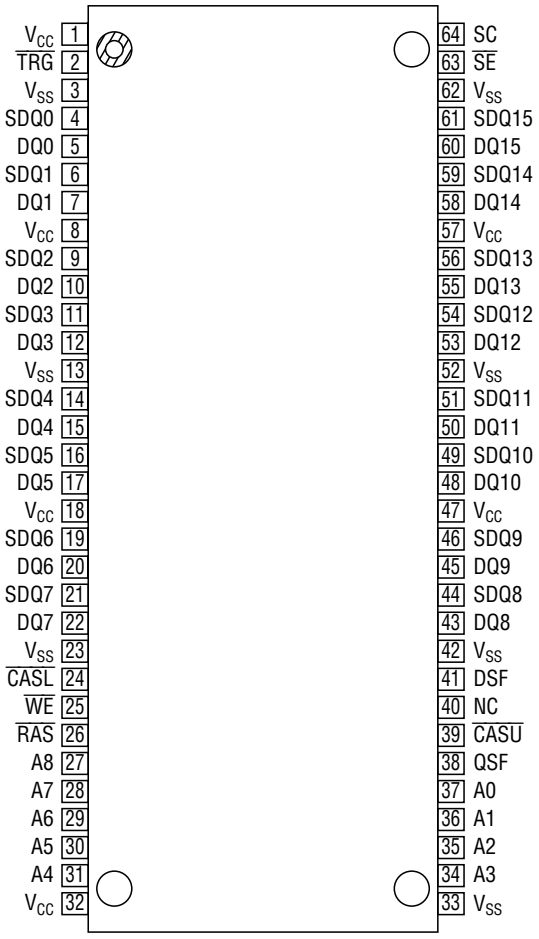
FEATURES

- Single power supply: 3.3 V ±0.3 V
- Full TTL compatibility
- Multiport organization
  RAM : 256K word × 16 bits
  SAM : 512 word × 16 bits
- Extended page mode
- Write per bit
- Persistent write per bit
- Byte read/write
- Masked flash write
- Masked block write (8 columns)
- Package options:
  64-pin 525 mil plastic SSOP (SSOP64-P-525-0.80-K) (Product : MSM54V16273-xxGS-K)
  70/64-pin 400 mil plastic TSOP (Type II)(TSOPII70/64-P-400-0.65-K) (Product : MSM54V16273-xxTS-K)
  xx indicates speed rank.
- $\overline{\text{RAS}}$ only refresh
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh
- Hidden refresh
- Serial read/write
- 512 tap location
- Programmable stops
- Bidirectional data transfer
- Split transfer
- Masked write transfer
- Refresh: 512 cycles/8 ms

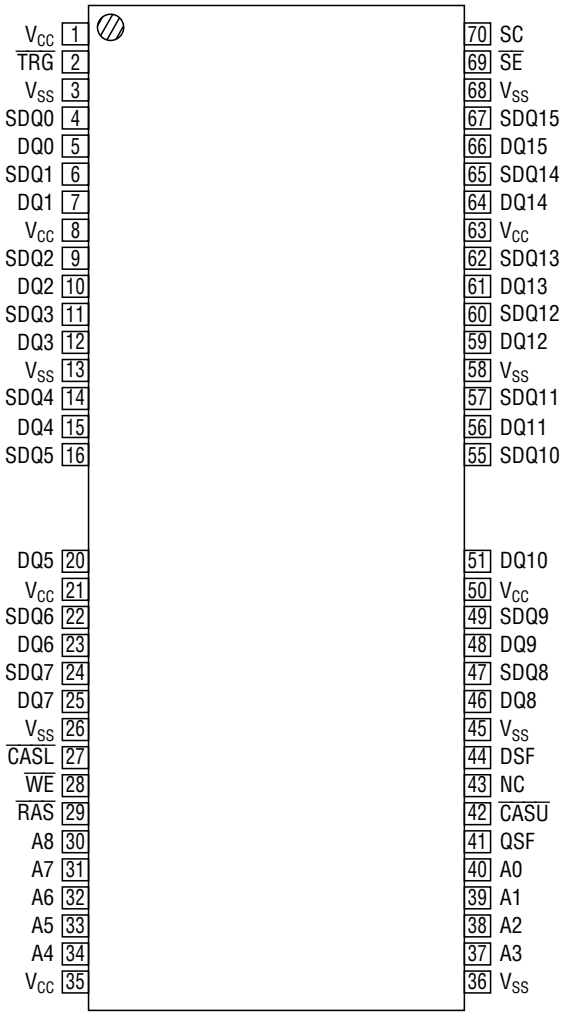
PRODUCT FAMILY

Family	Access Time		Cycle Time		Power Dissipation	
	RAM	SAM	RAM	SAM	Operating	Standby
MSM54V16273-60	60 ns	18 ns	120 ns	22 ns	160 mA	8 mA
MSM54V16273-70	70 ns	20 ns	140 ns	22 ns	150 mA	8 mA

PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic SSOP

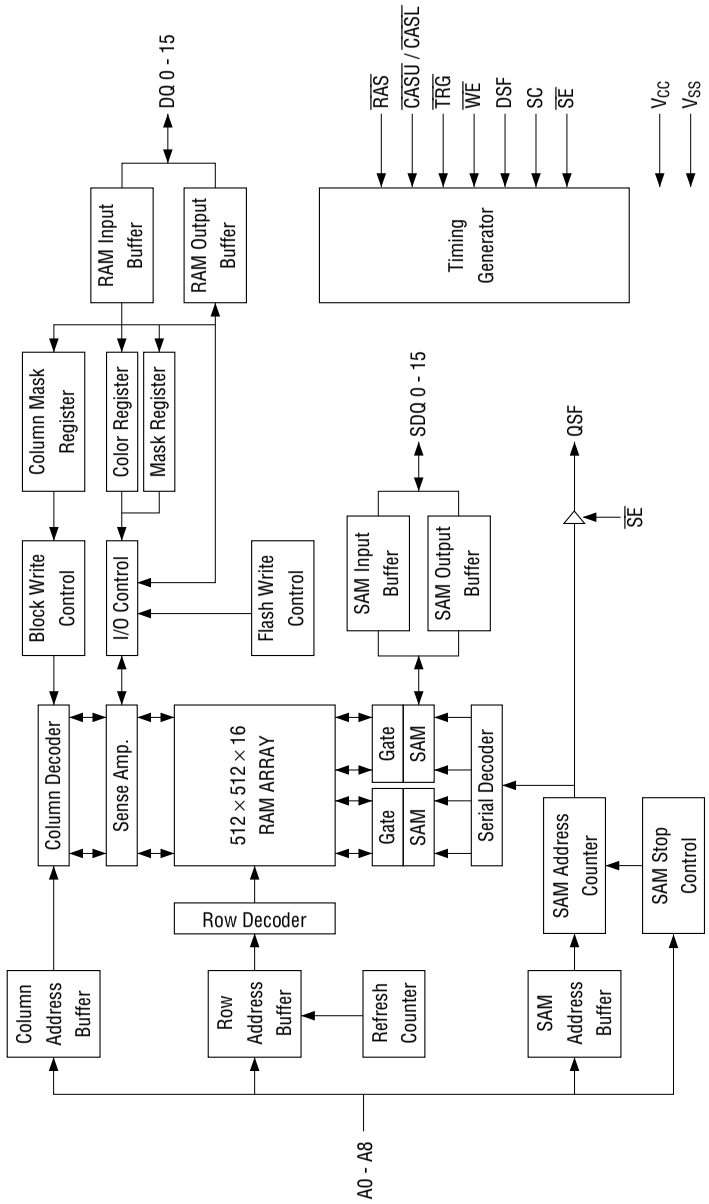


70/64-Pin Plastic TSOP (II)
(K Type)

Pin Name	Function	Pin Name	Function
A0 - A8	Address Input	SC	Serial Clock
DQ0 - DQ15	RAM Inputs/Outputs	$\overline{SE}$	SAM Port Enable
SDQ0 - SDQ15	SAM Inputs/Outputs	DSF	Special Function Input
$\overline{RAS}$	Row Address Strobe	QSF	Special Function Output
$\overline{CASL}$	Column Address Strobe Lower	V_{CC}	Power Supply (3.3 V)
$\overline{CASU}$	Column Address Strobe Upper	V_{SS}	Ground (0 V)
$\overline{WE}$	Write Enable	NC	No Connection
$\overline{TRG}$	Transfer/Output Enable		

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Note: 1)

Parameter	Symbol	Condition	Rating	Unit
Input Output Voltage	V_T	Ta = 25°C	–0.5 to 4.6	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 150	°C

Recommended Operating Conditions

(Ta = 0°C to 70°C) (Note: 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Capacitance

(V_{CC} = 3.3 V ±0.3 V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_i	—	6	pF
Input/Output Capacitance	C_{io}	—	7	pF
Output Capacitance	C_o(QSF)	—	7	pF

Note: This parameter is periodically sampled and is not 100% tested.

DC Characteristics 1

Parameter	Symbol	Condition	Min.	Max.	Unit
Output "H" Level Voltage	V_{OH}	I_{OH} = –2 mA	2.4	—	V
Output "L" Level Voltage	V_{OL}	I_{OL} = 2 mA	—	0.4	
Input Leakage Current	I_{LI}	$0 \le V_{IN} \le V_{CC}$ All other pins not under test = 0 V	–10	10	µA
Output Leakage Current	I_{LO}	$0 \le V_{OUT} \le V_{CC}$ Output Disable	–10	10	

DC Characteristics 2

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

Item (RAM)	SAM	Symbol	-60	-70	Unit	Note
			Max.	Max.		
Operating Current	Standby	I_{CC1}	120	110	mA	3, 4
($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Active	$I_{CC1}A$	160	150		17
Standby Current	Standby	I_{CC2}	8	8		
($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Active	$I_{CC2}A$	55	55		3, 4
$\overline{RAS}$ Only Refresh Current	Standby	I_{CC3}	120	110		3, 4
($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Active	$I_{CC3}A$	160	150		17
Page Mode Current	Standby	I_{CC4}	120	110		3, 4
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Active	$I_{CC4}A$	160	150		18
$\overline{CAS}$ before $\overline{RAS}$ Refresh Current	Standby	I_{CC5}	100	90		3, 4
($\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Active	$I_{CC5}A$	140	130		3, 4
Data Transfer Current	Standby	I_{CC6}	110	100		3, 4
($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Active	$I_{CC6}A$	150	140		17
Flash Write Current	Standby	I_{CC7}	110	100		3, 4
($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Active	$I_{CC7}A$	150	140		3, 4
Block Write Current	Standby	I_{CC8}	110	100		3, 4
($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Active	$I_{CC8}A$	150	140		3, 4
$\overline{CAS}$ before $\overline{RAS}$ Self-Refresh Current ($\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V)	Standby	I_{CC9}	1	1		3, 4

AC Characteristics (1/3)

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	104	—	124	—	ns	
Read Modify Write Cycle	t_{RWC}	140	—	170	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	70	—	74	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	8, 14
Access Time from Column Address	t_{AA}	—	30	—	35	ns	8, 14
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	8, 15
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	ns	8, 15
Output Buffer Turn-off Delay	t_{OFF}	0	15	0	17	ns	10
Transition Time (Rise and Fall)	t_T	2	35	2	35	ns	7
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	t_{RASP}	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	45	—	55	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10k	10	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	15	42	15	50	ns	14
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	12	30	12	35	ns	14
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	10	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	50	—	55	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	11
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	11
$\overline{CAS}$ "H" to $\overline{RAS}$ "H" Lead Time	t_{CRL}	0	—	0	—	ns	
$\overline{RAS}$ "H" to $\overline{CAS}$ "H" Lead Time	t_{RCL}	0	—	0	—	ns	
Data Output Hold after $\overline{CAS}$ Low	t_{COH}	3	—	3	—	ns	19
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	13
Write Command Hold Time	t_{WCH}	10	—	10	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	50	—	55	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	15	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	15	—	ns	

AC Characteristics (2/3)

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Data Set-up Time	t_{DS}	0	—	0	—	ns	12
Data Hold Time	t_{DH}	10	—	12	—	ns	12
Data Hold Time referenced to $\overline{RAS}$	t_{DHR}	50	—	55	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	90	—	ns	13
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	55	—	ns	13
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	40	—	ns	13
Data to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	
Data to $\overline{TRG}$ Delay Time	t_{DZO}	0	—	0	—	ns	
Access Time from $\overline{TRG}$	t_{OEA}	—	15	—	20	ns	
Output Buffer Turn-off Delay from $\overline{TRG}$	t_{OEZ}	0	15	0	15	ns	
$\overline{TRG}$ Command Hold Time	t_{OEH}	10	—	10	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{TRG}$	t_{ROH}	10	—	15	—	ns	
$\overline{CAS}$ Set-up Time for $\overline{CAS}$ before $\overline{RAS}$ Cycle	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Cycle	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{RPC}	0	—	0	—	ns	
Refresh Period	t_{REF}	—	8	—	8	ms	
$\overline{WE}$ Set-up Time	t_{WSR}	0	—	0	—	ns	
$\overline{WE}$ Hold Time	t_{RWH}	10	—	10	—	ns	
DSF Set-up Time referenced to $\overline{RAS}$	t_{FSR}	0	—	0	—	ns	
DSF Hold Time referenced to $\overline{RAS}$ (1)	t_{RFH}	10	—	10	—	ns	
DSF Hold Time referenced to $\overline{RAS}$ (2)	t_{FHR}	50	—	55	—	ns	
DSF Set-up Time referenced to $\overline{CAS}$	t_{FSC}	0	—	0	—	ns	
DSF Hold Time referenced to $\overline{CAS}$	t_{CFH}	10	—	10	—	ns	
Write Per Bit Mask Data Set-up Time	t_{MS}	0	—	0	—	ns	
Write Per Bit Mask Data Hold Time	t_{MH}	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{RASS}	100	—	100	—	μs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{RPS}	120	—	140	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{CHS}	0	—	0	—	ns	
$\overline{TRG}$ High Set-up Time	t_{THS}	0	—	0	—	ns	
$\overline{TRG}$ High Hold Time	t_{THH}	10	—	10	—	ns	
$\overline{TRG}$ Low Set-up Time	t_{TLS}	0	—	0	—	ns	
$\overline{TRG}$ Low Hold Time	t_{TLH}	10	10k	10	10k	ns	
$\overline{TRG}$ Low Hold Time referenced to $\overline{RAS}$	t_{RTH}	50	10k	60	10k	ns	
$\overline{TRG}$ Low Hold Time referenced to Column Address	t_{ATH}	20	—	25	—	ns	
$\overline{TRG}$ Low Hold Time referenced to $\overline{CAS}$	t_{CTH}	15	—	20	—	ns	

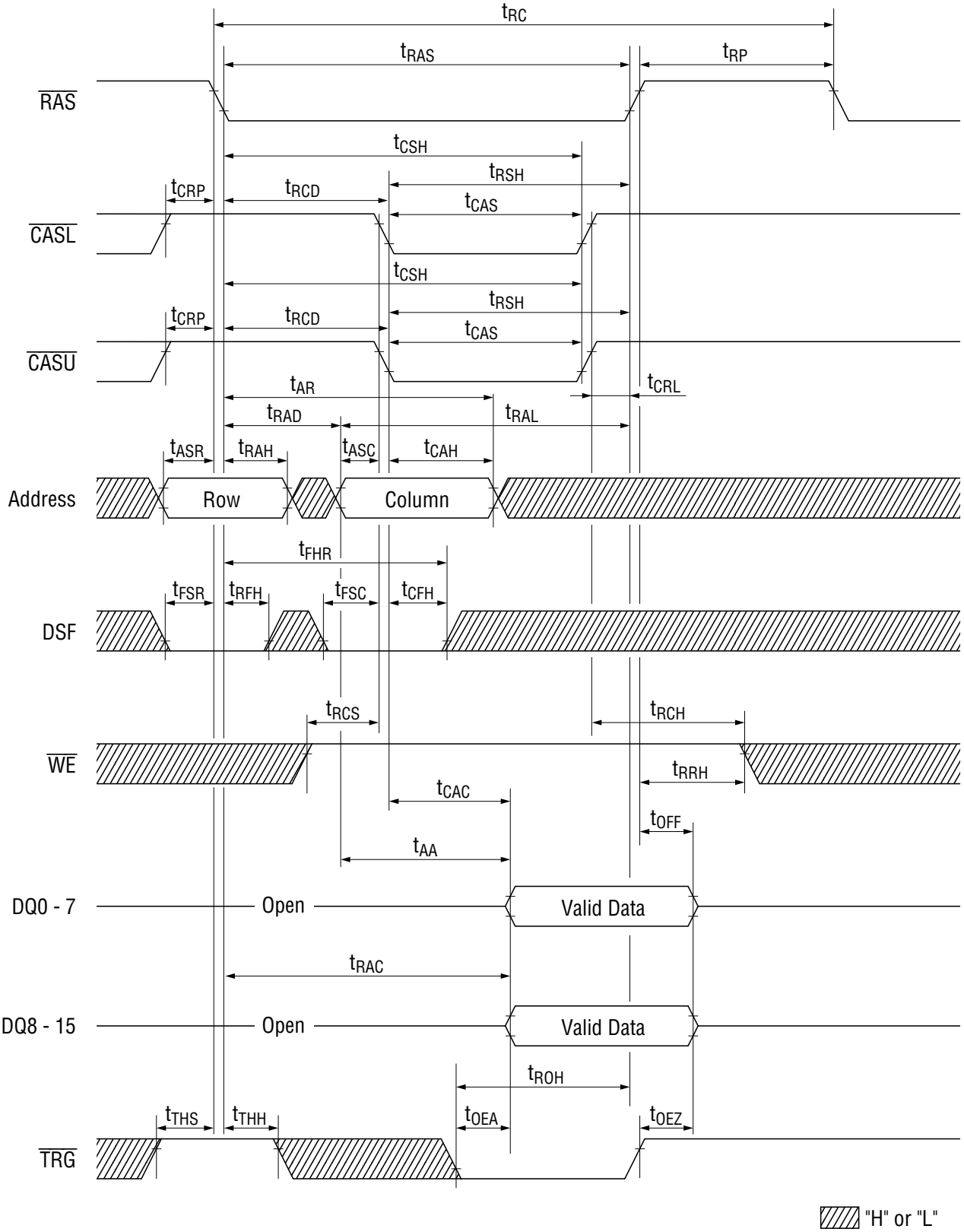
AC Characteristics (3/3)

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
$\overline{TRG}$ to $\overline{RAS}$ Precharge Time	t_{TRP}	40	—	50	—	ns	
$\overline{TRG}$ Precharge Time	t_{TP}	20	—	20	—	ns	
$\overline{RAS}$ to First SC Delay Time (Read Transfer)	t_{RSD}	60	—	70	—	ns	
Column Address to First SC Delay Time	t_{ASD}	30	—	35	—	ns	
$\overline{CAS}$ to First SC Delay Time (Read Transfer)	t_{CSD}	20	—	20	—	ns	
Last SC to $\overline{TRG}$ Lead Time	t_{TSL}	5	—	5	—	ns	
$\overline{TRG}$ to First SC Delay Time (Read Transfer)	t_{TSD}	10	—	10	—	ns	
Last SC to $\overline{RAS}$ Set-up Time (Serial Input)	t_{SRS}	20	—	25	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SDZ}	10	30	10	40	ns	10
SC Cycle Time	t_{SCC}	18	—	20	—	ns	
SC Pulse Width (SC High Time)	t_{SC}	5	—	5	—	ns	
SC Precharge Time (SC Low Time)	t_{SCP}	5	—	5	—	ns	
Access Time from SC	t_{SCA}	—	15	—	17	ns	9
Serial Output Hold Time from SC	t_{SOH}	3	—	5	—	ns	19
Access Time from $\overline{SE}$	t_{SEA}	—	15	—	17	ns	9
$\overline{SE}$ Pulse Width	t_{SE}	10	—	10	—	ns	
$\overline{SE}$ Precharge Time	t_{SEP}	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	0	15	0	15	ns	10
Split Transfer Set-up Time	t_{STS}	20	—	25	—	ns	
Split Transfer Hold Time	t_{STH}	20	—	25	—	ns	
SC-QSF Delay Time	t_{SQD}	—	20	—	25	ns	
$\overline{TRG}$-QSF Delay Time	t_{TQD}	—	20	—	25	ns	
$\overline{CAS}$-QSF Delay Time	t_{CQD}	—	30	—	35	ns	
$\overline{RAS}$-QSF Delay Time	t_{RQD}	—	70	—	75	ns	
$\overline{RAS}$ to Serial Input Delay Time	t_{SDD}	30	—	40	—	ns	
Serial Input Set-up Time	t_{SDS}	0	—	0	—	ns	
Serial Input Hold Time	t_{SDH}	10	—	10	—	ns	
Serial Input to $\overline{SE}$ Delay Time	t_{SZE}	0	—	0	—	ns	
Serial Input to First SC Delay Time	t_{SZS}	0	—	0	—	ns	
Serial Write Enable Set-up Time	t_{SWS}	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	10	—	10	—	ns	
Serial Write Disable Set-up Time	t_{SWIS}	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	10	—	10	—	ns	

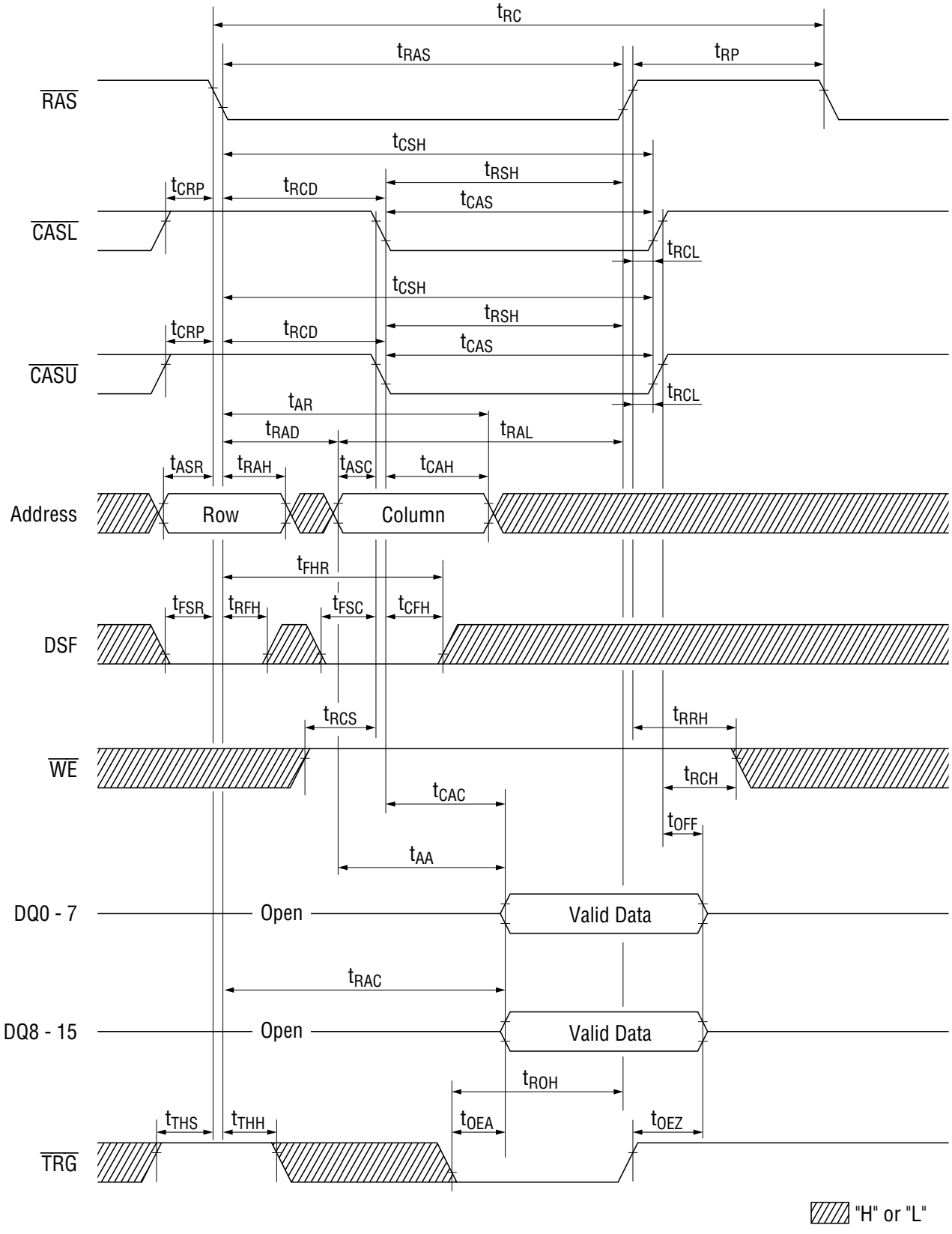
Notes:
1. Exposure beyond the "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on the cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 µs is required after power up followed by any 8 $\overline{RAS}$ cycles ($\overline{TRG}$ = "high") and any 8 SC cycles before proper device operation is achieved. In the case of using an internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 50 pF. DOUT reference levels : V_{OH}/V_{OL} = 2.0 V/0.8 V.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. DOUT reference levels : V_{OH}/V_{OL} = 2.0 V/0.8 V.
10. t_{OFF} (Max.), t_{OEZ} (Max.), t_{SDZ} (Max.) and t_{SEZ} (Max.) define the time at which the outputs achieve the open circuit condition, and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles, and to $\overline{WE}$ leading edge in $\overline{TRG}$ controlled write cycles and read modify write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read modify write cycle, and the data out will contain data read from the selected cell; If neither of the above sets of conditions are satisfied, the condition of the data out is indeterminate.
14. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
16. Input levels at the AC testing are 3.0 V/0 V.
17. Address (A0 - A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
18. Address (A0 - A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
19. This is guaranteed by design. ($t_{SOH}/t_{COH} = t_{SCA}/t_{CAC}$ - output transition time) This parameter is not 100% tested.

TIMING WAVEFORM

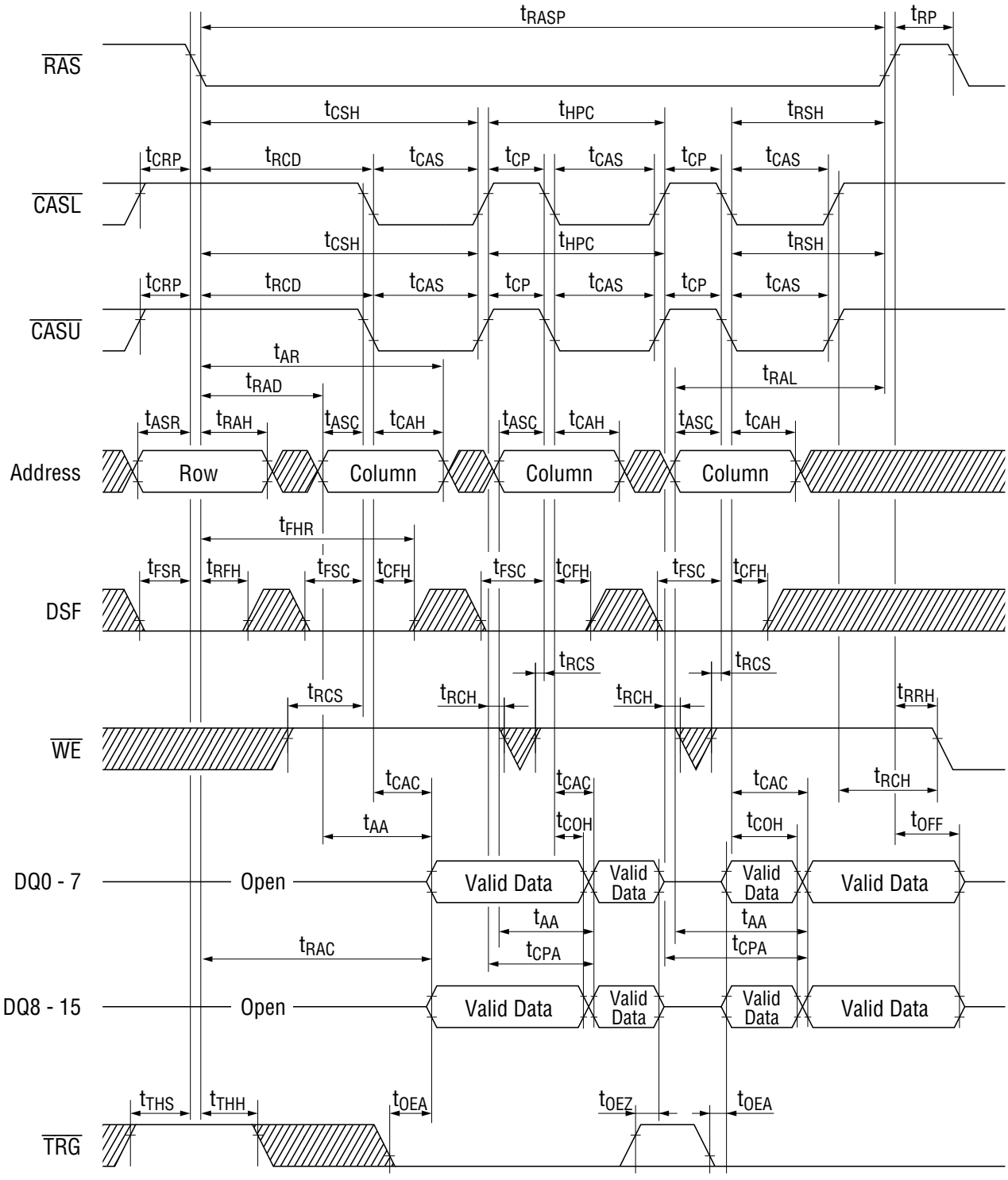
Read Cycle (Outputs Controlled by $\overline{RAS}$)



Read Cycle (Outputs Controlled by $\overline{CAS}$)



Extended Page Mode Read Cycle



Write Cycle Function Table

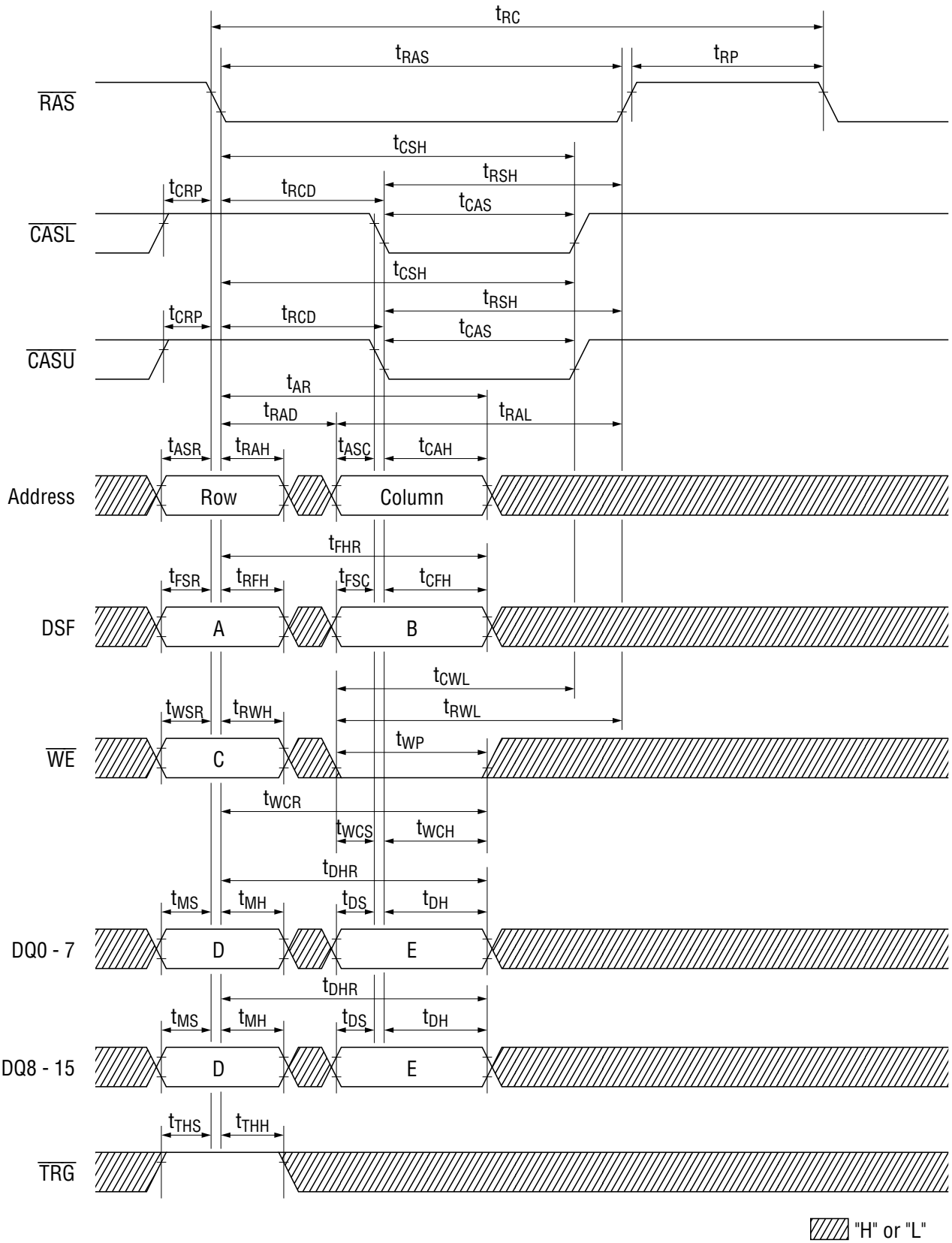
Code	$\overline{RAS}$ Falling Edge			$\overline{CAS}$ Falling Edge		Function
	A	C	D	B	E	
	DSF	$\overline{WE}$	DQ	DSF	DQ	
RWM	0	0	Write Mask	0	Valid Data	Masked Write (New/Old)
BWM	0	0	Write Mask	1	Column Mask	Masked Block Write (New/Old)
FWM	1	0	Write Mask	X	X	Masked Flash Write (New/Old)
RW	0	1	X	0	Valid Data	Normal Write
BW	0	1	X	1	Column Mask	Block Write
LMR	1	1	X	0	Write Mask Data	Load Mask Register
LCR	1	1	X	1	Color Data	Load Color Register

WRITE MASK DATA: "Low" = Mask, "High" = No Mask

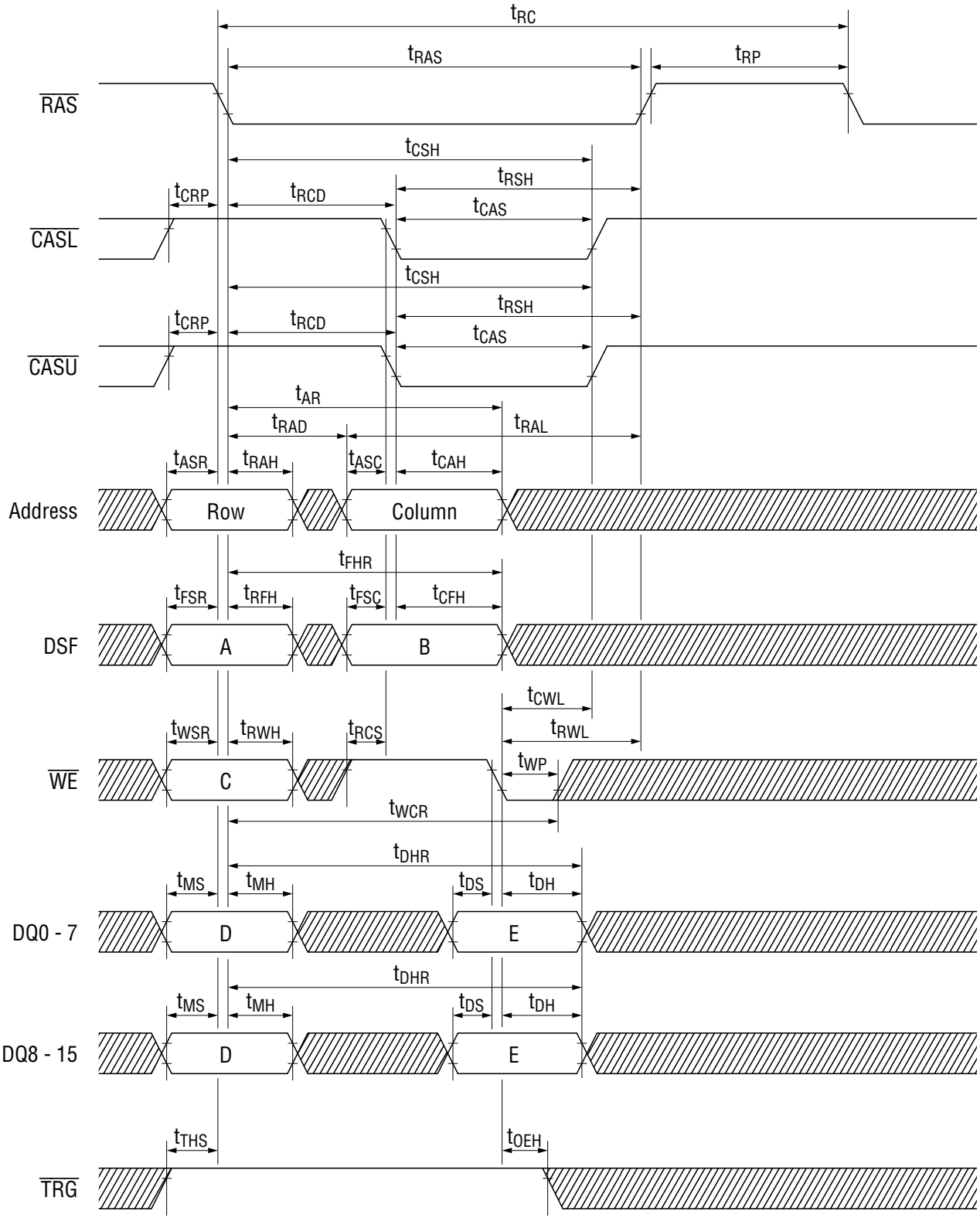
Column Mask Data

	DQ0 - 15	Column Mask Data	
Lower Byte	DQ0	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low : Mask High : No Mask
	DQ1	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ2	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ3	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ4	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ5	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ6	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ7	Column 7 (A0 = 1, A1 = 1, A2 = 1)	
Upper Byte	DQ8	Column 0 (A0 = 0, A1 = 0, A2 = 0)	Low : Mask High : No Mask
	DQ9	Column 1 (A0 = 1, A1 = 0, A2 = 0)	
	DQ10	Column 2 (A0 = 0, A1 = 1, A2 = 0)	
	DQ11	Column 3 (A0 = 1, A1 = 1, A2 = 0)	
	DQ12	Column 4 (A0 = 0, A1 = 0, A2 = 1)	
	DQ13	Column 5 (A0 = 1, A1 = 0, A2 = 1)	
	DQ14	Column 6 (A0 = 0, A1 = 1, A2 = 1)	
	DQ15	Column 7 (A0 = 1, A1 = 1, A2 = 1)	

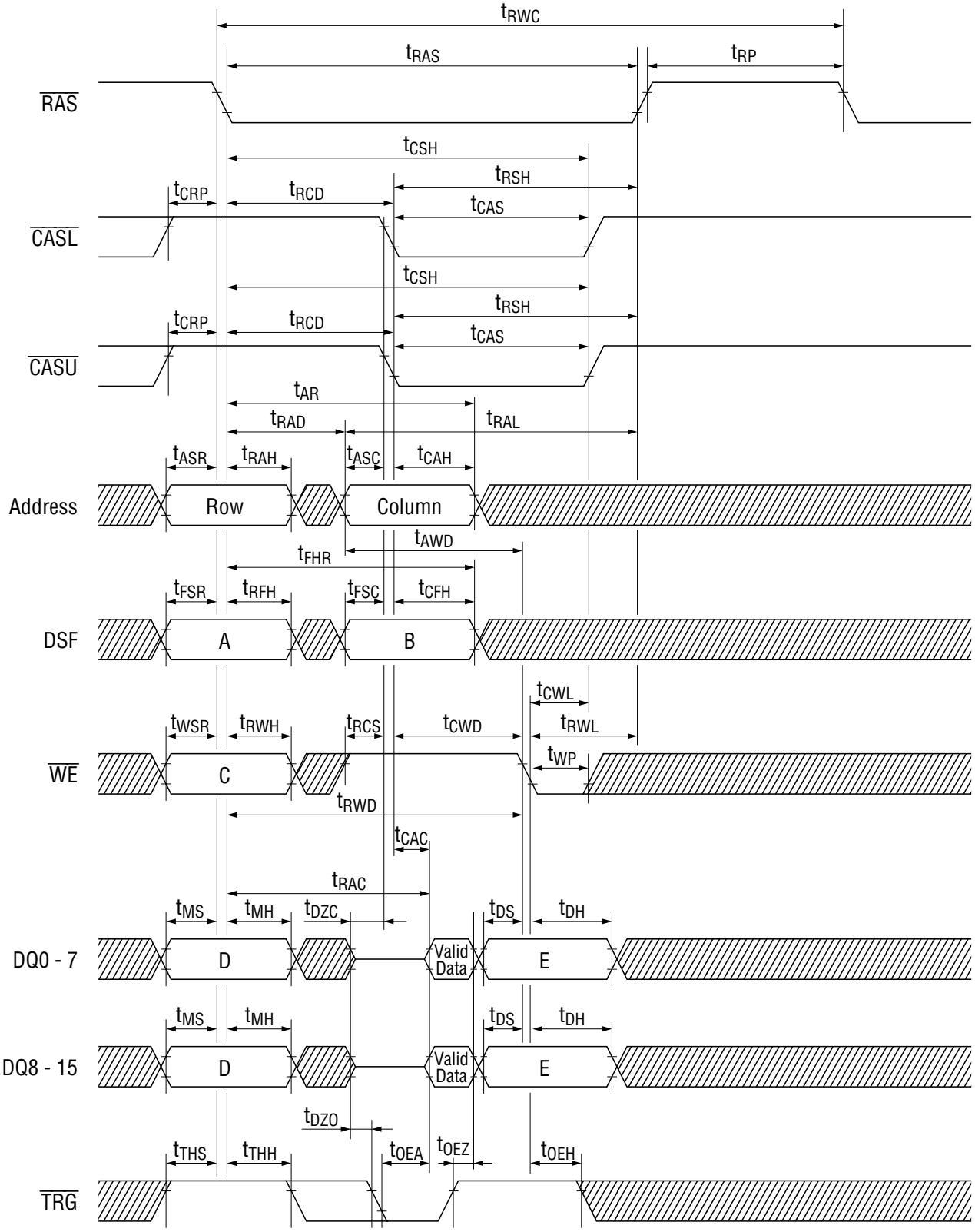
Early Write Cycle



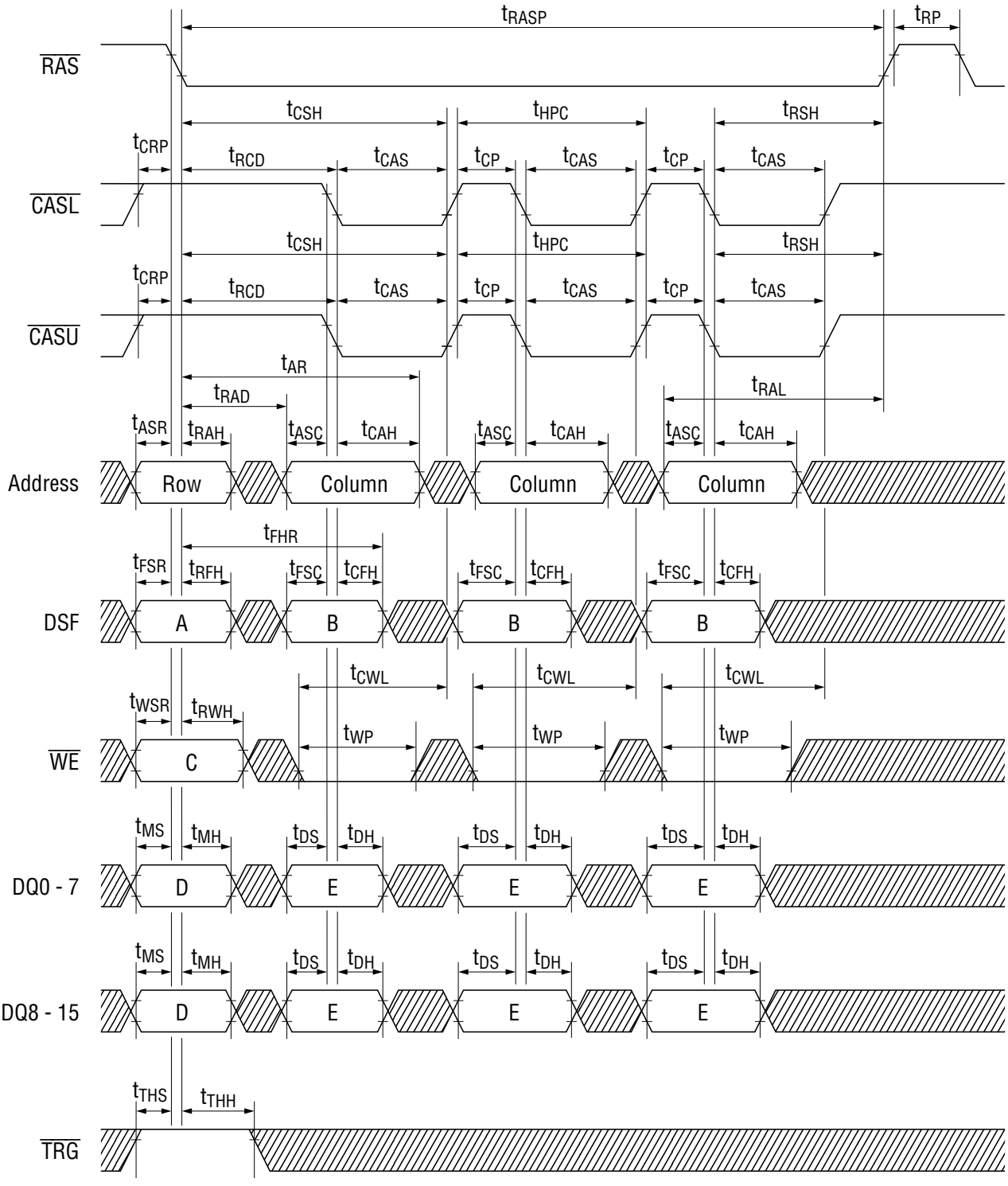
Late Write Cycle



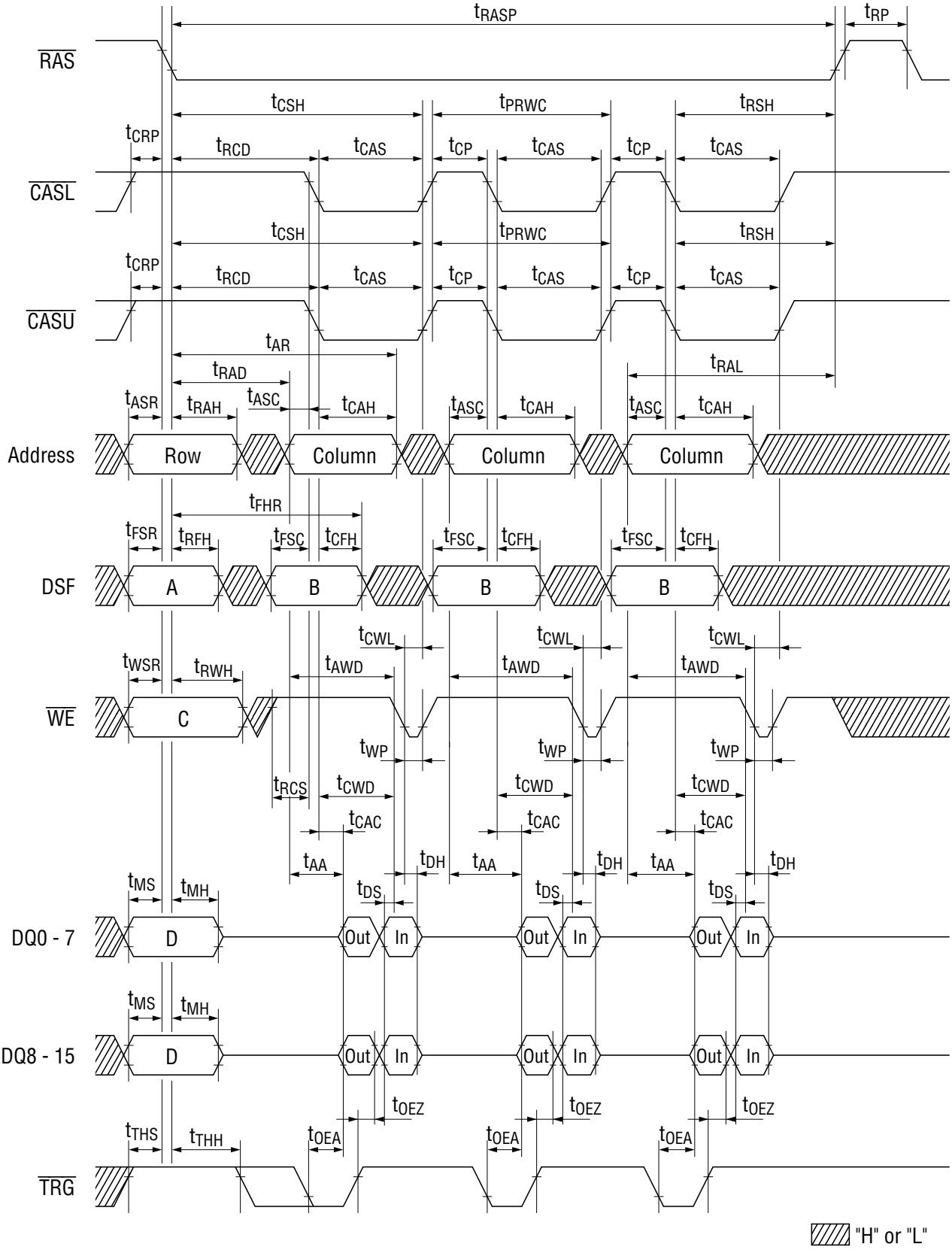
Read Modify Write Cycle



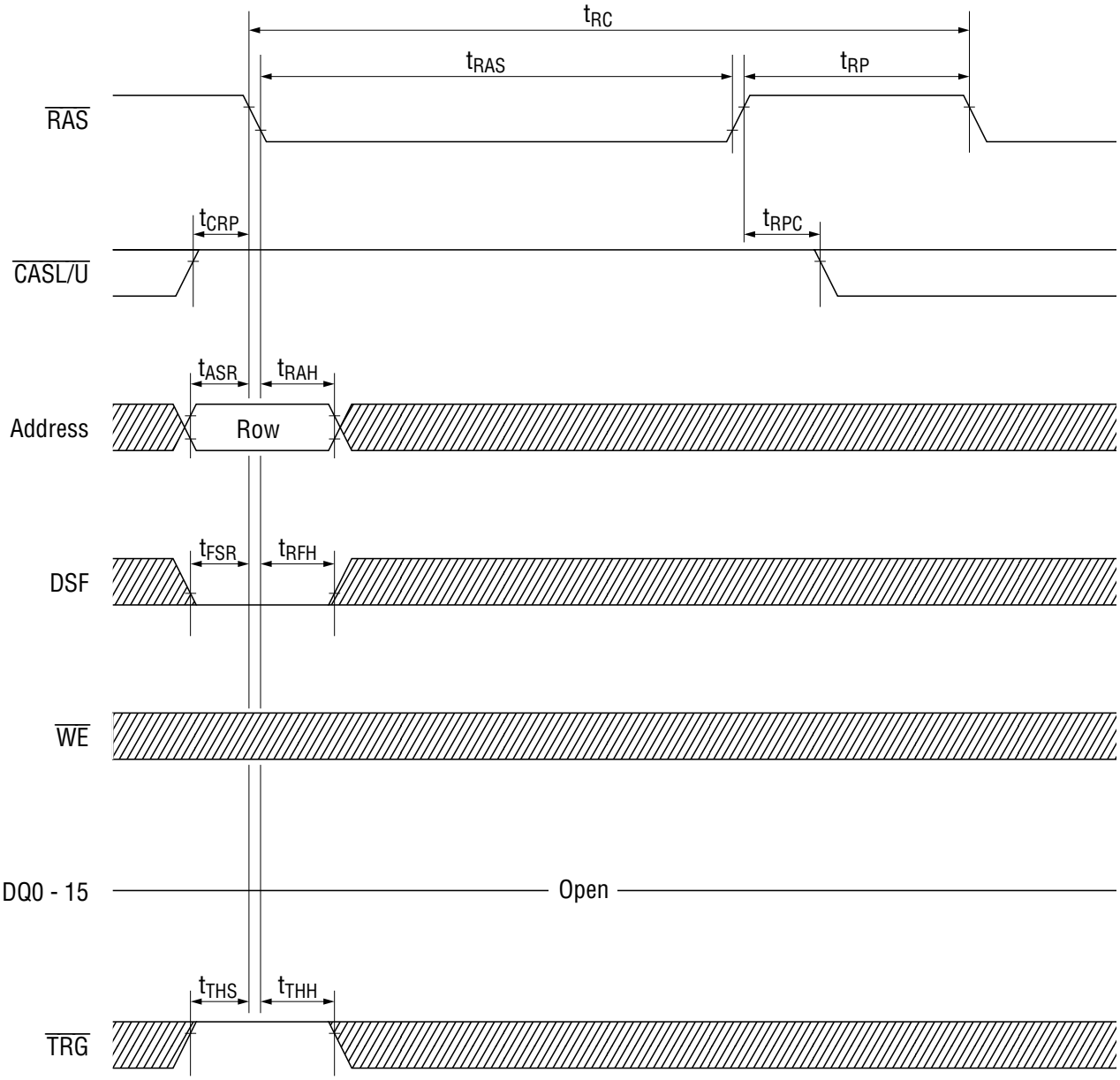
Fast Page Mode Early Write Cycle



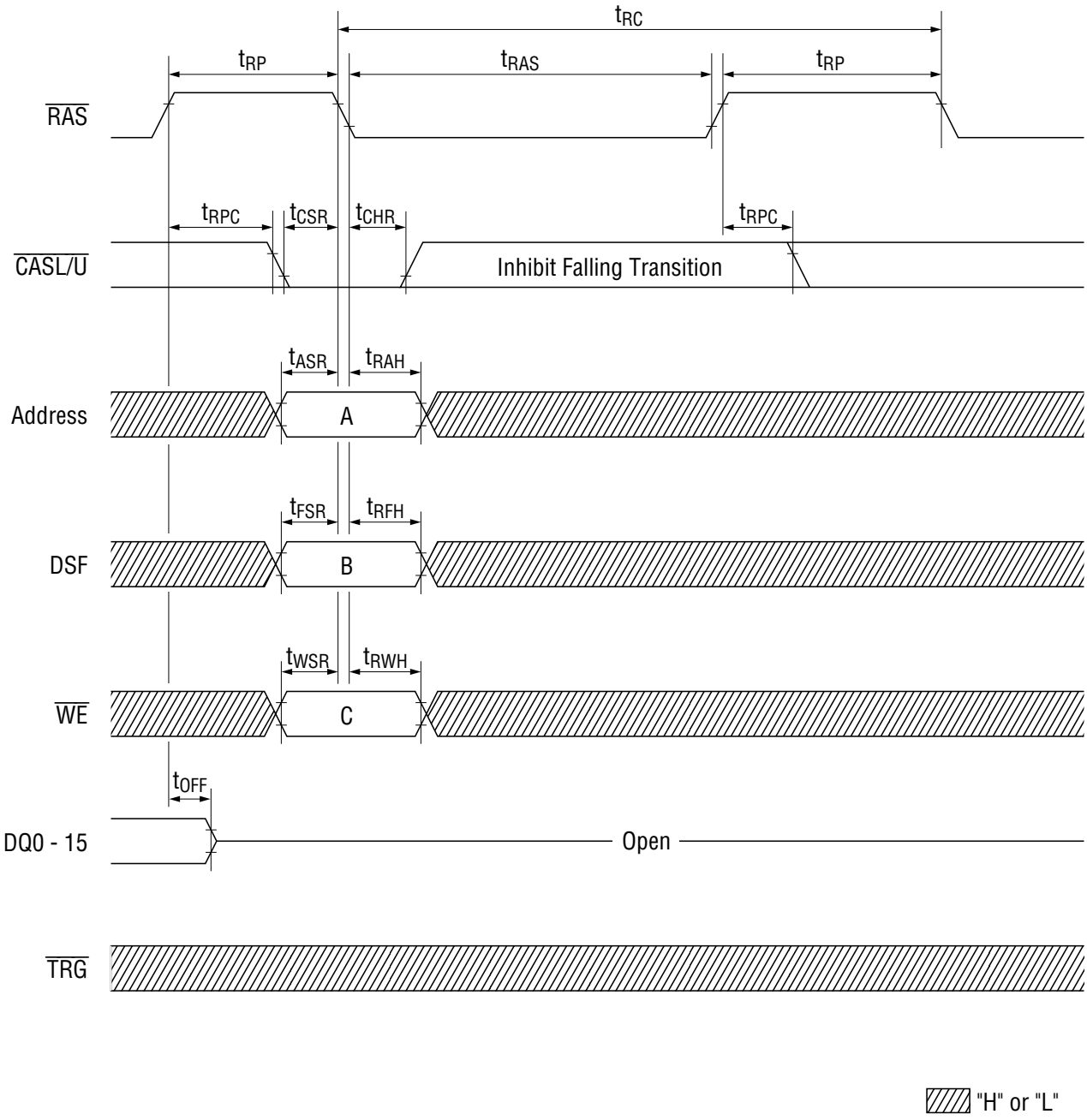
Fast Page Mode Read Modify Write Cycle



$\overline{\text{RAS}}$ Only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

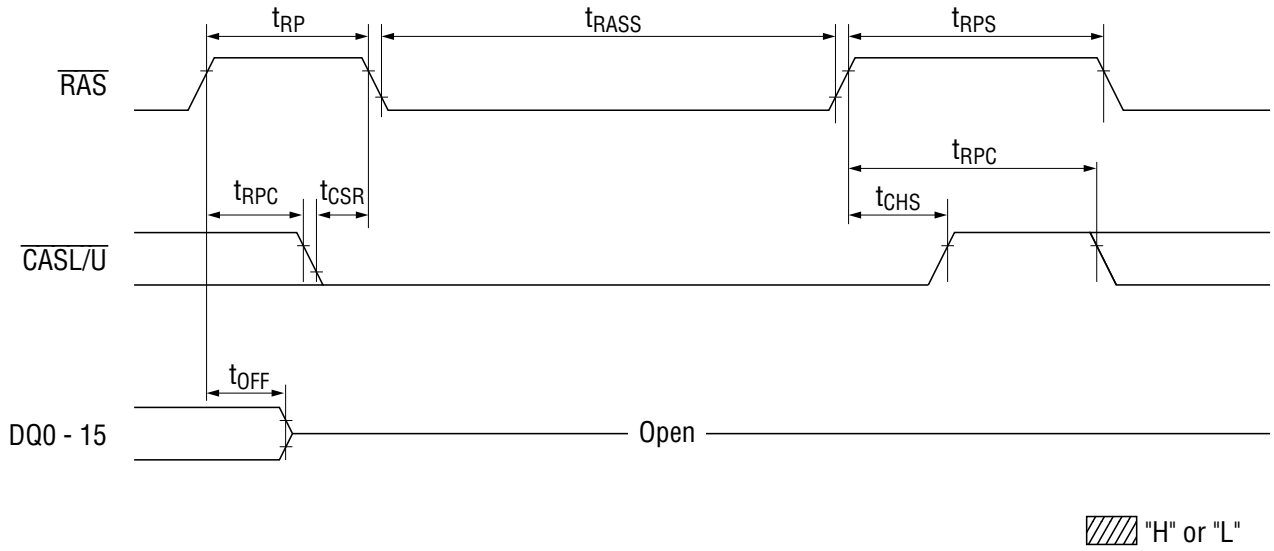


Note: The type of CBR operations are determined by the logic states of "A", "B" and "C".

CBR Cycle Function Table

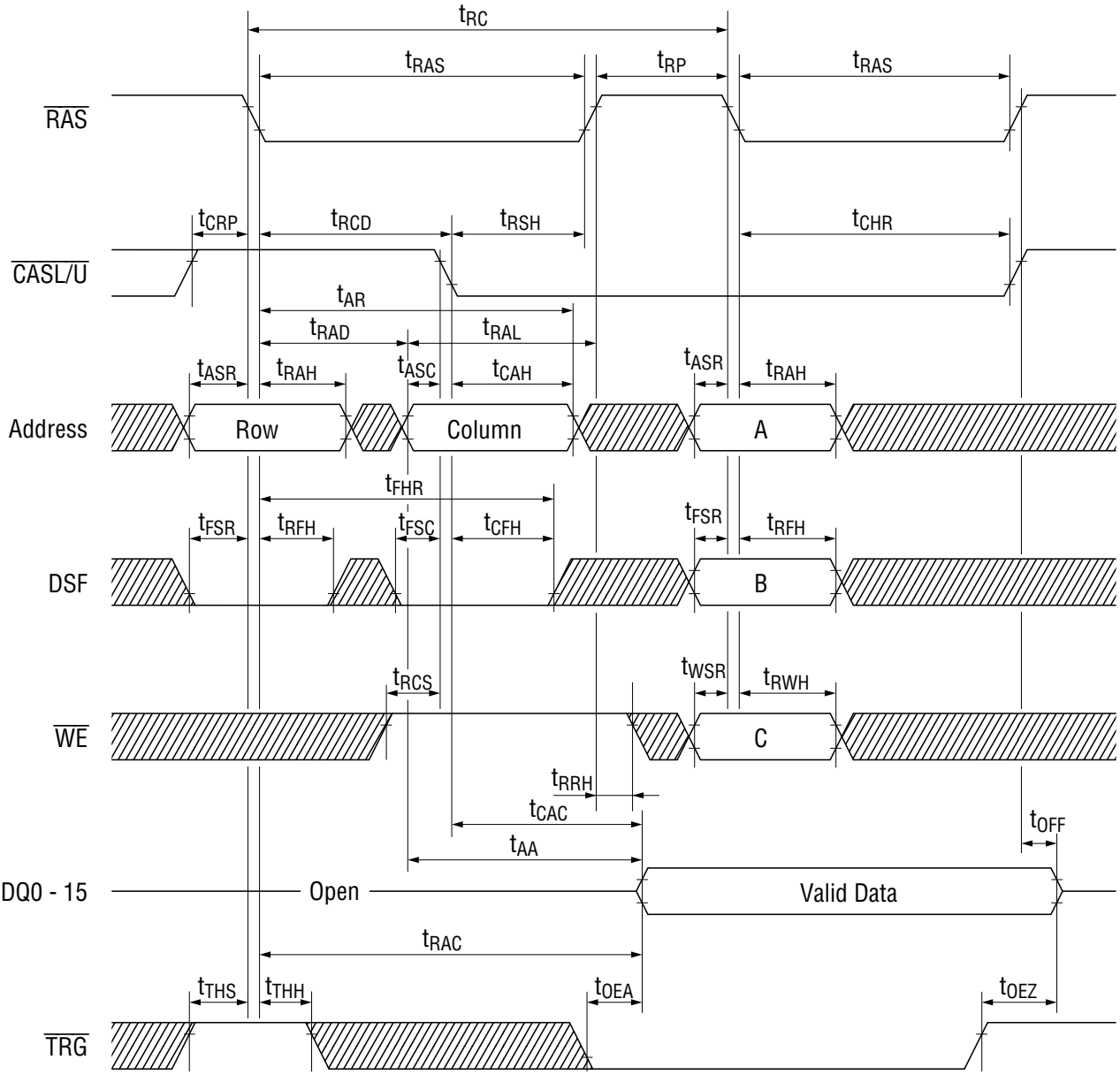
Code	$\overline{RAS}$ Falling Edge			Function
	A	B	C	
CBRR	X	0	1	CBR Refresh (Reset All Options)
CBRS	STOP Address	1	0	CBR Refresh (Set STOP Address)
CBRN	X	1	1	CBR Refresh (No Reset Options)

$\overline{CAS}$ before $\overline{RAS}$ Self-Refresh Cycle



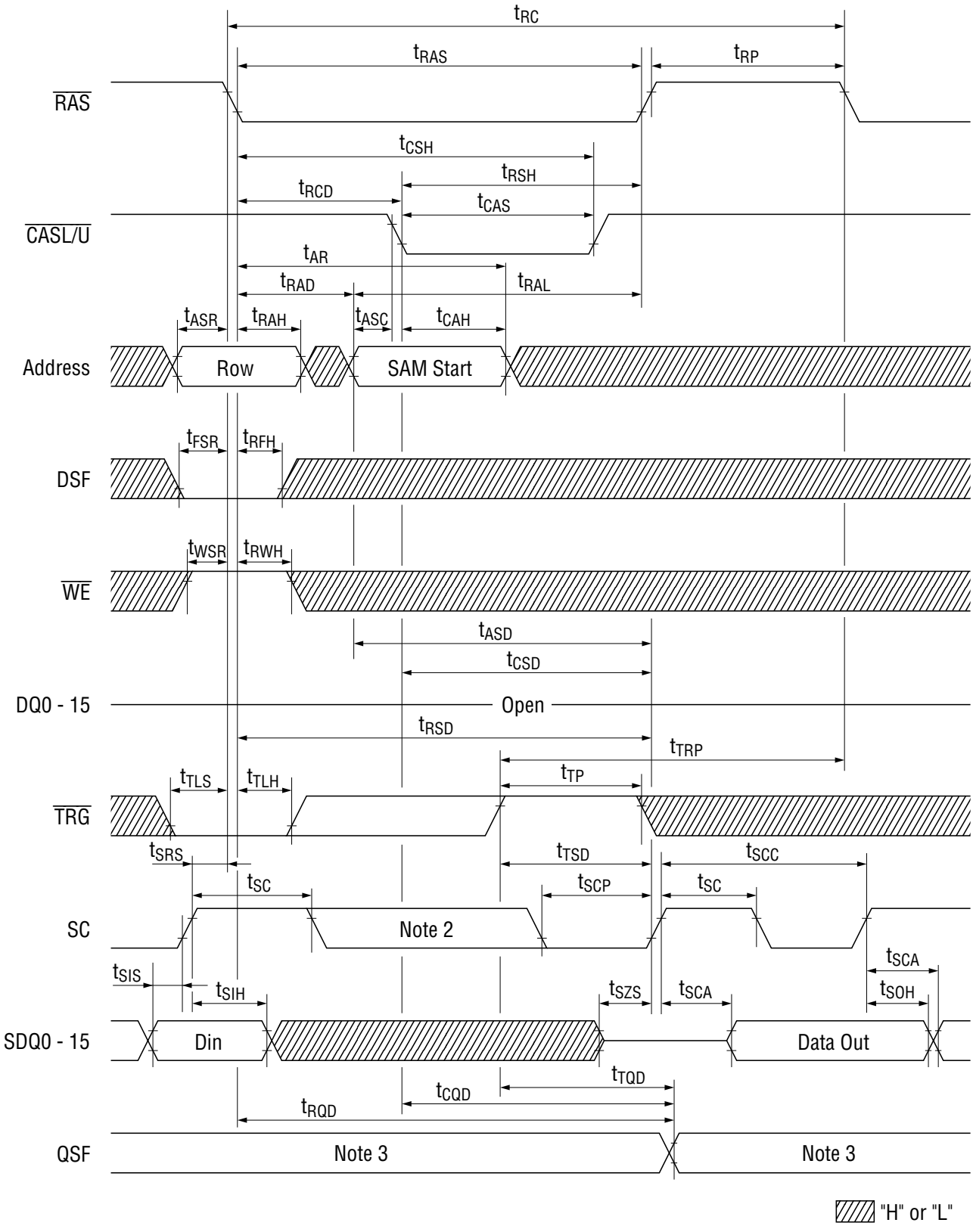
Note: Address, DSF, $\overline{WE}$, $\overline{TRG}$ = "H" or "L"

Hidden Refresh Cycle



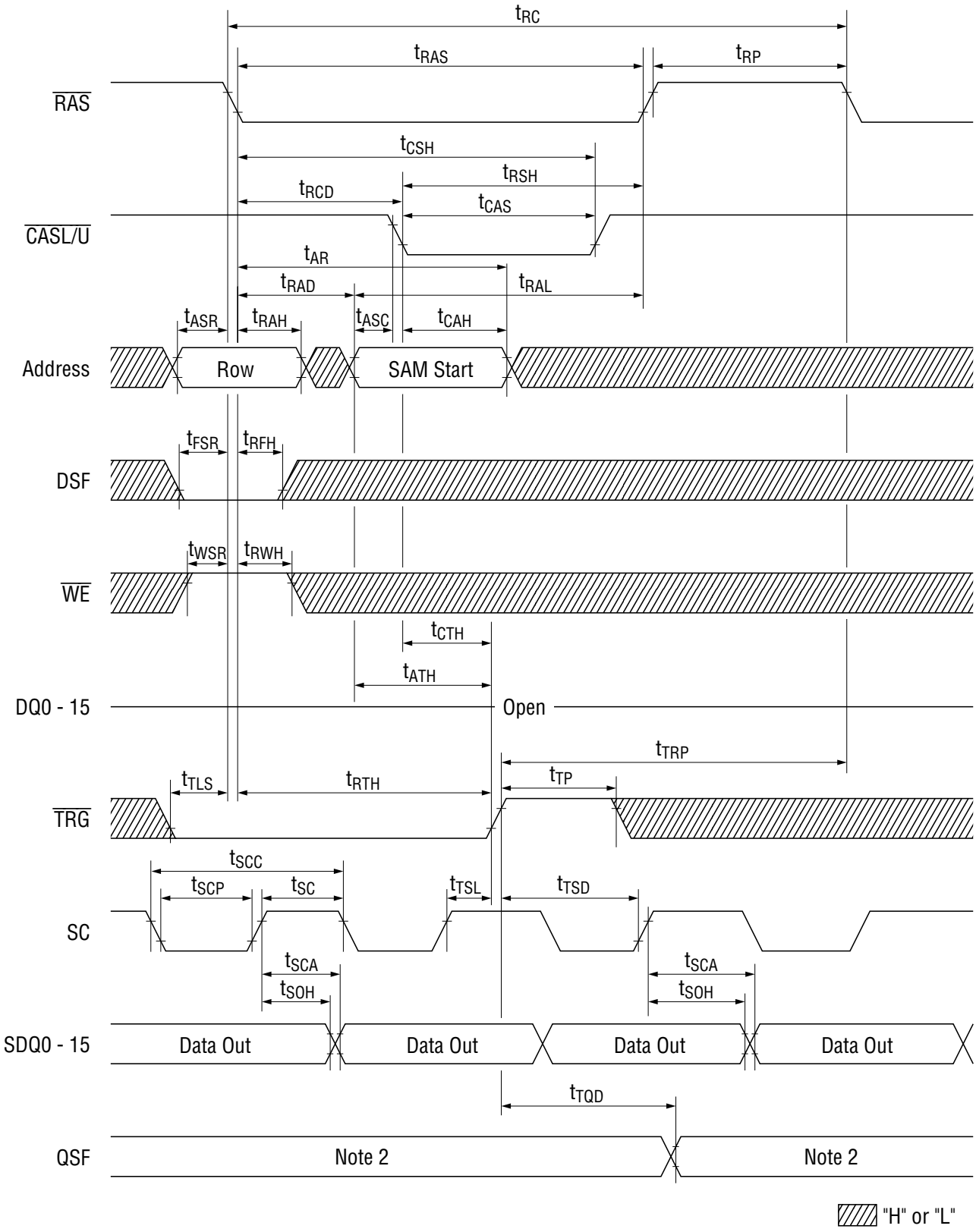
Note: The type of CBR operations are determined by the logic states of "A", "B" and "C".

Read Transfer 1



Note 1: $\overline{SE}$ = "L"
Note 2: There must be no rising transitions
Note 3: QSF = "L"-- Lower SAM (0 - 255) is active
QSF = "H"-- Upper SAM (256 - 511) is active

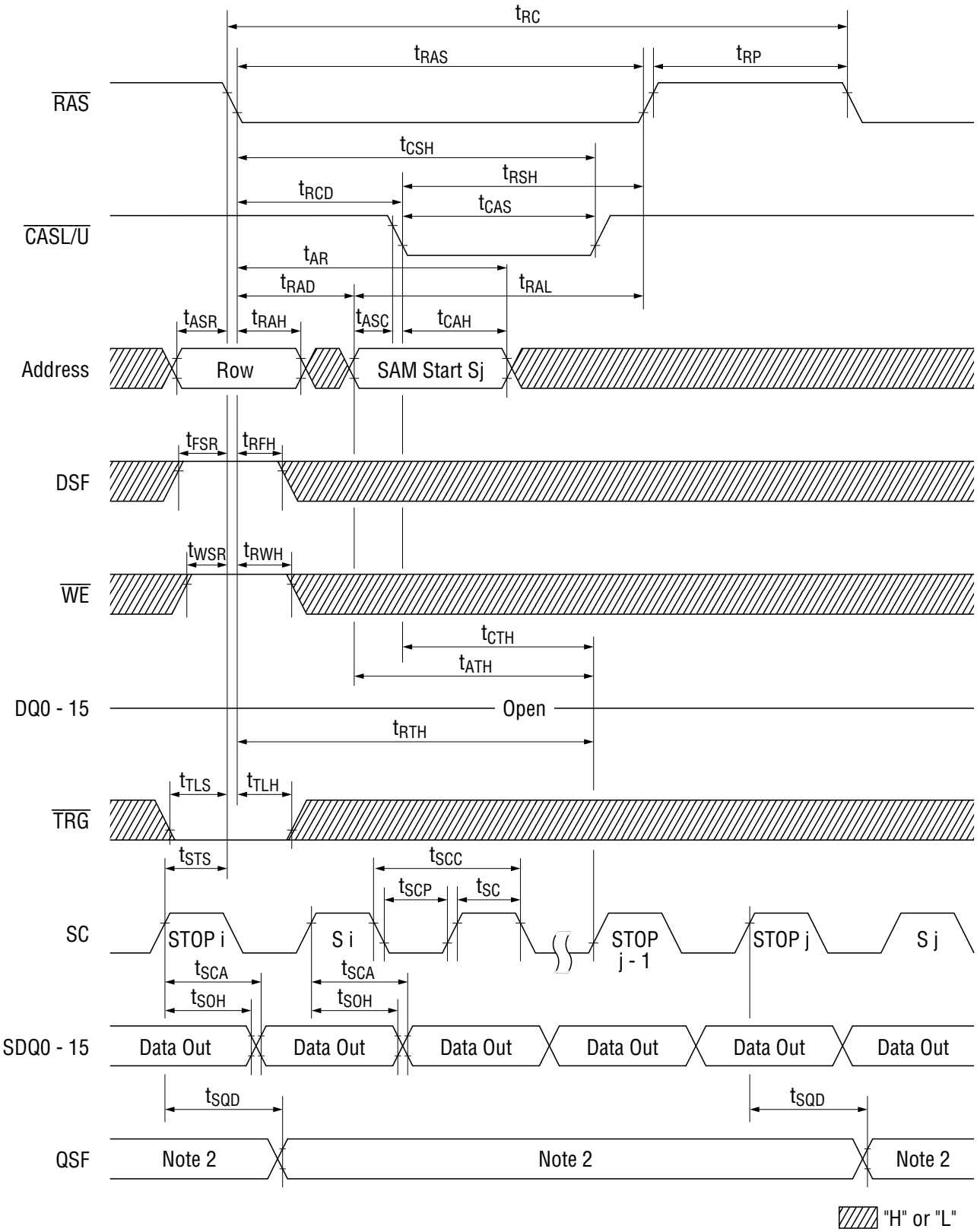
Read Transfer 2 (Real Time Read Transfer)



Note 1: $\overline{SE}$ = "L"

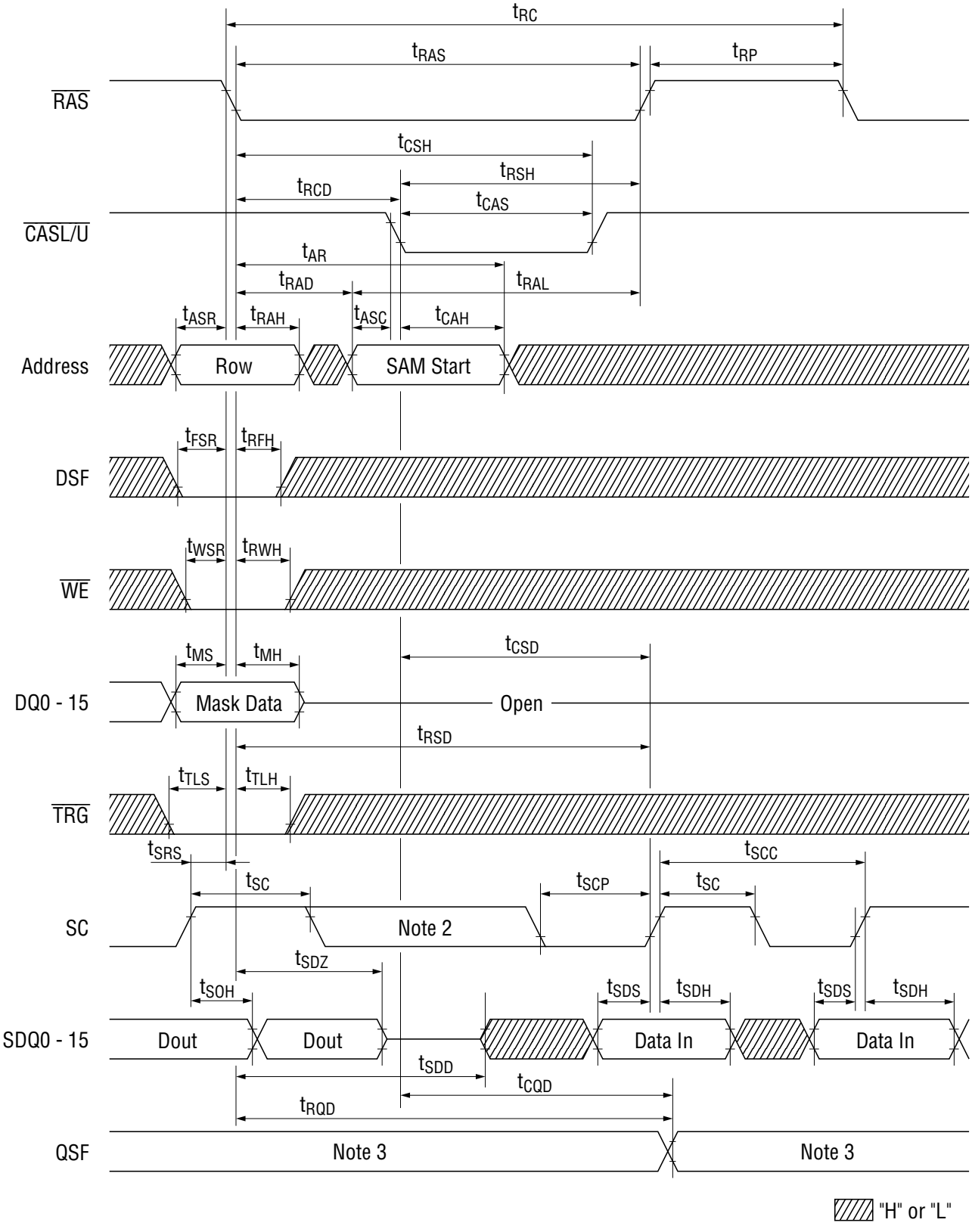
Note 2: QSF = "L"-- Lower SAM (0 - 255) is active
QSF = "H"-- Upper SAM (256 - 511) is active

Split Read Transfer



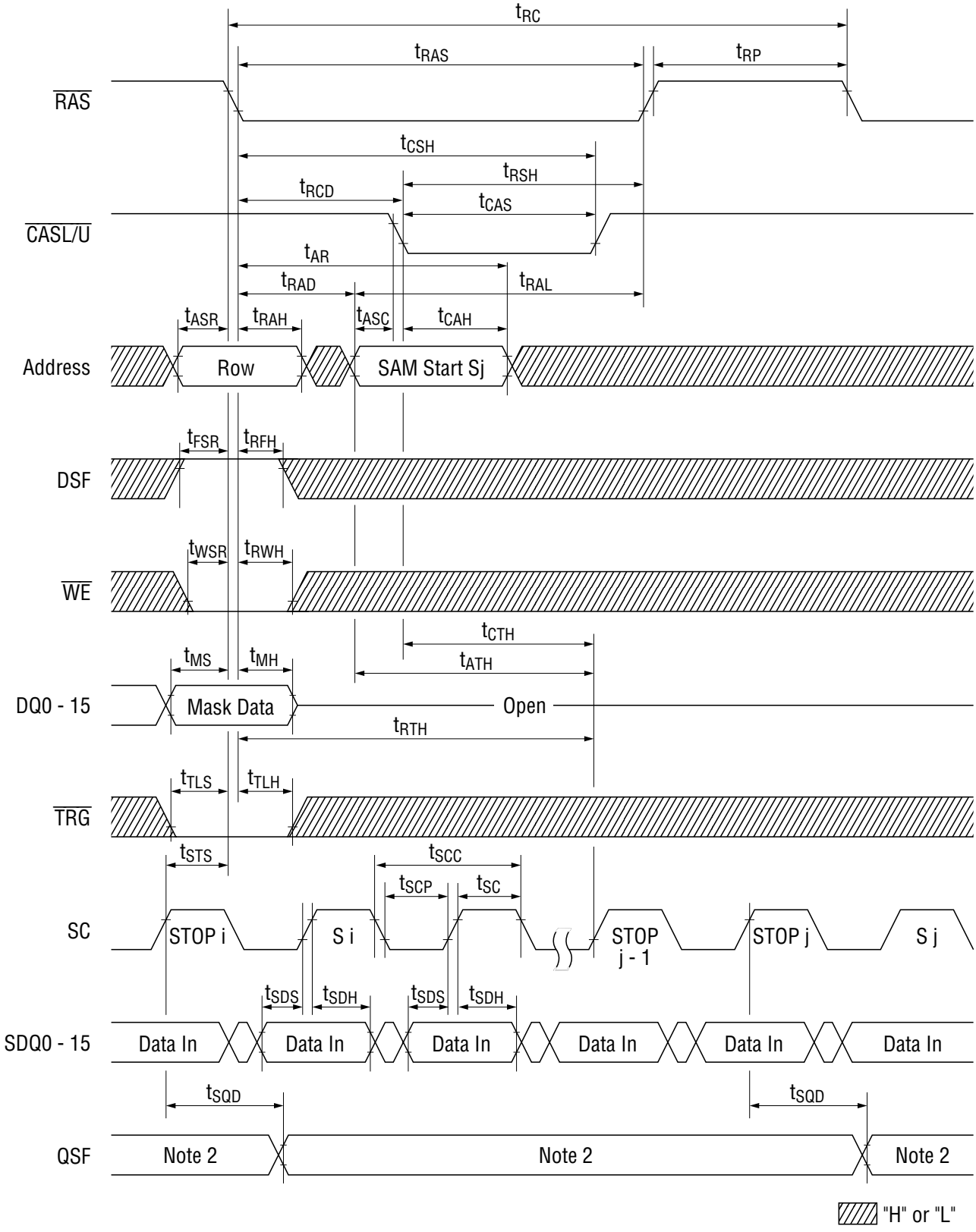
Note 1: $\overline{SE}$ = "L"
Note 2: QSF = "L"-- Lower SAM (0 - 255) is active
QSF = "H"-- Upper SAM (256 - 511) is active
Note 3: Si is the SAM start address in before SRT
Note 4: STOP i and STOP j are programmable stop addresses

Masked Write Transfer



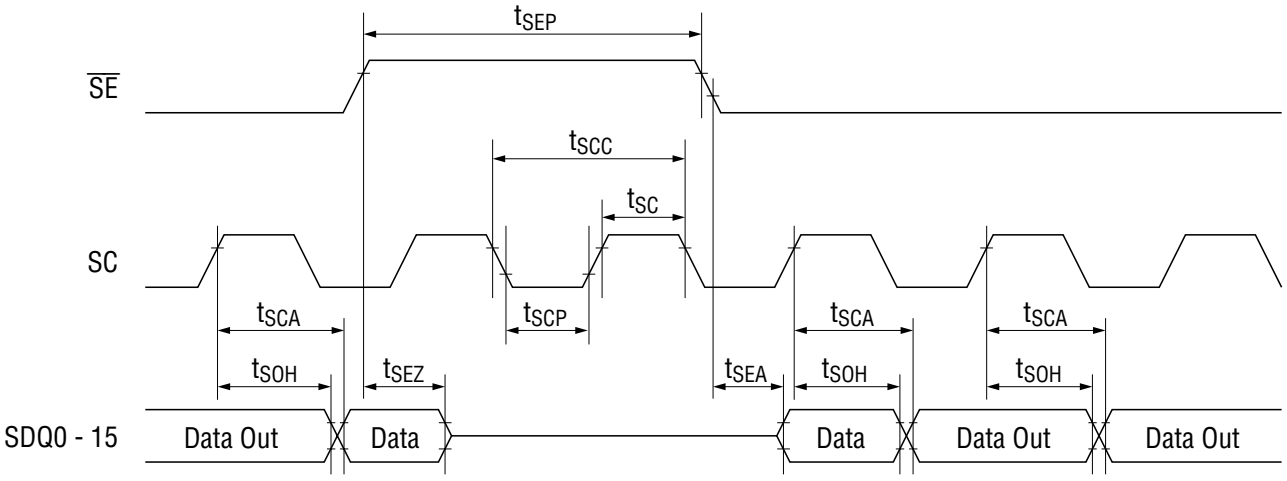
Note 1: $\overline{SE}$ = "L"
Note 2: There must be no rising transitions
Note 3: QSF = "L"-- Lower SAM (0 - 255) is active
QSF = "H"-- Upper SAM (256 - 511) is active

Masked Split Write Transfer

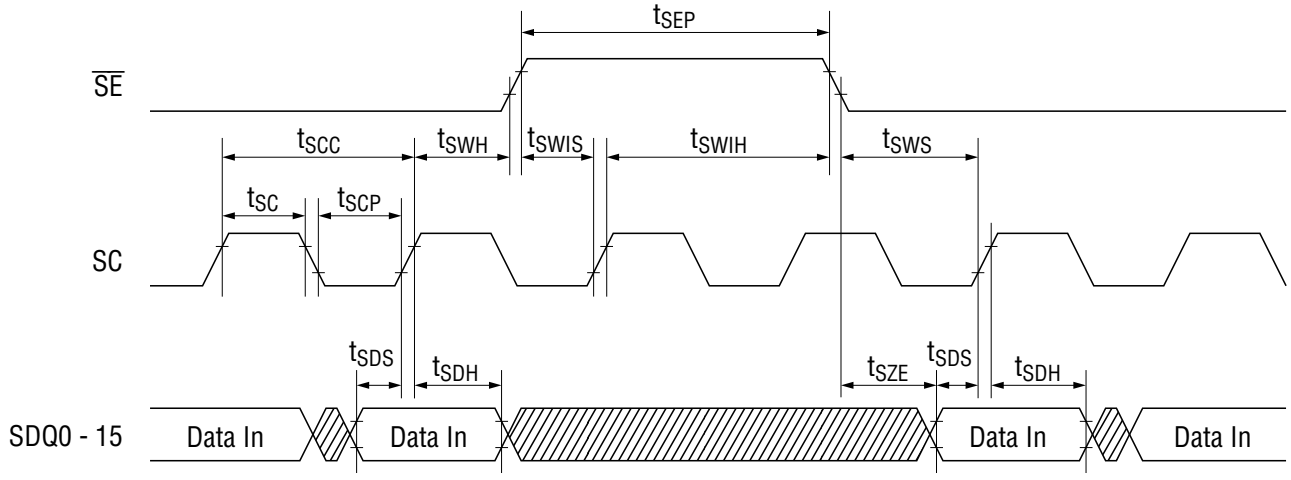


Note 1: $\overline{SE}$ = "L"
Note 2: QSF = "L"-- Lower SAM (0 - 255) is active
QSF = "H"-- Upper SAM (256 - 511) is active
Note 3: Si is the SAM start address in before SWT
Note 4: STOP i and STOP j are programmable stop addresses

Serial Read Cycle



Serial Write Cycle



"H" or "L"

PIN FUNCTIONS

Address Input: A0 - A8

The 18 address bits decode 16 bits of the 4,194,304 locations in the MSM54V16273 memory array. The address bits are multiplexed to 9 address input pins (A0 - A8) as standard DRAM. 9 row address bits are latched at the falling edge of $\overline{RAS}$. The following 9 column address bits are latched at the falling edge of $\overline{CAS}$.

Row Address Strobe: $\overline{RAS}$

$\overline{RAS}$ is a basic RAM control signal. The RAM port is in standby mode when the $\overline{RAS}$ level is "high". As the standard DRAM's $\overline{RAS}$ signal function, $\overline{RAS}$ is the control input that latches the row address bits, and a random access cycle begins at the falling edge of $\overline{RAS}$.
In addition to the conventional $\overline{RAS}$ signal function, the level of the input signals $\overline{CAS}$, $\overline{TRG}$, $\overline{WE}$ and DSF at the falling edge of $\overline{RAS}$, determines the MSM54V16273 operation mode.

Column Address Strobe: $\overline{CASL}$ and $\overline{CASU}$

As the standard DRAM's $\overline{CAS}$ signal function, $\overline{CAS}$ is the control input signal that latches the column address input, and the state of the special function input DSF to select in conjunction with the $\overline{RAS}$ control, either read/write operations or the special block write feature on the RAM port when the DSF is held "low" at the falling edge of $\overline{RAS}$.
$\overline{CAS}$ also acts as a RAM port output enable signal.

Data Transfer/Output Enable: $\overline{TRG}$

$\overline{TRG}$ is also a control input signal having multiple functions. As the standard DRAM's $\overline{OE}$ signal function, $\overline{TRG}$ is used as an output enable control when $\overline{TRG}$ is "high" at the falling edge of $\overline{RAS}$. In addition to the conventional $\overline{OE}$ signal function, a data transfer operation is started between the RAM port and the SAM port when $\overline{TRG}$ is "low" at the falling edge of $\overline{RAS}$.

Write Per Bit/Write Enable: $\overline{WE}$

$\overline{WE}$ is control input signal having multiple functions. As the standard DRAM's $\overline{WE}$ signal function, this is used to write data into the memory on the RAM port when $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$.
In addition to the conventional $\overline{WE}$ signal function, the $\overline{WE}$ determines the write-per-bit function, when $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$ during RAM port operations.
The $\overline{WE}$ also determines the direction of data transfer between the RAM and SAM. When the $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When the $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred SAM to RAM (write transfer).

Write Mask Data/Data Input and Output: DQ0 - DQ15

In conventional write-per bit mode, the DQ pins function as mask data at the falling edge of $\overline{RAS}$. Data is written only to high DQ pins. Data on low DQ pins is masked and internal data is retained. After that, they function as input/output pins similar to a standard DRAM.
In persistent write-per-bit mode, DQ pins do not consider the falling edge of $\overline{RAS}$. The mask data is determined in the mask register load cycle.

Serial Clock: SC

SC is a main serial cycle control input signal. All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read cycle, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC.
In a serial write cycle, data on SDQ pins at the rising edge of SC are fetched into the SAM register.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ is a serial access enable control and serial read/write control signal. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled. However, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Special Function Input: DSF

The DSF is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$. It allows for the selection of several RAM ports and transfer operating modes. In addition to the conventional multiport DRAM, the special functions consisting of flash write, block write, load/read color register, and split read/write transfer can be invoked.

Special Function Output: QSF

QSF is an output signal, which during split register mode indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (0 - 255) is being accessed. QSF "high" indicates that the upper SAM (256 - 511) is being accessed.
QSF is enabled by $\overline{SE}$. When $\overline{SE}$ is "high", QSF is in high impedance.

Serial Input/Output: SDQ0 - SDQ15

Serial input/output mode is determined by the most recent read or write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode.

OPERATION MODES

Table-1 shows the function truth table for a listing of all available RAM ports, and transfer operations of the MSM54V16273.
The RAM port and data transfer operations are determined by the state of $\overline{CAS}$, $\overline{TRG}$, $\overline{WE}$ and DSF at the falling edge of $\overline{RAS}$, and by the level of DSF at the falling edge of $\overline{CAS}$.

Table-1. Function Truth Table

Code	$\overline{RAS}\downarrow$				$\overline{CAS}\downarrow$	Address		W/IO		Write Mask	Pers. W.M.	Register		Function
	$\overline{CAS}$	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}\downarrow$	$\overline{CAS}\downarrow$	$\overline{RAS}\downarrow$	$\overline{CAS}$ /$\overline{WE}\downarrow$			WM	Color	
CBRR	0	*	1	0	—	*	*	*	*	—	Reset	Reset	—	CBR Refresh (Register Reset)
CBRS	0	*	0	1	—	STOP	*	*	*	—	—	—	—	CBR Refresh (Stop Register Set)
CBRN	0	*	1	1	—	*	*	*	*	—	—	—	—	CBR Refresh (No Reset)
ROR	1	1	*	0	—	Row	—	*	—	—	—	—	—	$\overline{RAS}$ Only Refresh
MWT	1	0	0	0	*	Row	TAP	WM1	*	Yes	No/ Yes	Load Use	—	Masked Write Transfer
MSWT	1	0	0	1	*	Row	TAP	WM1	*	Yes	No/ Yes	Load Use	—	Masked Split Write Transfer
RT	1	0	1	0	*	Row	TAP	*	*	—	—	—	—	Read Transfer
SRT	1	0	1	1	*	Row	TAP	*	*	—	—	—	—	Split Read Transfer
RWM	1	1	0	0	0	Row	Column	WM1	Din,Dout	Yes	No/ Yes	Load Use	—	Read/Write (New/Old Mask)
BWM	1	1	0	0	1	Row	Column A3c - 8c	WM1	Column Select	Yes	No/ Yes	Load Use	Use	Masked Block Write (New/Old)
FWM	1	1	0	1	*	Row	*	WM1	—	Yes	No/ Yes	Load Use	Use	Masked Flash Write (New/Old)
RW	1	1	1	0	0	Row	Column	*	Din,Dout	No	No	—	—	Read/Write (No Mask)
BW	1	1	1	0	1	Row	Column A3c - 8c	*	Column Select	No	No	—	Use	Block Write (No Mask)
LMR	1	1	1	1	0	Row	*	*	Mask Data	—	Set	Load	—	Load Mask Register (Old Mask Set)
LCR	1	1	1	1	1	Row	*	*	Color Data	—	—	—	Load	Load Color Register

Notes: 1. With CBRS and SAM operations use stop register.
2. After LMR, RWM, BWM, FWM and MSWT, use the old mask which can be reset by CBRR.

If the DSF is "high" at the falling edge of $\overline{RAS}$, special functions such as split transfer, flash write, load mask register, load color register, CBRS and CBRN can be invoked.
If the DSF is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write feature can be invoked.

RAM PORT OPERATION

Extended RAM Read Cycle: $\overline{RAS}$ falling edge --- $\overline{TRG}$ = $\overline{CAS}$ = "H", DSF = "L"
$\overline{CAS}$ falling edge --- DSF = "L"

The MSM54V16273 offers an accelerated page mode cycle (EXTENDED PAGE MODE) by eliminating output disable from $\overline{CAS}$ "high", and it allows $\overline{CAS}$ precharge time (t_{CP}) to occur without the output data becoming invalid. This new data out operates (Extended data out) as any RAM read or Page Mode Read, except data will be held valid after $\overline{CAS}$ goes "high", as long as $\overline{RAS}$ is "low".
Byte read occurs if either $\overline{CASL}$ or $\overline{CASU}$ falls during the cycle.

RAM Write Cycle: $\overline{RAS}$ falling edge --- $\overline{TRG}$ = $\overline{CAS}$ = "H", DSF = "L"
$\overline{CAS}$ falling edge --- DSF = "L"

1) Write cycle with no mask: $\overline{RAS}$ falling edge -- $\overline{WE}$ = "H"

If $\overline{WE}$ is set "low" at the falling edge of $\overline{CAS}$ after $\overline{RAS}$ goes "low", a write cycle is excuted. If $\overline{WE}$ is set "low" before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle, and all DQ pins attain high impedance.
If $\overline{WE}$ is "low" when $\overline{CAS}$ goes "low", the write affects only those corresponding 8 bits with the latched data.
If $\overline{WE}$ is set "low" after the $\overline{CAS}$ falling edge, this cycle becomes a late write cycle, and all 16 data are latched on the falling edge of $\overline{WE}$.
Byte write occurs if either $\overline{CASL}$ or $\overline{CASU}$ falls during the cycle. DQ pins don't achieve high impedance in this cycle, so data should be entered with $\overline{TRG}$ in "high".

2) Write cycle with mask: $\overline{RAS}$ falling edge -- $\overline{WE}$ = "L"

If $\overline{WE}$ is set "low" at the falling edge of $\overline{RAS}$, two modes of mask write can be invoked.
#1 In new mask mode mask data is loaded and used. The mask data on DQ0 - DQ15 is latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data is low, writing is inhibited into the RAM and the mask data is high, data is written into the RAM. This mask data is in effect during the $\overline{RAS}$ cycle. In page mode cycle the mask data is retained during page access.
#2 If a load mask register cycle (LMR) has been performed, the mask data is not loaded from DQ pins, and the mask data stored in the mask register is persistently used.
This operation is known as persistent write mask, set by LMR and reset by CBRR.

Load/Read Color Register: **$\overline{RAS}$ falling edge --- $\overline{CAS}$ = $\overline{TRG}$ = $\overline{WE}$ = DSF = "H"**
$\overline{CAS}$ falling edge --- DSF = "H"

The MSM54V16273 is provided with an on-chip 16-bit color register for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks.
The data presented on the DQi lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WE}$ whichever occurs later.
The read color register cycle is activated by holding $\overline{WE}$ "high" at the falling edge of $\overline{CAS}$, and throughout the remainder of the cycle. The data in the color register becomes valid on the DQi lines after the specified access times from $\overline{RAS}$ and $\overline{TRG}$ are satisfied.
During the load/read color register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

Load/Read Mask Register: **$\overline{RAS}$ falling edge --- $\overline{CAS}$ = $\overline{TRG}$ = $\overline{WE}$ = DSF = "H"**
$\overline{CAS}$ falling edge --- DSF = "L"

The MSM54V16273 is provided with an on-chip 16-bit mask register for use during the mask write cycle, flash write cycle, block write cycle, masked write transfer, and masked split write transfer. Each bit of the mask register corresponds to one of the DRAM I/O blocks.
The data presented on the DQi lines is subsequently latched into the mask register at the falling edge of either $\overline{CAS}$ or $\overline{WE}$ whichever occurs later.
The read mask register cycle is activated by holding $\overline{WE}$ "high" at the falling edge of $\overline{CAS}$, and throughout the remainder of the cycle. The data in the mask register becomes valid on the DQi lines after the specified access times from $\overline{RAS}$ and $\overline{TRG}$ are satisfied.
During the load/read mask register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

Flash Write: $\overline{RAS}$ falling edge --- $\overline{CAS}$ = $\overline{TRG}$ = DSF = "H", $\overline{WE}$ = "L"

Flash write allows for the data in the color register to be written into all the memory locations of a selected row.
Each bit of the color register corresponds to one of the DRAM I/O blocks. The flash write operation can be selectively controlled on an I/O basis in the same manner as the write per bit operation. The mask data is the same as that of a RAM write cycle.

Block Write: $\overline{RAS}$ falling edge --- $\overline{CAS}$ = $\overline{TRG}$ = "H", DSF = "L"
$\overline{CAS}$ falling edge --- DSF = "H"

Block write allows for the data in the color register to be written into 8 consecutive column address locations, starting from a selected column address in a selected row.
The block write operation can be selectively controlled on an I/O basis, and a column mask capability is also available. This function is implemented as lower byte and upper byte. During a block write cycle, the 3 least significant column address locations (A0C, A1C and A2C) are internally controlled, and only the 6 most significant column addresses (A3C - A8C) are latched at the falling edge of $\overline{CAS}$.

1) No mask block write: $\overline{WE}$ "high" at the falling edge of $\overline{RAS}$
   The data on 16 DQ pins is cleared by the data of the color register.
2) Masked block write: $\overline{WE}$ "low" at the falling edge of $\overline{RAS}$
   The mask data is the same as that of a RAM write cycle. (new mask and persistent mask)

	Bit 0	Bit 15
Color Register	11001110	01110011
I/O Mask	11111010	01101011
Column Mask	10010011	00111100
	Lower Byte	Upper Byte

	8 Column × 8 DQ (Lower Byte)								8 Column × 8 DQ (Upper Byte)							
Column 7	1	1	0	0	1	*	1	*	*	*	*	*	*	*	*	*
Column 6	1	1	0	0	1	*	1	*	*	*	*	*	*	*	*	*
Column 5	*	*	*	*	*	*	*	*	*	1	1	*	0	*	1	1
Column 4	*	*	*	*	*	*	*	*	*	1	1	*	0	*	1	1
Column 3	1	1	0	0	1	*	1	*	*	1	1	*	0	*	1	1
Column 2	*	*	*	*	*	*	*	*	*	1	1	*	0	*	1	1
Column 1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Column 0	1	1	0	0	1	*	1	*	*	*	*	*	*	*	*	*
	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8	DQ9	DQ10	DQ11	DQ12	DQ13	DQ14	DQ15

Note : Location "*" can not be loaded.

Example of Block Write

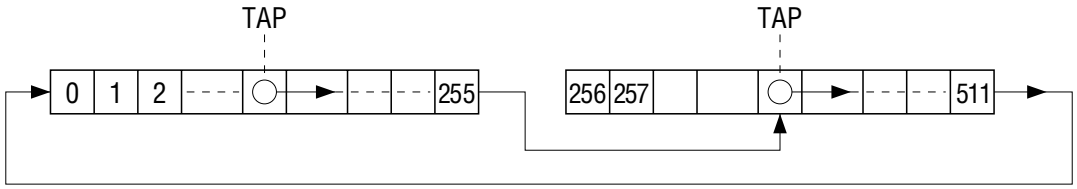
SAM PORT OPERATION

Single Register Mode

High speed serial read or write operations can be performed through the SAM port independent of the RAM port operation, except during read/write transfer cycles.
The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer is a read transfer, the SAM port is in the output mode. If the preceding transfer is write transfer, the SAM port is in the input mode.
Serial data can be read out of the SAM after a read transfer has been performed. The data is shifted out of the SAM starting at any of the 512 bits locations.
The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read or write transfer cycle. The SAM registers are configured as a circular data register. The data is shifted out sequentially. It starts from the selected TAP location at the most significant bit (511), then wraps around to the least significant bit (0).

Split Register Mode

In split register mode data can be shifted into or out of one half of the SAM, while a split read or split write transfer is being performed on the other half of the SAM.
Conventional (non split) read, or write transfer cycle must precede any split read or split write transfers. The split read and write transfers will not change the SAM port mode set by the preceding conventional transfer operation. In the split register mode, serial data can be shifted in or out of one of the split SAM registers, starting from any at the 256 TAP locations, excluding the last address of each split SAM the data is shifted in or out sequentially starting from the selected TAP location at the most significant bit (255 or 511) of the first split SAM, and then the SAM pointer moves to the TAP location selected for the second split SAM to shift data in or out sequentially, starts from this TAP location at the most significant bit (511 or 255), and finally wraps around to the least significant bit.



DATA TRANSFER OPERATIONS

The MSM54V16273 features two types of bidirectional data transfer capability between RAM and SAM.

1) Conventional (non split) transfer: 512 words by 16 bits of data can be loaded from RAM to SAM (Read transfer), or from SAM to RAM (Write transfer).
2) Split transfer: 256 words by 16 bits of data can be loaded from the lower/upper half of the RAM to the lower/upper half of the SAM (Split read transfer), or from the lower/upper half of SAM to the lower/upper half of RAM (Split write transfer).

The conventional transfer and split transfer modes are controlled by the DSF input signal.
Data transfer is invoked by holding the $\overline{TRG}$ signal "low" at the falling edge of $\overline{RAS}$.
The MSM54V16273 supports 4 types of transfer operations: Read transfer, Split read transfer, Write transfer and Split write transfer as shown in the truth table. The type of transfer operation is determined by the state of $\overline{CAS}$, $\overline{WE}$ and DSF latched at the falling edge of $\overline{RAS}$. During conventional transfer operations, the SAM port is switched from input to output mode (Read transfer), or output to input mode (Write transfer). It remains unchanged during split transfer operation (Split read transfer or Split write transfer).
Both RAM and SAM are divided by the most significant row address (AX8), as shown in Figure 1. Therefore, no data transfer between AX8 = 0 side RAM and AX8 = 1 side RAM can be provided through the SAM. Care must be taken if the split read transfer on AX8 = 1 side (or AX8 = 0 side) is provided after the read transfer or the split read transfer, is provided on AX8 = 0 side (or AX8 = 1 side).

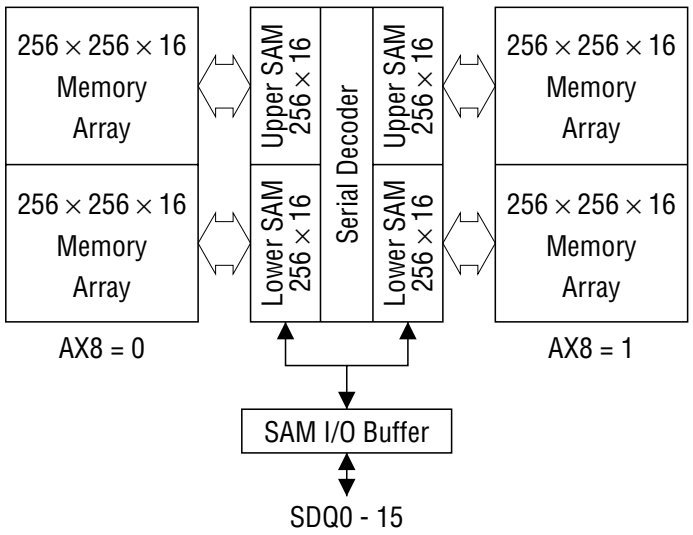


Figure 1. RAM and SAM Configuration

Read Transfer: $\overline{RAS}$ falling edge --- $\overline{CAS}$ = $\overline{WE}$ = "H", $\overline{TRG}$ = DSF = "L"

Read transfer consists of loading a selected row of data from the RAM into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{TRG}$ "low", $\overline{WE}$ "high", and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{TRG}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{TRG}$, and this data becomes valid on the SDQ lines after the specified access time t_{SCA} from the rising edge of the subsequent SC cycles. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$. In a read transfer cycle (which is preceded by a write transfer cycle), SC clock must be held at a constant V_{IL} or V_{IH} after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{TRG}$.
In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SQD lines until the $\overline{TRG}$ signal goes "high", and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{TRG}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$, and the subsequent rising edge of SC (t_{RTH}, t_{CTH} and t_{TSL}/t_{TSD} must be satisfied).

Masked Write Transfer: $\overline{RAS}$ falling edge --- $\overline{CAS}$ = "H", $\overline{TRG}$ = DSF = "L"
$\overline{WE}$ = "L"

Write transfer cycle consists of loading the content of the SAM register into a selected row of the RAM. This write transfer is the same as a mask write operation in RAM, so new and persistent (old) mask modes can be supported. (Masked write transfer)
If the SAM data to be transferred must first be loaded through the SAM, a Masked write transfer operation (all DQ pins "low" at falling edge of $\overline{RAS}$) must precede the write transfer cycles. A masked write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{TRG}$ "low", $\overline{WE}$ "low", and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.
When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{CSD} from the falling edge of the $\overline{CAS}$, at which time a new row of data can be written in the serial register.
Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to the other address of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle (row address AX8).

Split Data Transfer and QSF

The MSM54V16273 features a bidirectional split data transfer capability between the RAM and SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operation can be performed to or from one half of the serial register, while serial data can be shifted into or out of the other half of the serial register. The most significant column address location (A8C) is controlled internally to determine which half of the serial register will be reloaded from the RAM. QSF is an output which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM.

Split Read Transfer: $\overline{RAS}$ falling edge --- $\overline{CAS}$ = $\overline{WE}$ = DSF = "H", $\overline{TRG}$ = "L"

The MSM54V16273 supports two types of split register operation.
#1 Normal split register operation
#2 Boundary split register operation using programmable SAM stops described later.
Normal split read transfer consists of loading 256 words by 16 bits of data from a selected row of the split RAM into the corresponding non-active split SAM register. Serial data can be shifted out from the other half of the split SAM register simultaneously. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of real time read transfers. A split read transfer can be performed after a delay of t_{STS} from the change of state of the QSF output is satisfied. Conventional (non-split) read transfer operation must precede split read transfer cycles.

Masked Split Write Transfer: $\overline{RAS}$ falling edge --- $\overline{CAS}$ = DSF = "H", $\overline{TRG}$ = "L" $\overline{WE}$ = "L"

Split write transfer consists of loading 256 words by 16 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM. Serial data can be shifted into the other half of the split SAM register simultaneously. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. This operation is the same as a mask write operation in RAM, so new and persistent modes can be supported.
A split write transfer can be performed after a delay of t_{STS} from the change of state of the QSF output is satisfied.
A masked write transfer operation must precede split write transfer. The purpose is to switch the SAM port from output mode to input mode, and to set the initial TAP location prior to split write transfer operations.

Programmable SAM Stops in Split Transfer Cycle

The MSM54V16273 has a boundary split register operation using programmable stops. If a CBRS cycle has been performed, the split transfer cycle performs the boundary operation.
Figure 2 shows an example of a boundary split register (4 stop points). The stop points define a SAM location at which the access will change from one half of the SAM to the other half (at the TAP address).

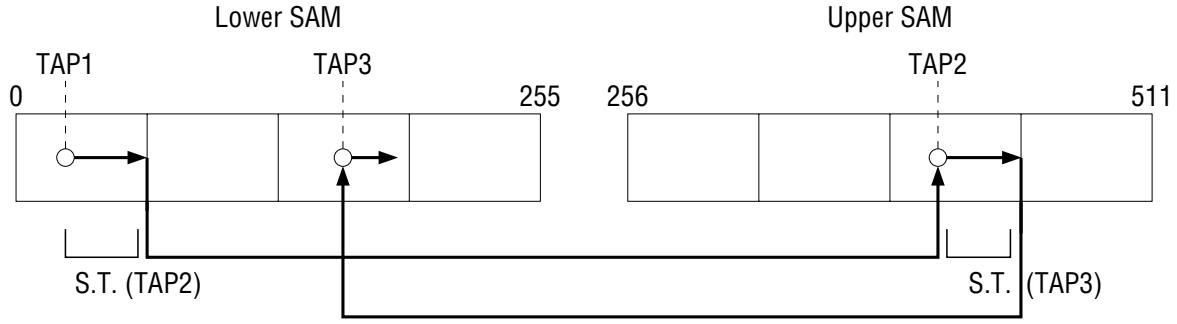


Figure 2. Example of Boundary Split Register

SAM Stop Set Cycle (CBRS): $\overline{RAS}$ falling edge --- $\overline{CAS}$ = "L", $\overline{WE}$ = "L", DSF = "H"

SAM stop location data (boundaries) are latched from address inputs at the falling edge of $\overline{RAS}$. To determine the boundary A4 - A7 are used, and A0 - A3, and A8 are ignored.
Once the CBRS is executed, the programmable SAM stop operation continues until CBRR.

SAM Stop Boundary Table

Number of Stop Points	Address				Size of Partition
	A4	A5	A6	A7	
1	1	1	1	1	256
2	1	1	1	0	128
4	1	1	0	X	64
8	1	0	X	X	32
16	0	X	X	X	16

Register Reset Cycle (CBRR): $\overline{RAS}$ falling edge --- $\overline{CAS}$ = "L", $\overline{WE}$ = "H", DSF = "L"

A CBRR can reset the programmable SAM stop operation, and persistent mask write operation. The CBRR will take effect immediately; it doesn't require a split transfer cycle.

POWER UP

Power must be applied to the $\overline{RAS}$ and $\overline{TRG}$ input signals to pull them "high" before, or at the same time as, the V_{CC} supply is turned on. After power-up, a pause of 200 µs minimum is required with $\overline{RAS}$ and $\overline{TRG}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{TRG}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$ before $\overline{RAS}$ cycles are required instead of 8 $\overline{RAS}$ cycles.

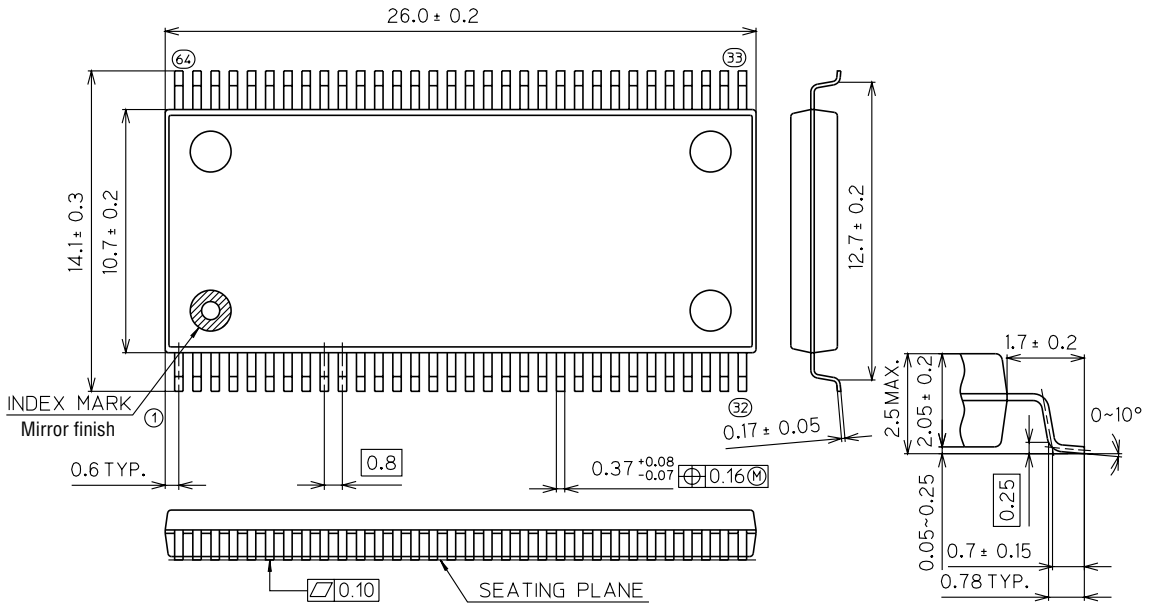
(NOTE) INITIAL STATE AFTER POWER UP

The initial state can not be guaranteed for various power up conditions and input signal levels. Therefore, it is recommended that the initial state be set (ex. Perform a CBRR cycle to select Non Persistent Write-per-bit mode) after the initialization of the device is performed and before valid operations begin.

PACKAGE DIMENSIONS

(Unit : mm)

SSOP64-P-525-0.80-K



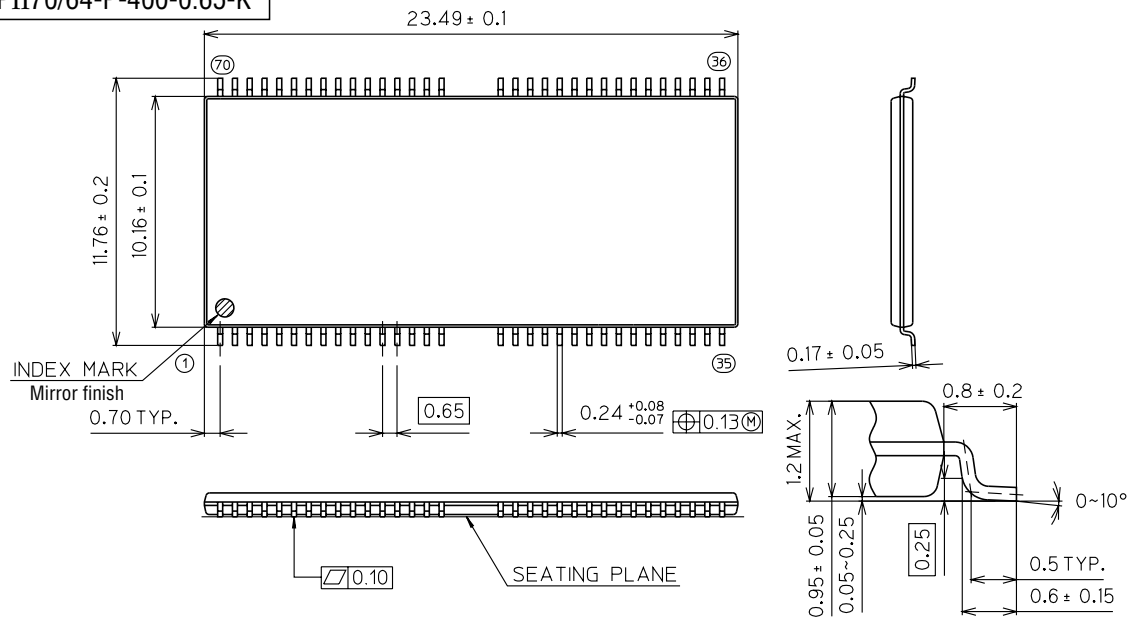
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.34 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPII70/64-P-400-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.59 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).