

MSM6404A/6404VS**High speed and High performance 4-Bit Microcontroller****GENERAL DESCRIPTION**

The MSM6404A microcontroller is a low-power device implemented in complementary metal-oxide semiconductor technology. The MSM6404A is optimized for high-speed processing and complicated-control applications.

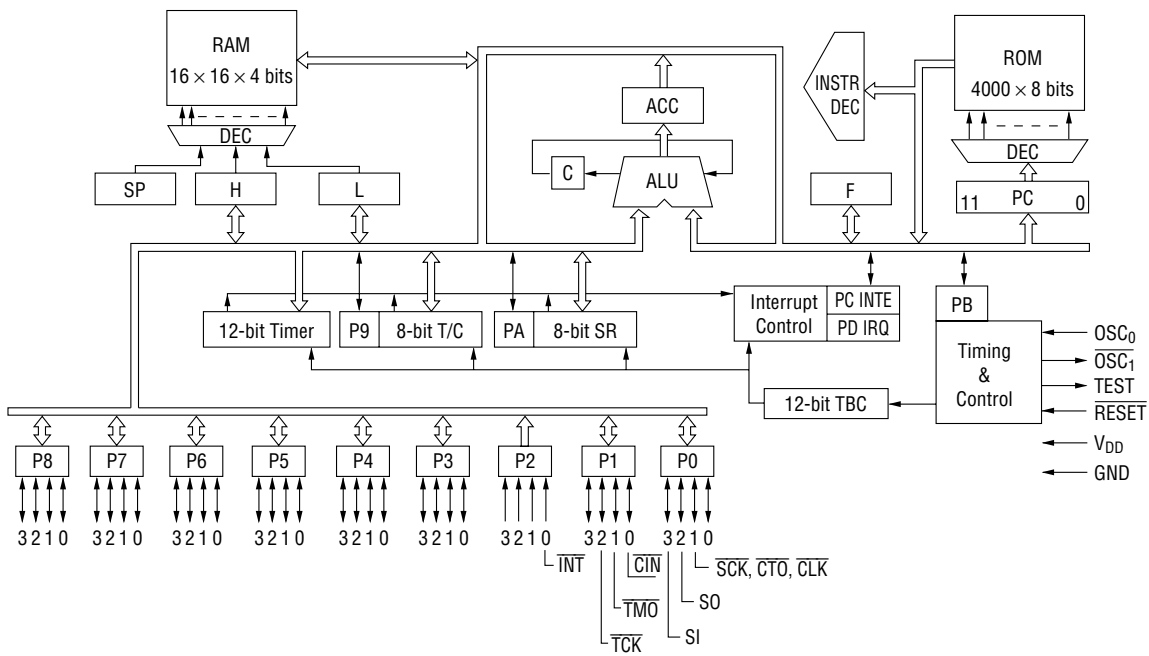
The MSM6404VS is a CMOS 4-bit microcontroller that employs an external EPROM using a piggy-back package in place of the program memory (ROM) internal to the MSM6404A. The MSM6404VS can be used for program development verification because the programs can be modified by programming an external EPROM 2732 equivalent or 2764A equivalent.

FEATURES

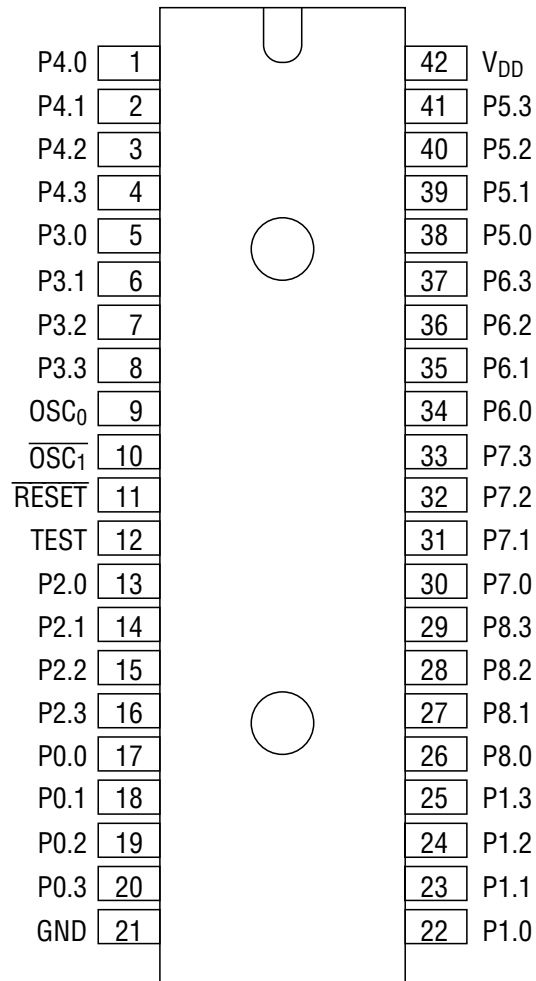
- Mask ROM (MSM6404A) : 4000 words × 8 bits
- External ROM (MSM6404VS) : 8196 words × 8 bits
- RAM (including the stack area) : 256 words × 4 bits
- I/O port
 - Input-output port : 8 ports × 4 bits
 - Input port : 1 port × 4 bits
 4 bits are for input ports having a latch; the other 32 bits are input/output ports that allow bit manipulation
- Three built-in counters : 12-bit time-base counter
12-bit programmable timer
8-bit high-speed programmable timer/event counter
- Built-in 8-bit serial I/O register (with 3-bit counter)
- Five interrupts with five priority levels (4 internal, 1 external)
- 32 stacks (in RAM)
- Power-down features
- Minimum instruction execution time : 952 ns @ 4.2 MHz clock
- Instruction systems suitable for control
- Fully static operation
- Low power consumption
- Single 5 V supply
- Package options:
 - MSM6404A
 - 42-pin plastic DIP (DIP42-P-600-2.54) : (Product name : MSM6404A-xxxRS)
 - 44-pin plastic QFP (QFP44-P-910-0.80-K) : (Product name : MSM6404A-xxxGS-K)
 - 44-pin plastic QFP (QFP44-P-910-0.80-2K) : (Product name : MSM6404A-xxxGS-2K)
 - MSM6404VS
 - 42-pin ceramic piggyback (ADIP42-C-600-2.54) : (Product name : MSM6404VS)
 xxx indicates a code number.

BLOCK DIAGRAM

MSM6404A

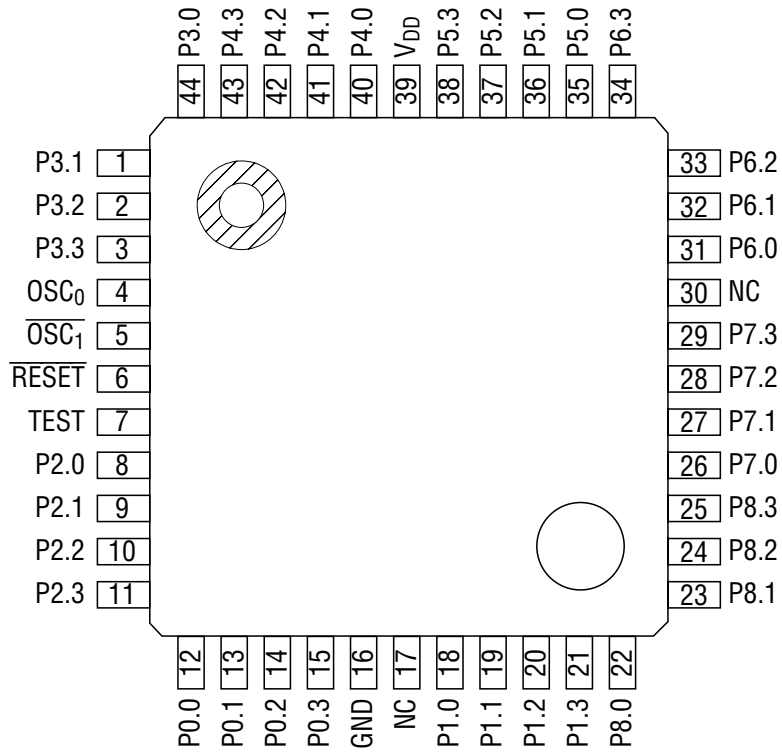


PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

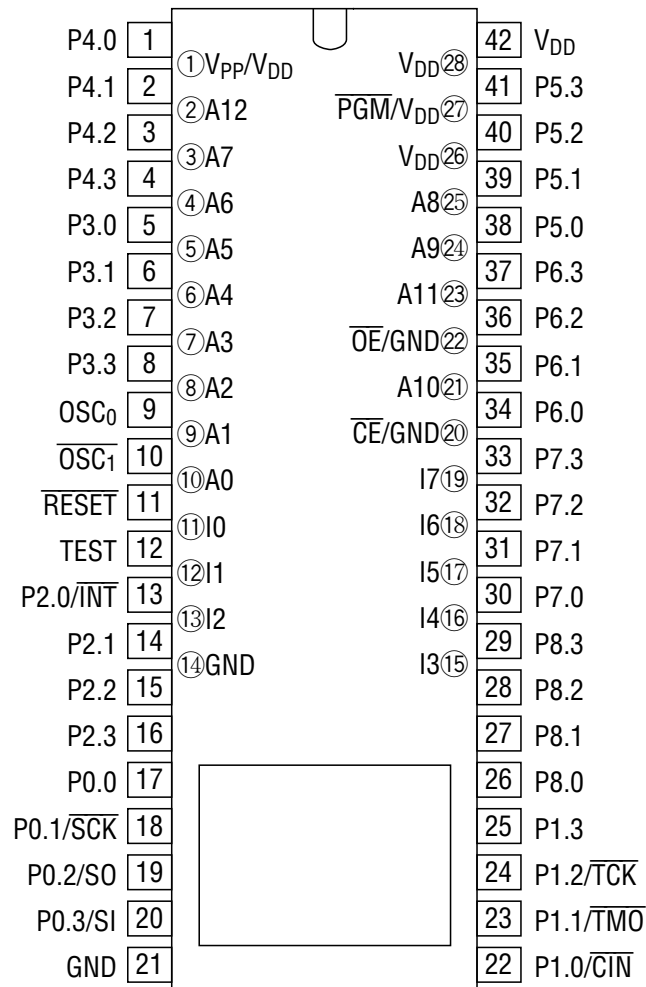
PIN CONFIGURATION (TOP VIEW) (continued)



NC: No-connection pin

44-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (continued)



42-Pin Ceramic Piggyback

PIN DESCRIPTIONS

Symbol	Type	Description	During reset
P0.0 P0.1/ $\overline{\text{SCK}}$ P0.2/SO P0.3/SI	I/O	P0.1 is shared with serial clock ($\overline{\text{SCK}}$) input/output. P0.2 is shared with serial data (SO) output. P0.3 is shared with serial data (SI) input.	"1"
P1.0/ $\overline{\text{CIN}}$ P1.1/ $\overline{\text{TMO}}$ P1.2/ $\overline{\text{TCK}}$ P1.3	I/O	P1.0 is shared with counter input ($\overline{\text{CIN}}$). P1.1 is shared with timer output ($\overline{\text{TMO}}$). P1.2 is shared with timer clock input ($\overline{\text{TCK}}$).	"1"
P2.0/ $\overline{\text{INT}}$ P2.1 P2.2 P2.3	I	P2.0 is shared with external interrupt input ($\overline{\text{INT}}$). } Input port with a latch, built-in pull-up resistor	The latch is reset.
P3.0 to 3.3	I/O	—	"1"
P4.0 to 4.3 P5.0 to 5.3	I/O I/O	} 8-bit output ports (at OPT instruction execution)	"0"
P6.0 to 6.3	I/O	—	"0"
P7.0 to 7.3	I/O	—	"0"
P8.0 to 8.3	I/O	—	"0"
OSC ₀ $\overline{\text{OSC}}_1$	I O	Crystal connection pins for clock oscillation	Oscillation waveform
TEST	O		
$\overline{\text{RESET}}$	I	Input pin for system reset	—
V _{DD} GND	—	Power supply voltage pins	—

Note: 1. The ports except for pins P2.0 to P2.3 are pseudo bidirectional ports.
 2. When each port is used for output, the MSM6404A can drive one TTL (one input) and the MSM6404VS can drive one LS TTL (one input).

Upper Pins for MSM6404VS

Symbol	Type	Description
A0 to A12	O	Address output
I0 to I7	I	Data input
$\overline{\text{CE}}$ /GND	I	Chip enable input
$\overline{\text{OE}}$ /GND	I	Output enable input
$\overline{\text{PGM}}$ /V _{DD}	I	Program input
V _{DD} GND	—	Power supply voltage pins
V _{PP} /V _{DD}	—	Programmed power supply voltage pin

ABSOLUTE MAXIMUM RATINGS (MSM6404A)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +7	V
Input Voltage	V_I		-0.3 to V_{DD}	V
Output Voltage	V_O		-0.3 to V_{DD}	V
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$ per package	200 max.	mW
		$T_a = 25^\circ\text{C}$ per output	50 max.	mW
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS (MSM6404A)

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	$f_{OSC} \leq 1 \text{ MHz}$	3 to 6	V
		$f_{OSC} \leq 4.2 \text{ MHz}$	4.5 to 5.5	V
Data-Hold Voltage	V_{DDH}	$f_{OSC} = 0 \text{ Hz}$	2 to 6	V
Operating Temperature	T_{op}	—	-40 to +85	$^\circ\text{C}$
Fan Out	N	MOS load	15	—
		TTL load	1	

Note: Refer to the f_{OSC} - V_{DD} characteristic in OPERATING CHARACTERISTICS for the relationship between power supply voltage and operating frequency.

ELECTRICAL CHARACTERISTICS (MSM6404A)

DC Characteristics

(V_{DD} = 5 V ±10%, T_a = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage*1, *2	V _{IH}	—	2.4	—	V _{DD}	V
"H" Input Voltage*3, *4	V _{IH}	—	3.6	—	V _{DD}	V
"L" Input Voltage	V _{IL}	—	-0.3	—	+0.8	V
"H" Output Voltage*1, *5	V _{OH}	I _O = -15 μA	4.2	—	—	V
"L" Output Voltage*1	V _{OL}	I _O = 1.6 mA	—	—	0.4	V
"L" Output Voltage*5	V _{OL}	I _O = 15 μA	—	—	0.4	V
Input Current*3	I _{IH} /I _{IL}	V _I = V _{DD} /0 V	—	—	15/-15	μA
Input Current*2, *4	I _{IH} /I _{IL}	V _I = V _{DD} /0 V	—	—	1/-30	μA
"H" Output Current*1	I _{OH}	V _O = 2.4 V	-0.1	—	—	mA
"H" Output Current*1	I _{OH}	V _O = 0.4 V	—	—	-1.2	mA
Input Capacitance	C _I	f = 1 MHz, T _a = 25°C	—	5	—	pF
Output Capacitance	C _O		—	7	—	
Power Supply Current (In Stop Mode)	I _{DDs}	V _{DD} = 2 V, no load, T _a = 25°C	—	0.2	5	μA
		No load	—	1	100	μA
Power Supply Current	I _{DD}	Crystal oscillation f = 4.194304 MHz, no load	—	6	12	mA

*1 Applied to P0, P1, P3, P4, P5, P6, P7 and P8.

*2 Applied to P2.

*3 Applied to OSC₀.*4 Applied to RESET.*5 Applied to OSC₁.

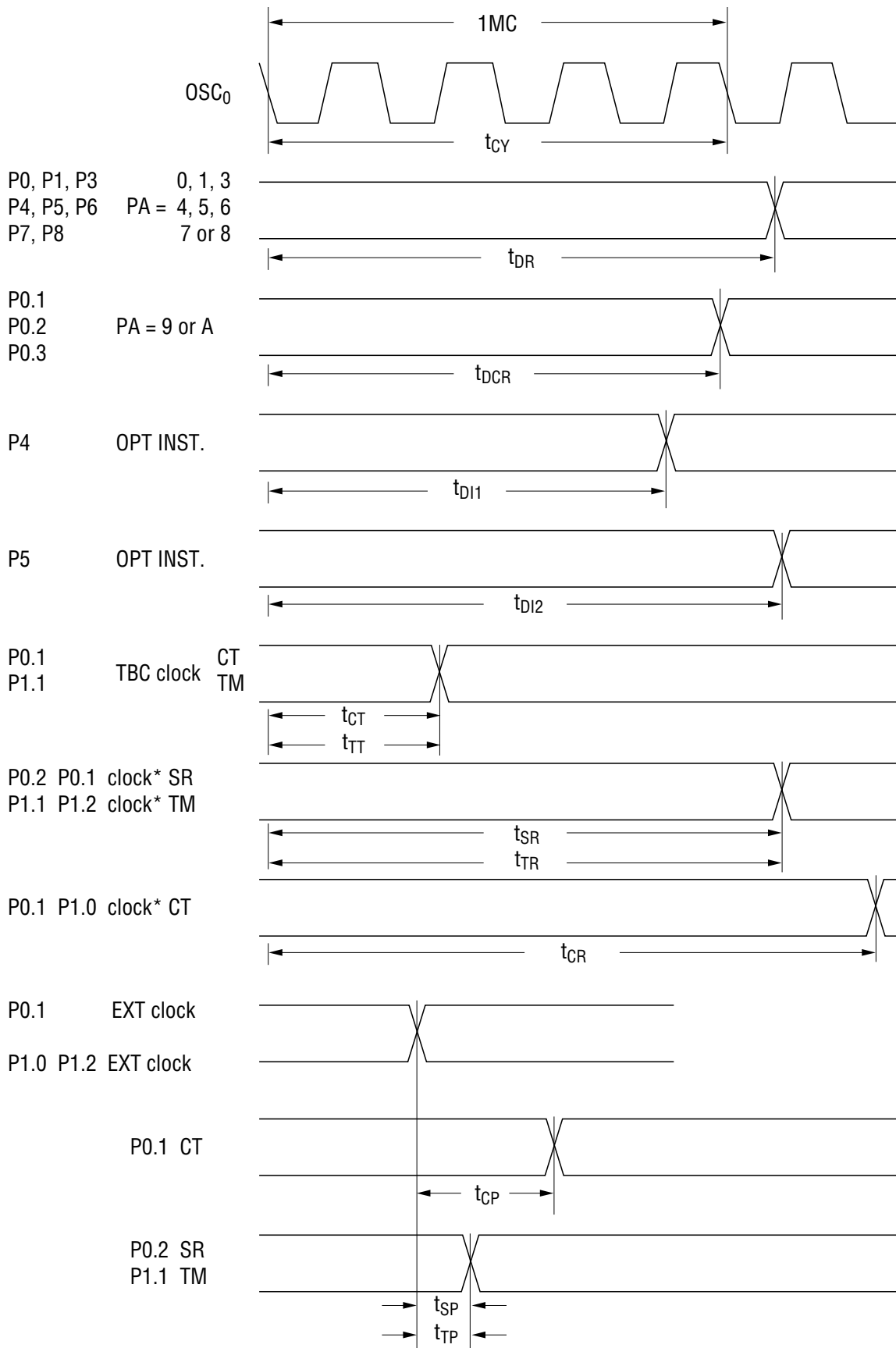
AC Characteristics (MSM6404A)

(V_{DD} = 5 V ±10%, T_a = -40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (OSC ₀) Pulse Width	t _{φW}	—	119	—	—	ns
Cycle Time	t _{CY}	—	952	—	—	ns
Input Data Setup Time	t _{DS}	—	120	—	—	ns
Input Data Hold Time	t _{DH}	—	120	—	—	ns
SR/TM Clock Pulse Width	t _{WS} /t _{WT}	—	120	—	—	ns
CT Clock Pulse Width	t _{WC}	—	2/8 t _{CY} + 120	—	—	ns
P2 Input Data Clock Pulse Width	t _{WP}	—	120	—	—	ns
SR Data Setup Time	t _{SS}	—	120	—	—	ns
SR Data Hold Time	t _{SH}	—	120	—	—	ns
Data Delay Time	t _{DR}	C _L = 15 pF	—	—	t _{CY} + 300	ns
Data Delay Time at Mode Switching	t _{DCR}	C _L = 15 pF	—	—	7/8 t _{CY} + 300	ns
Data Delay Time at OPT Instruction	t _{DI1}	C _L = 15 pF	—	—	6/8 t _{CY} + 300	ns
Data Delay Time at OPT Instruction	t _{DI2}	C _L = 15 pF	—	—	7/8 t _{CY} + 300	ns
CT/TM Data Delay Time Using TBC Clock	t _{CT} /t _{TT}	C _L = 15 pF	—	—	2/8 t _{CY} + 360	ns
SR/TM Data Delay Time Using PORT Clock	t _{SR} /t _{TR}	C _L = 15 pF	—	—	t _{CY} + 480	ns
CT Data Delay Time Using PORT Clock	t _{CR}	C _L = 15 pF	—	—	10/8 t _{CY} + 480	ns
CT Data Delay Time Using External Clock	t _{CP}	C _L = 15 pF	—	—	2/8 t _{CY} + 360	ns
SR/TM Data Delay Time Using External Clock	t _{SP} /t _{TP}	C _L = 15 pF	—	—	360	ns
SR Clock Invalid Time	t _{SINH}	—	2/8 t _{CY}	—	—	ns
INT Invalid Time	t _{IINH}	—	1/8 t _{CY}	—	—	ns

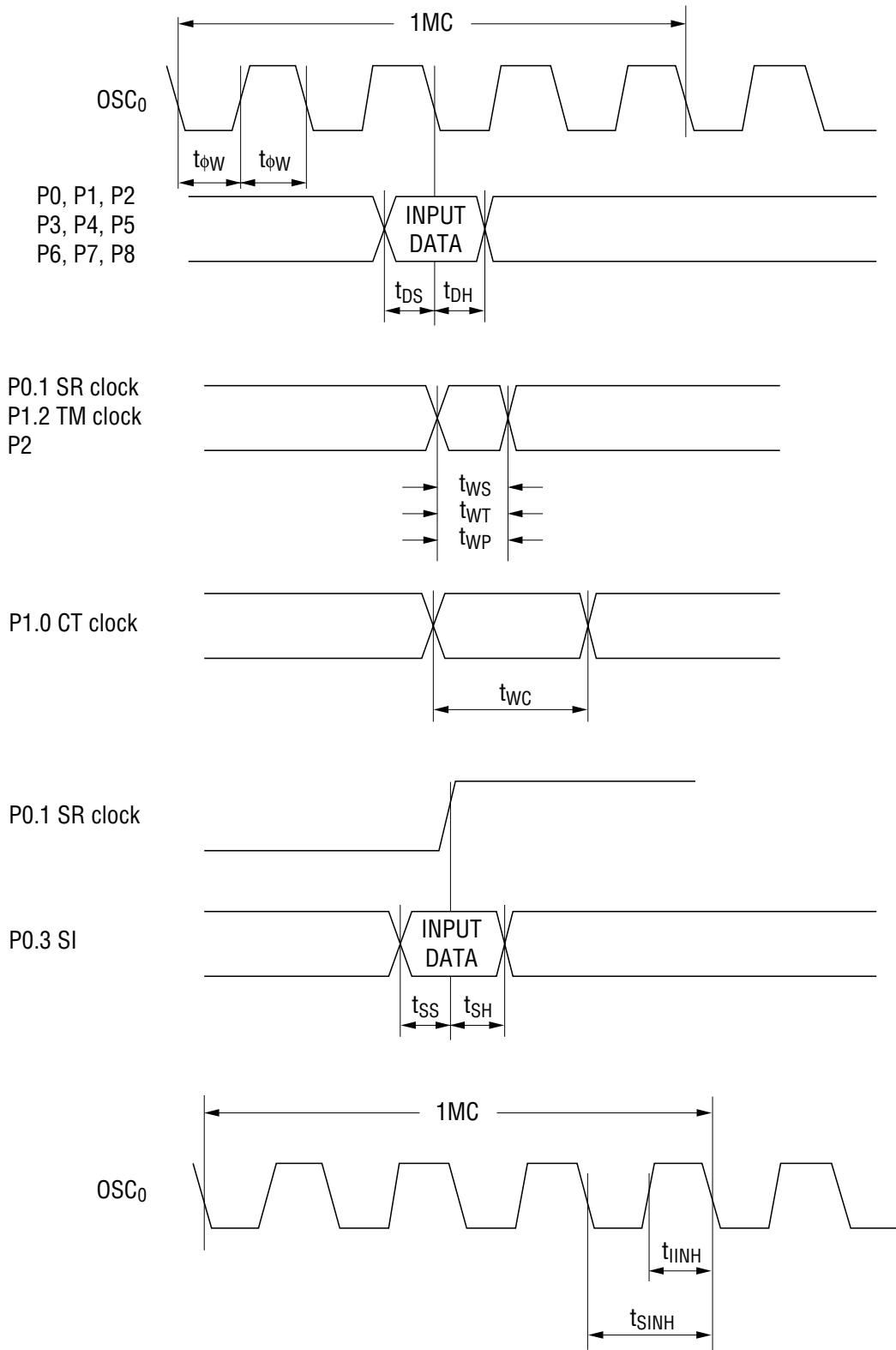
Timing Diagrams (MSM6404A)

Output Conditions



* Output data to port is clock for SR, TM or CT.

Input Conditions

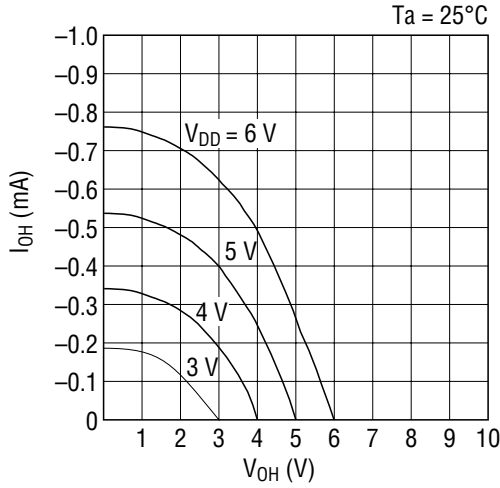


t_{SINH} : P0.1 (SR clock) INH period during LMSR INST.
 (Note : P0.1 is used for clock of SR.)

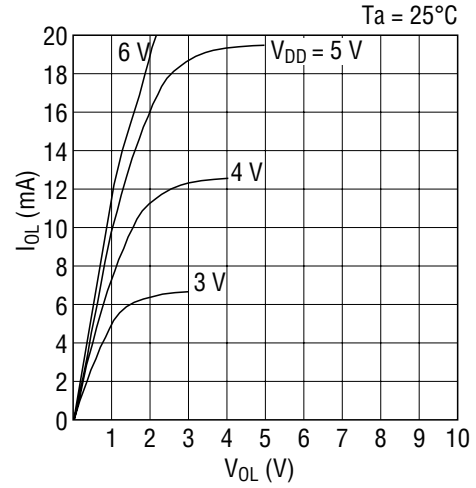
t_{IINH} : P2.0 (interrupt) INH period during RPB and RPBD INST.

Operating Characteristics (MSM6404A)

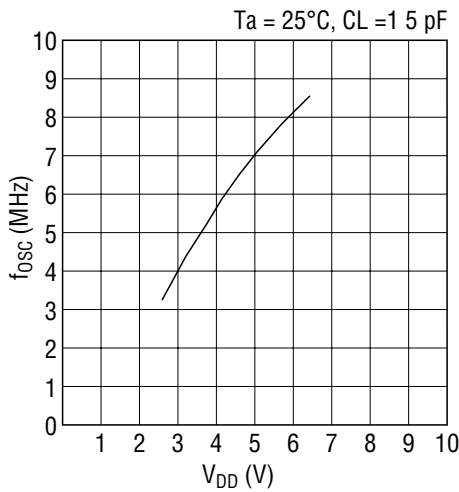
Current (I_{OH}) vs Voltage (V_{OH}) for High State Output



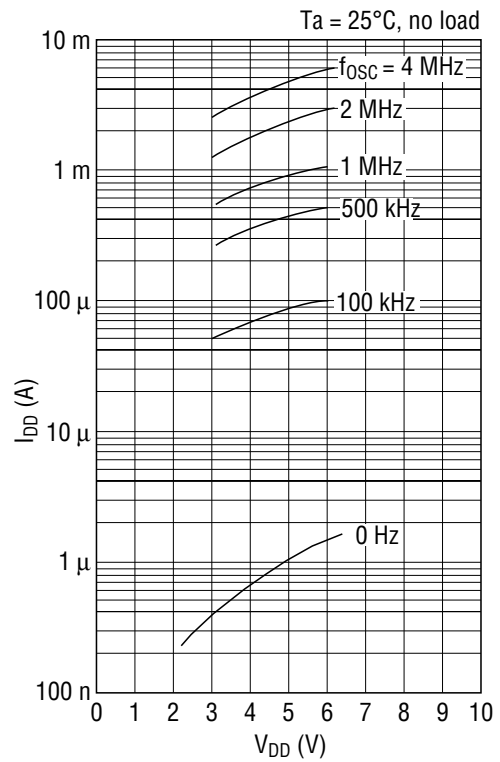
Current (I_{OL}) vs Voltage (V_{OL}) for Low State Output



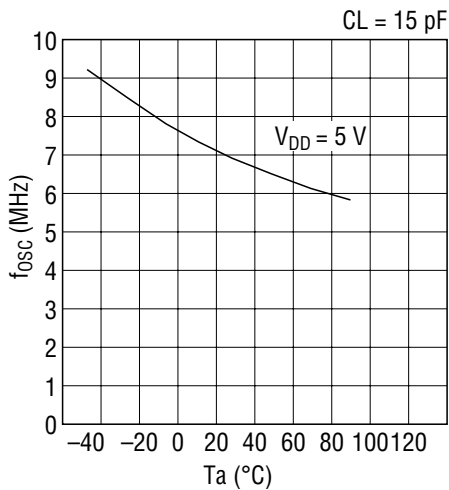
Maximum Clock Frequency (f_{OSC}) vs Supply Voltage (V_{DD})



Supply Current (I_{DD}) vs Supply Voltage (V_{DD})



Maximum Clock Frequency (f_{OSC}) vs Temperature (T_a)



ABSOLUTE MAXIMUM RATINGS (MSM6404VS)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to +7	V
Input Voltage	V_I		-0.3 to V_{DD}	V
Output Voltage	V_O		-0.3 to V_{DD}	V
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$ per package	200 max.	mW
		$T_a = 25^\circ\text{C}$ per output	50 max.	mW
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS (MSM6404VS)

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	$f_{OSC} \leq 1 \text{ MHz}$	3 to 6	V
		$f_{OSC} \leq 4.2 \text{ MHz}$	4.75 to 5.25	V
Data-Hold Voltage	V_{DDH}	$f_{OSC} = 0 \text{ Hz}$	2 to 6	V
Operating Temperature	T_{op}	—	0 to +40	$^\circ\text{C}$
Fan Out	N	MOS load	15	—
		LSTTL load	1	

ELECTRICAL CHARACTERISTICS (MSM6404VS)

DC Characteristics

(V_{DD} = 5 V ±5%, T_a = 0 to +40°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage*1, *2	V _{IH}	—	3.6	—	V _{DD}	V
"H" Input Voltage*3, *4	V _{IH}	—	3.6	—	V _{DD}	V
"L" Input Voltage	V _{IL}	—	-0.3	—	+0.8	V
"H" Output Voltage*1, *5	V _{OH}	I _O = -15 μA	4.2	—	—	V
"L" Output Voltage*1	V _{OL}	I _O = 0.4 mA	—	—	0.4	V
"L" Output Voltage*5	V _{OL}	I _O = 15 μA	—	—	0.4	V
Input Current*3	I _{IH} /I _{IL}	V _I = V _{DD} /0 V	—	—	15/-15	μA
Input Current*2, *4	I _{IH} /I _{IL}	V _I = V _{DD} /0 V	—	—	1/-30	μA
"H" Output Current*1	I _{OH}	V _O = 2.4 V	-0.1	—	—	mA
"H" Output Current*1	I _{OH}	V _O = 0.4 V	—	—	-1.2	mA
Input Capacitance	C _I	f = 1 MHz, T _a = 25°C	—	5	—	pF
Output Capacitance	C _O		—	7	—	
Power Supply Current*6 (In Stop Mode)	I _{DD} S	V _{DD} = 2 V, no load, T _a = 25°C	—	1	5	μA
		No load	—	10	100	μA
Power Supply Current*6	I _{DD}	Crystal oscillation f = 4.2 MHz, no load	—	6	12	mA

*1 Applied to P0, P1, P3, P4, P5, P6, P7 and P8.

*2 Applied to P2.

*3 Applied to OSC₀.*4 Applied to $\overline{\text{RESET}}$.*5 Applied to $\overline{\text{OSC}}_1$.

*6 The EPROM current is not included.

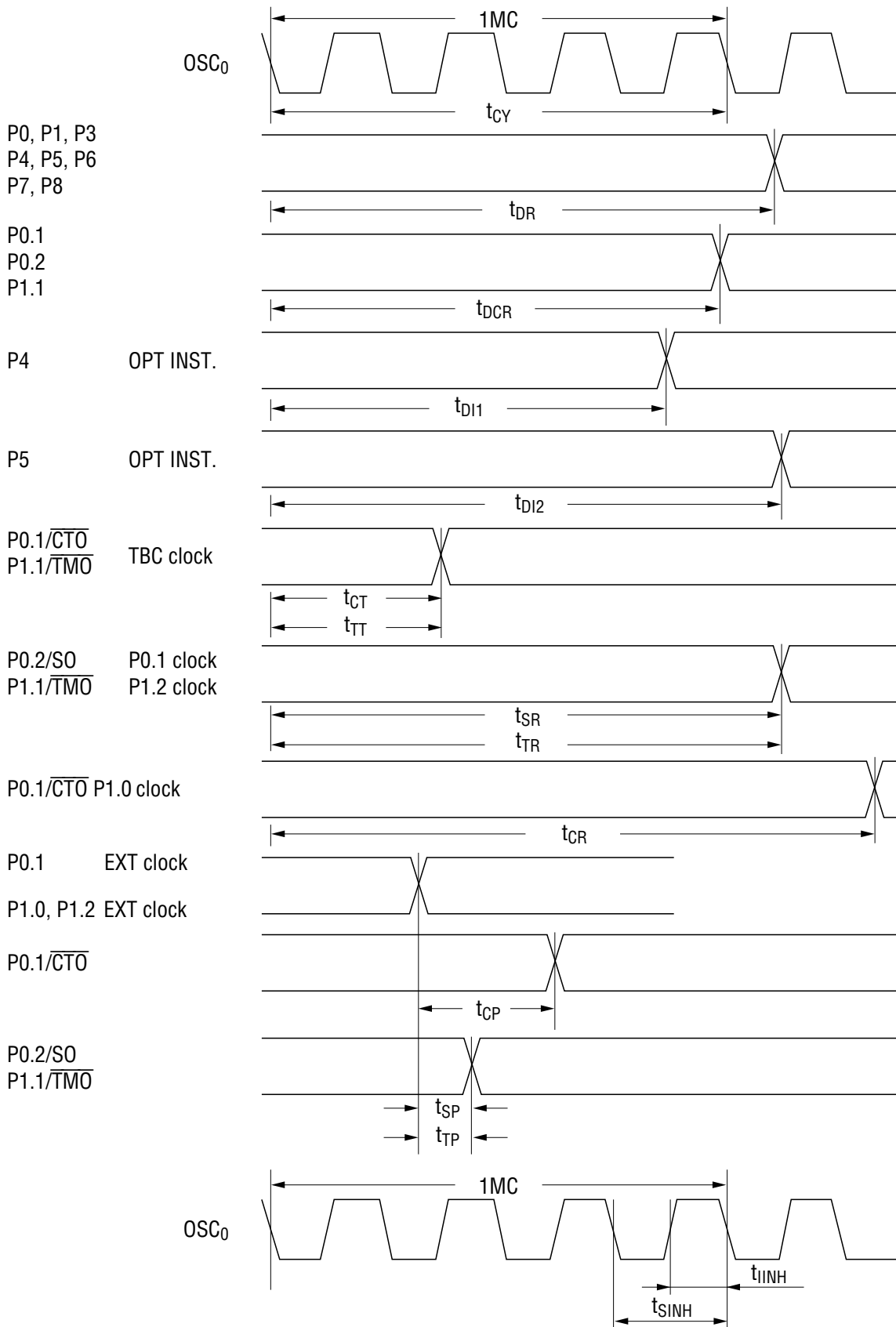
AC Characteristics (MSM6404VS)

(V_{DD} = 5 V ±5%, Ta = 0 to +40°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (OSC ₀) Pulse Width	t _{φW}	—	119	—	—	ns
Cycle Time	t _{CY}	—	952	—	—	ns
Input Data Setup Time	t _{DS}	—	120	—	—	ns
Input Data Hold Time	t _{DH}	—	120	—	—	ns
SR/TM Clock Pulse Width	t _{WS} /t _{WT}	—	120	—	—	ns
CT Clock Pulse Width	t _{WC}	—	2/8 t _{CY} + 120	—	—	ns
P2 Input Data Clock Pulse Width	t _{WP}	—	120	—	—	ns
SR Data Setup Time	t _{SS}	—	120	—	—	ns
SR Data Hold Time	t _{SH}	—	120	—	—	ns
Data Delay Time	t _{DR}	C _L = 15 pF	—	—	t _{CY} + 300	ns
Data Delay Time at Mode Switching	t _{DCR}	C _L = 15 pF	—	—	7/8 t _{CY} + 300	ns
Data Delay Time at OPT Instruction	t _{DI1}	C _L = 15 pF	—	—	6/8 t _{CY} + 300	ns
Data Delay Time at OPT Instruction	t _{DI2}	C _L = 15 pF	—	—	7/8 t _{CY} + 300	ns
CT/TM Data Delay Time Using TBC Clock	t _{CT} /t _{TT}	C _L = 15 pF	—	—	2/8 t _{CY} + 360	ns
SR/TM Data Delay Time Using PORT Clock	t _{SR} /t _{TR}	C _L = 15 pF	—	—	t _{CY} + 480	ns
CT Data Delay Time Using PORT Clock	t _{CR}	C _L = 15 pF	—	—	10/8 t _{CY} + 480	ns
CT Data Delay Time Using External Clock	t _{CP}	C _L = 15 pF	—	—	2/8 t _{CY} + 360	ns
SR/TM Data Delay Time Using External Clock	t _{SP} /t _{TP}	C _L = 15 pF	—	—	360	ns
SR Clock Invalid Time	t _{SINH}	—	2/8 t _{CY}	—	—	ns
INT Invalid Time	t _{IINH}	—	1/8 t _{CY}	—	—	ns

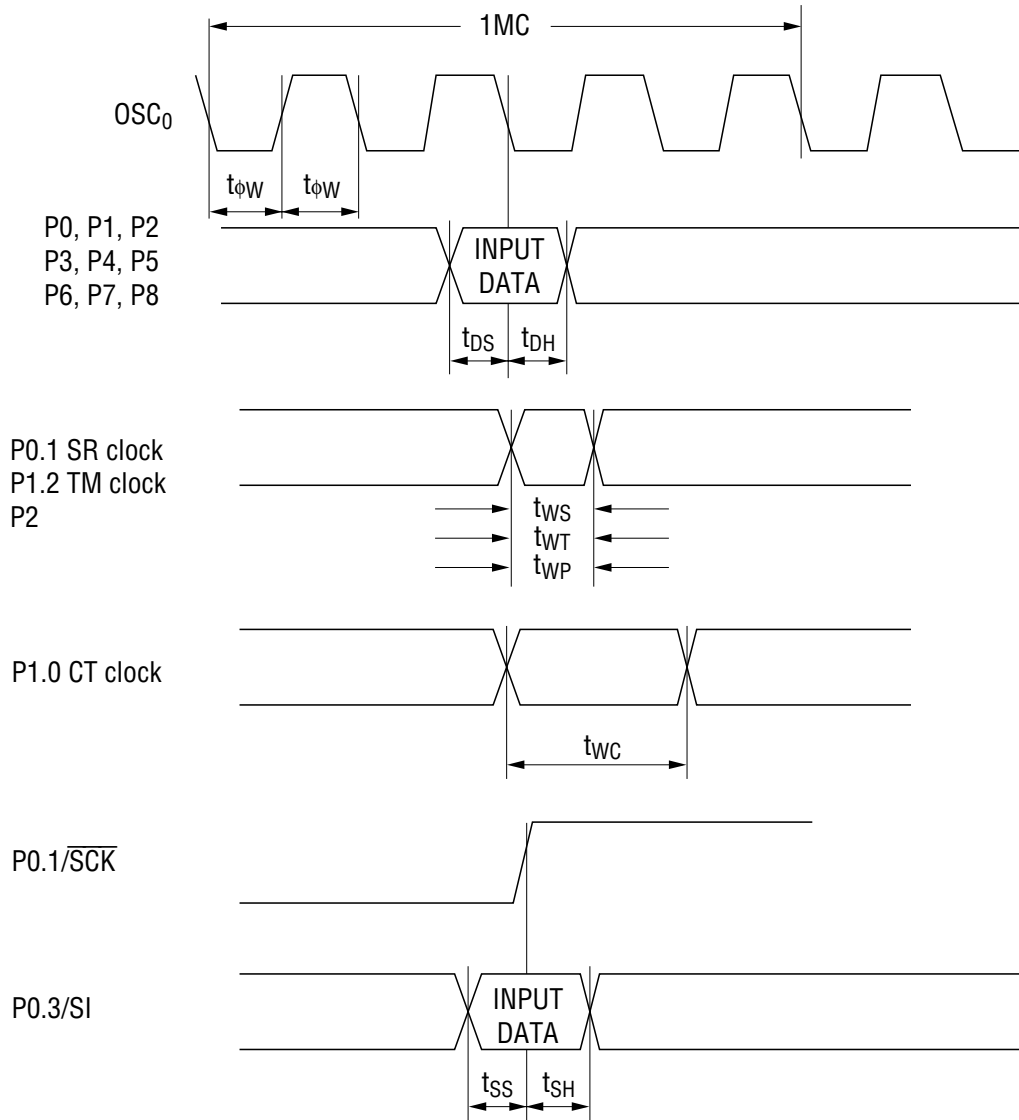
Timing Diagrams (MSM6404VS)

Output Conditions



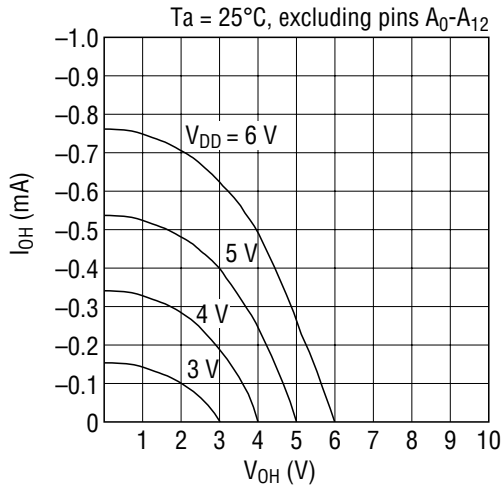
t_{SINH} : P0.1/ \overline{SCK} inhibit period during LMSR INST.
 t_{IINH} : P2.0/ \overline{INT} inhibit period during RPB and RPBD INST.

Input Conditions

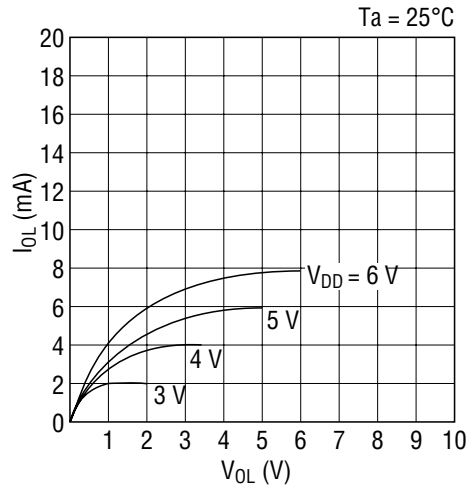


Operating Characteristics (MSM6404VS)

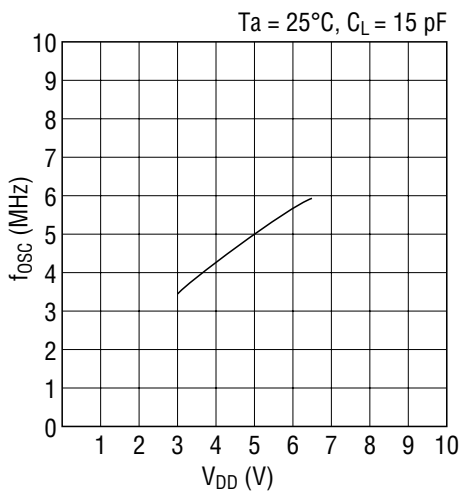
Current (I_{OH}) vs Voltage (V_{OH}) for High State Output



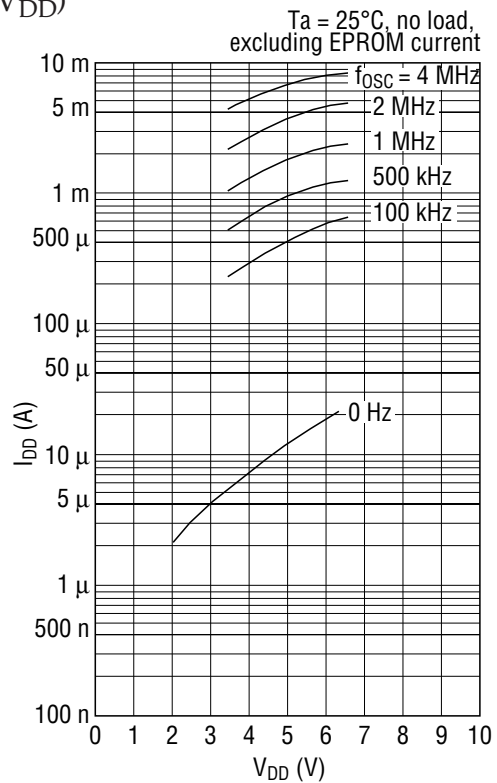
Current (I_{OL}) vs Voltage (V_{OL}) for Low State Output



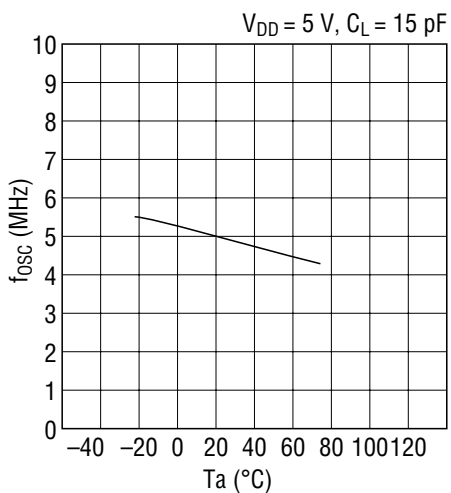
Maximum Clock Frequency (f_{OSC}) vs Supply Voltage (V_{DD})



Supply Current (I_{DD}) vs Supply Voltage (V_{DD})



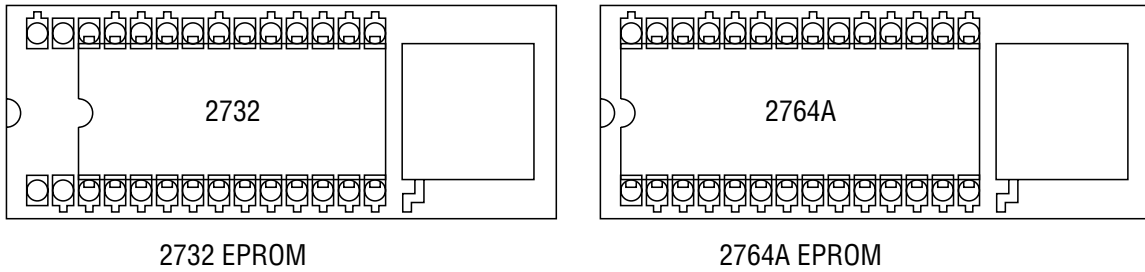
Maximum Clock Frequency (f_{OSC}) vs Temperature (T_a)



FUNCTIONAL DESCRIPTION

MSM6404VS Interface to EPROM

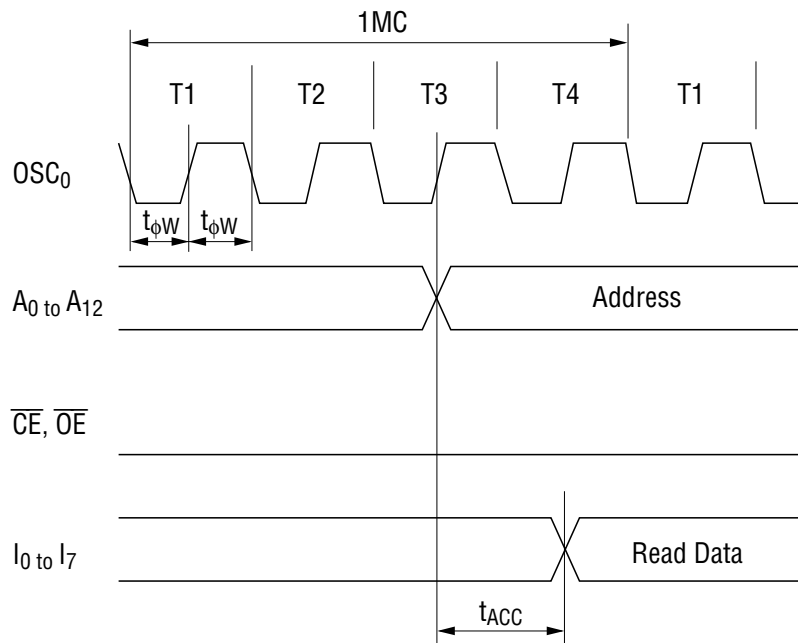
EPROM insertion method



2732 EPROM

2764A EPROM

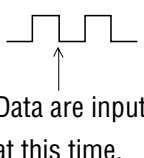
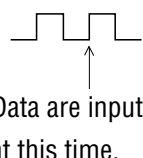
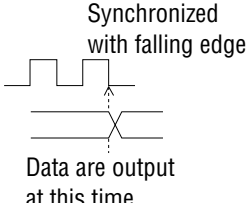
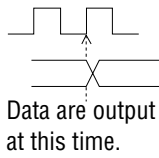
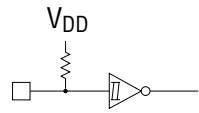
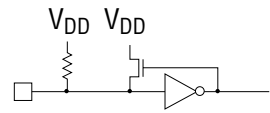
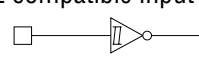
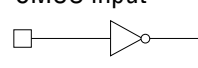
EPROM read timing



Use EPROM with t_{ACC} of less than 357 ns.

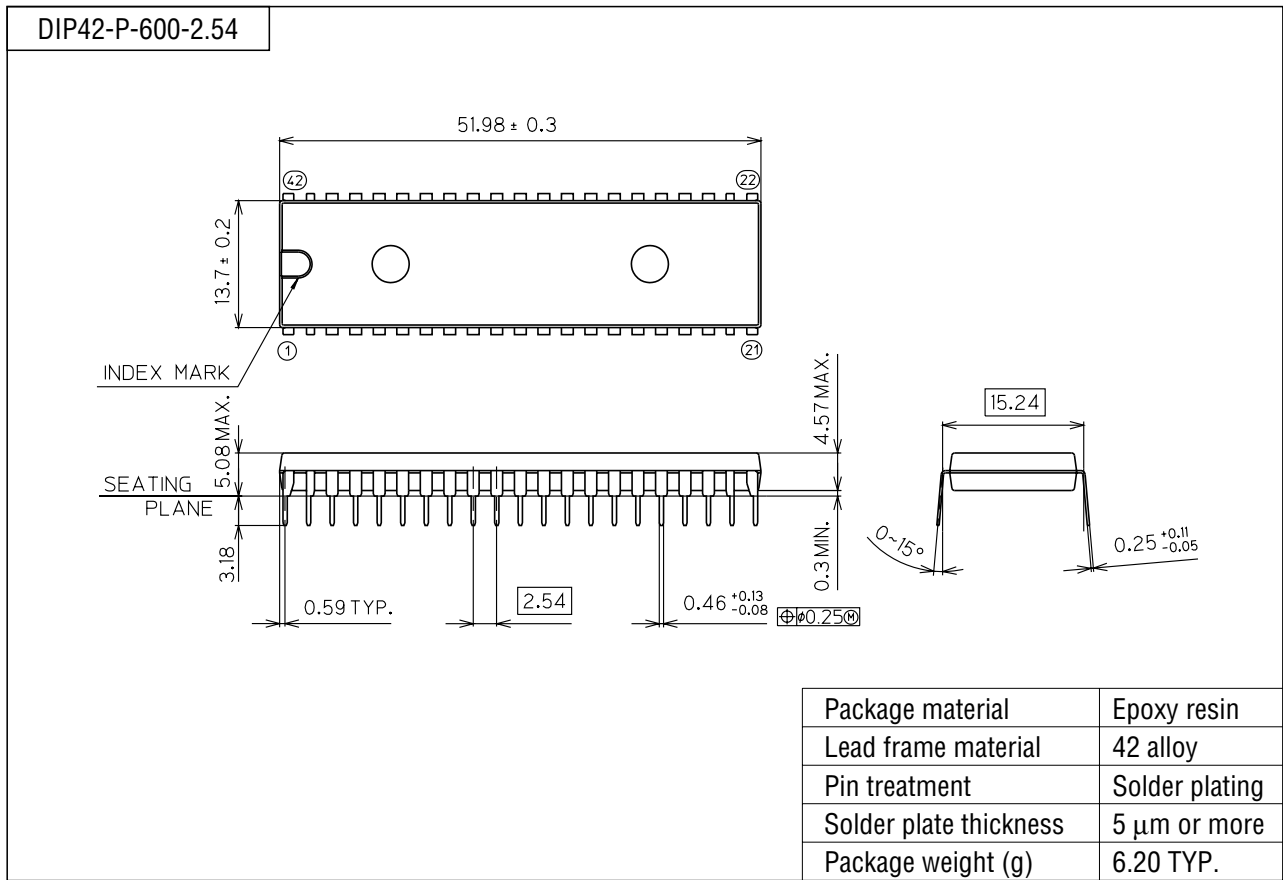
Read data is read into the instruction register in the first half of the T1 state.

Differences between MSM6404A and MSM6404VS (PIGGYBACK)

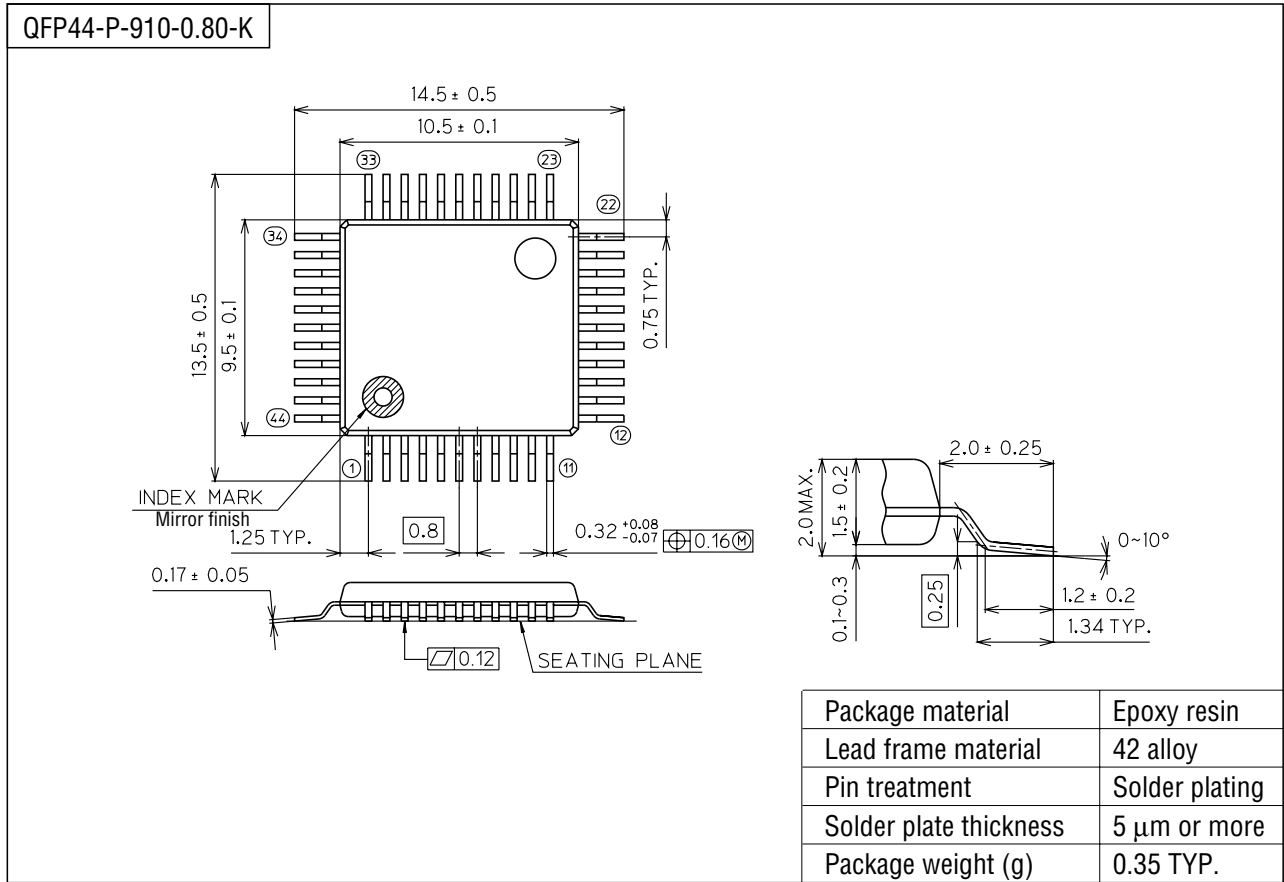
Item	MSM6404A	MSM6404VS (Piggyback)
1. Port initialization during reset	Ports P0, 1, 3 are set to "1" and ports P2, 4, 5, 6, 7, 8 are reset to "0" directly by the reset input signal.	Ports P0, 1, 3 are set to "1" and ports P2, 4, 5, 6, 7, 8 are initialized during reset cycle.
2. Timer operation	After being reset, the timer continues to stop until data is set in it.	It is undefined whether the timer starts or not after being reset. Therefore, the timer should be initialized by software.
3. Shift register	Serial out F/F (SOF/F) is set to "0" after being reset.	It is undefined whether serial out F/F (SOF/F) is "0" or "1" after being reset. Therefore the serial out F/F should be initialized by software.
4. Port input/output timing	Internal clock  Input Data are input at this time.	Internal clock  Input Data are input at this time.
	Internal clock  Output Synchronized with falling edge Data are output at this time.	Internal clock  Output Data are output at this time.
5. Port input/output characteristics	TTL FO = "1" ($I_{OL} = 1.6 \text{ mA @ } 0.4 \text{ V}$)	LSTTL FO = "1" ($I_{OL} = 0.4 \text{ mA @ } 0.4 \text{ V}$)
	P2.0-3 	P2.0-3 
	TTL compatible input P0.0-P8.3 (Except P2.0-3) 	CMOS input P0.0-P8.3 (Except P2.0-3) 
6. Available ROM capacity	Up to 4 Kbytes	Up to 8 Kbytes accessible
7. LJP a ₁₃ , LCAL a ₁₃ instruction	Not available	Available

PACKAGE DIMENSIONS

(Unit : mm)



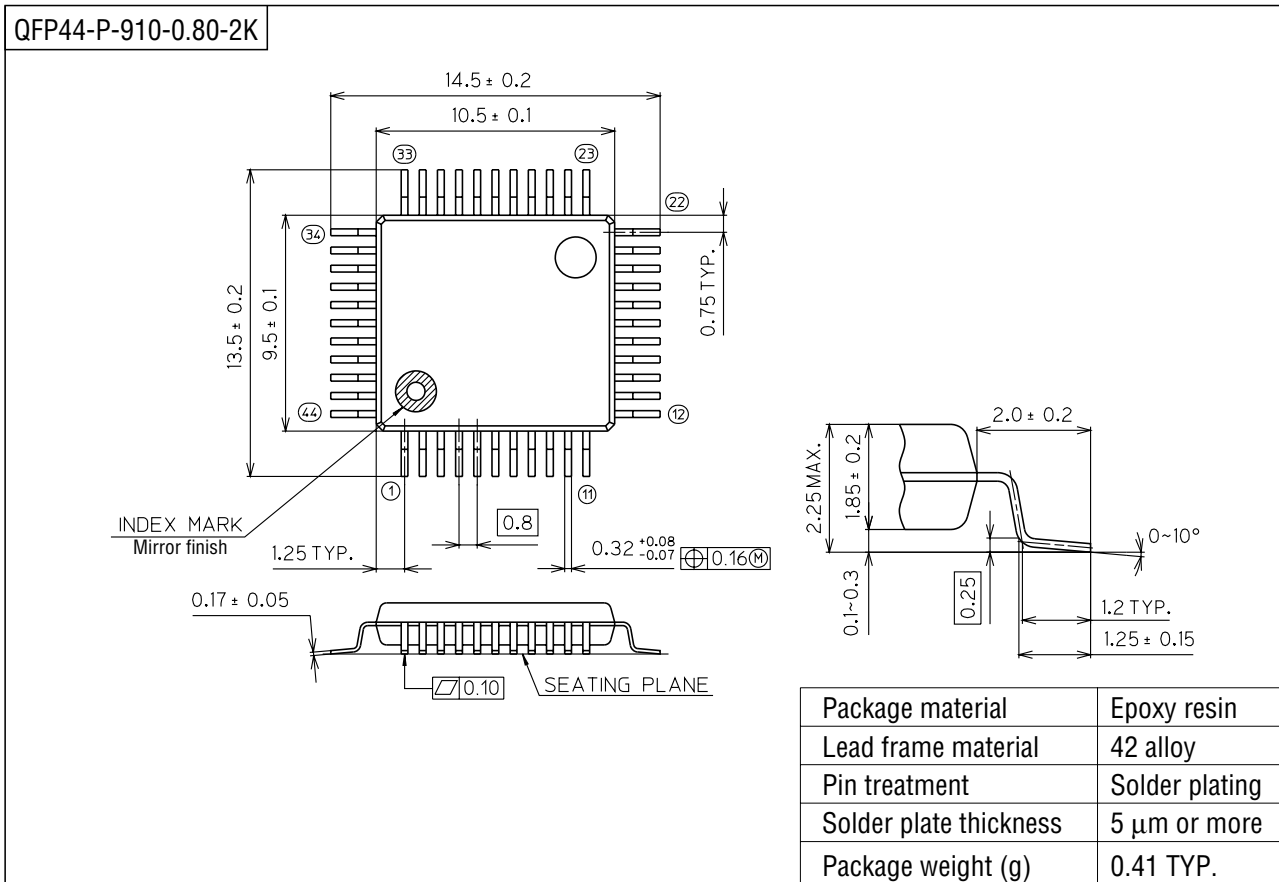
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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