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**MSM6599B**

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**80-DOT SEGMENT DRIVER**

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**GENERAL DESCRIPTION**

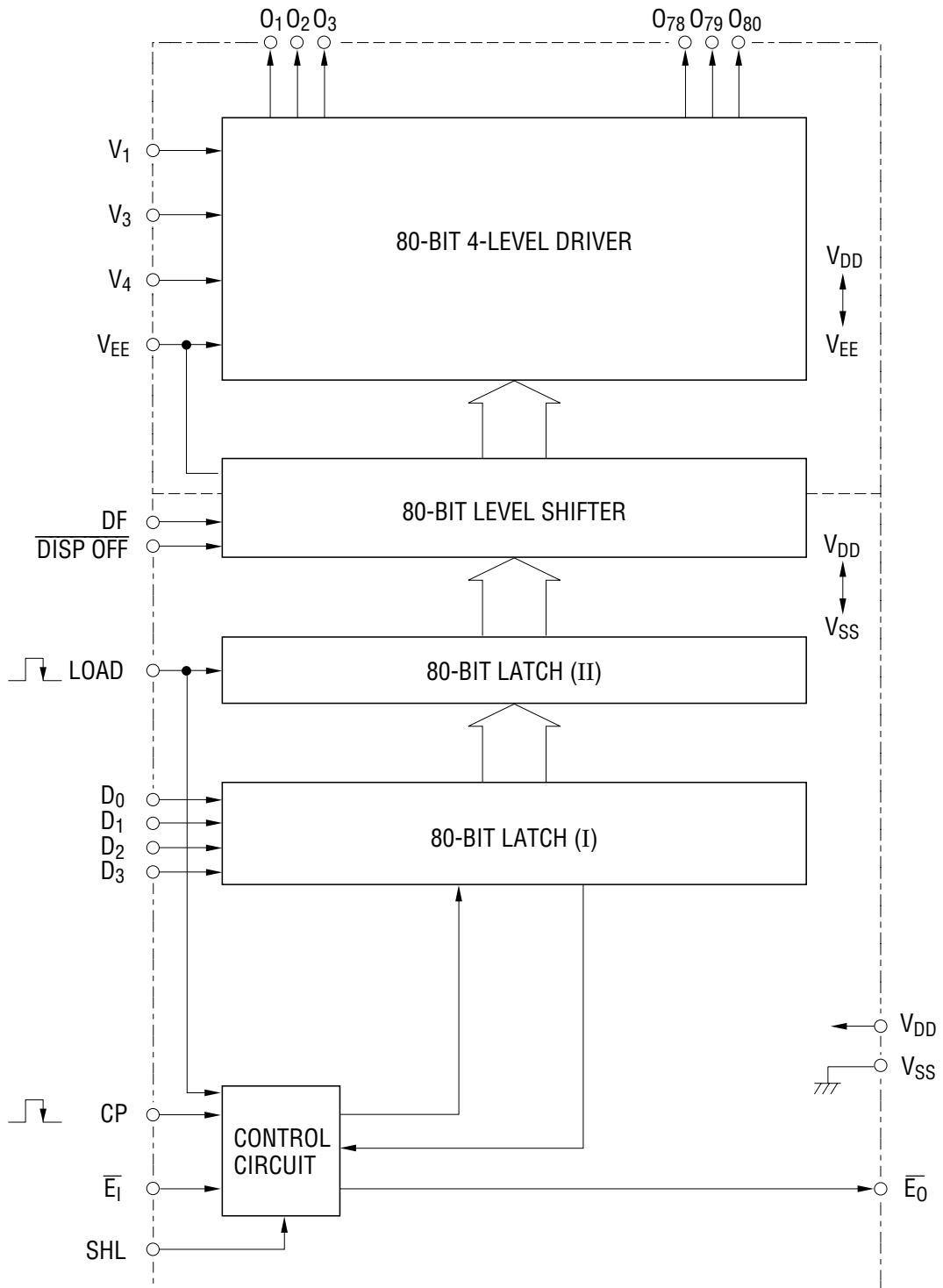
The MSM6599B is a dot matrix LCD segment driver LSI which consists of two 80-bit latches, an 80-bit level shifter and an 80-bit 4-level driver.

It latches the 4-bit parallel display data transferred from a microcomputer or LCD controller LSI, then outputs the LCD driving waveform to the LCD.

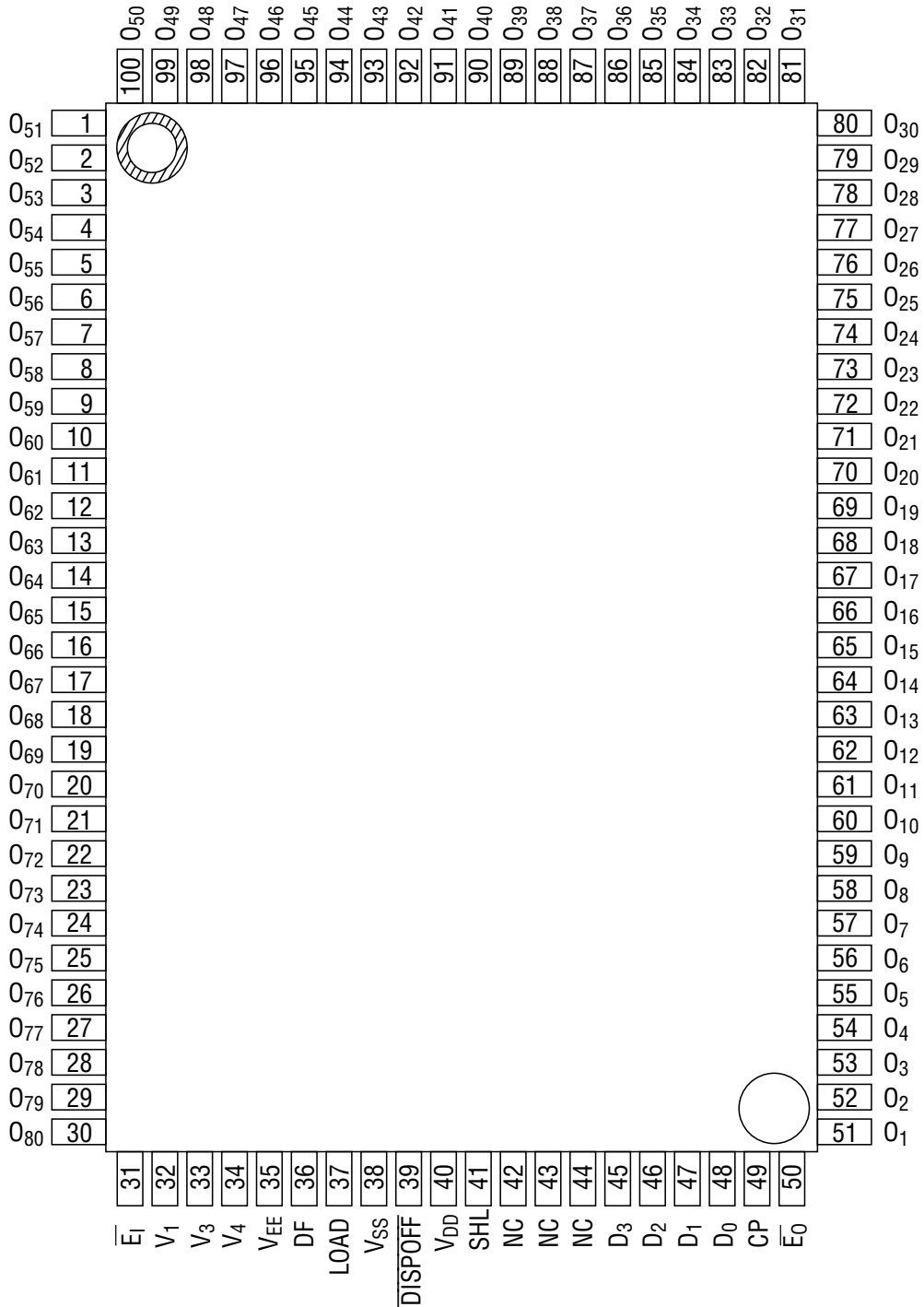
**FEATURES**

- Supply voltage : 4.5 to 5.5 V
- LCD driving voltage : 18 to 28 V
- Applicable LCD duty : 1/64 to 1/256
- LCD output : 80
- Because of 4-bit parallel transfers, the transfer speed is 1/4 that of conventional serial transfer, insuring low power consumption.
- Applicable common driver : MSM6698 (80 outputs)
- Package options:
  - 100-pin plastic QFP (QFP100-P-1420-0.65-K) (Product name : MSM6599B GS-K)
  - 100-pin plastic QFP(QFP100-P-1420-0.65-BK) (Product name : MSM6599B GS-BK)

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



NC : No connection

**100-Pin Plastic QFP**

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	$V_{DD}$	$T_a = 25^\circ\text{C}$	-0.3 to +6.5	V
Supply Voltage (2)	$V_{DD} - V_{EE}$ *1	$T_a = 25^\circ\text{C}$	0 to 32	V
Input Voltage	$V_I$	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-55 to +150	$^\circ\text{C}$

\*1  $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	$V_{DD}$	—	4.5 to 5.5	V
Supply Voltage (2)	$V_{DD} - V_{EE}$ *1	—	18 to 28	V
Operating Temperature	$T_{op}$	—	-20 to +75	$^\circ\text{C}$

\*1  $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

( $V_{DD} = 5V \pm 10\%$ ,  $T_a = -20$  to  $+75^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	$V_{IH}^{*1}$	—	$0.7V_{DD}$	—	$V_{DD}$	V
"L" Input Voltage	$V_{IL}^{*1}$	—	$V_{SS}$	—	$0.3V_{DD}$	V
"H" Input Current	$I_{IH}^{*1}$	$V_I = V_{DD}, V_{DD} = 5.5V$	—	—	1	$\mu A$
"L" Input Current	$I_{IL}^{*1}$	$V_I = 0V, V_{DD} = 5.5V$	—	—	-1	$\mu A$
"H" Output Voltage	$V_{OH}^{*2}$	$I_O = -0.2mA, V_{DD} = 4.5V$	$V_{DD}-0.4$	—	—	V
"L" Output Voltage	$V_{OL}^{*2}$	$I_O = 0.2mA, V_{DD} = 4.5V$	—	—	0.4	V
ON Resistance	$R_{ON}^{*4}$	$V_{DD}-V_{EE} = 25V,$ $ V_N - V_O  = 0.25V \quad V_{DD} = 4.5V$ <sup>*3</sup>	—	1.5	3.0	$k\Omega$
Standby Current	$I_{DDSBY}$	$f_{CP} = 6.0 MHz, V_{DD} = 5.5V$ $V_{DD}-V_{EE} = 25V, \text{No load}$ <sup>*5</sup>	—	—	300	$\mu A$
Supply Current (1)	$I_{DD1}$	$f_{CP} = 6.0 MHz, V_{DD} = 5.5V$ $V_{DD}-V_{EE} = 25V, \text{No load}$ <sup>*6</sup>	—	—	1.0 / 1.5	mA
Supply Current (2)	$I_V$	$f_{CP} = 6.0 MHz, V_{DD} = 5.5V$ $V_{DD}-V_{EE} = 25V, \text{No load}$ <sup>*7</sup>	—	—	100	$\mu A$
Input Capacitance	$C_I$	$f = 1 MHz$	—	5	—	$\mu F$

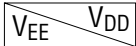
\*1 Applicable to  $\overline{LOAD}, CP, D_0$  to  $D_3, \overline{E_I}, DF, \overline{DISPOFF}, SHL$ .

\*2 Applicable to  $\overline{E_O}$ .

\*3  $V_N = V_1$  to  $V_{EE}$   $V_4 = 14/16 (V_{DD}-V_{EE}), V_3 = 2/16 (V_{DD}-V_{EE}), V_{DD} = V_1$ .

\*4 Applicable to  $O_1$  to  $O_{80}$ .

\*5 Display Data 1010  $f_{DF} = 45 Hz$ , current from  $V_{DD}$  to  $V_{SS}$  when the display data is not being processed.

\*6 Display Data 1010  $f_{DF} = 45 Hz$ , current ( $V_{DD}$  side current) from  $V_{DD}$  to  $V_{SS}$  and  $V_{EE}$ , and current ( $V_{EE}$  side current) from  $V_{DD}$  to  $V_{EE}$  when the display data is being processed. 

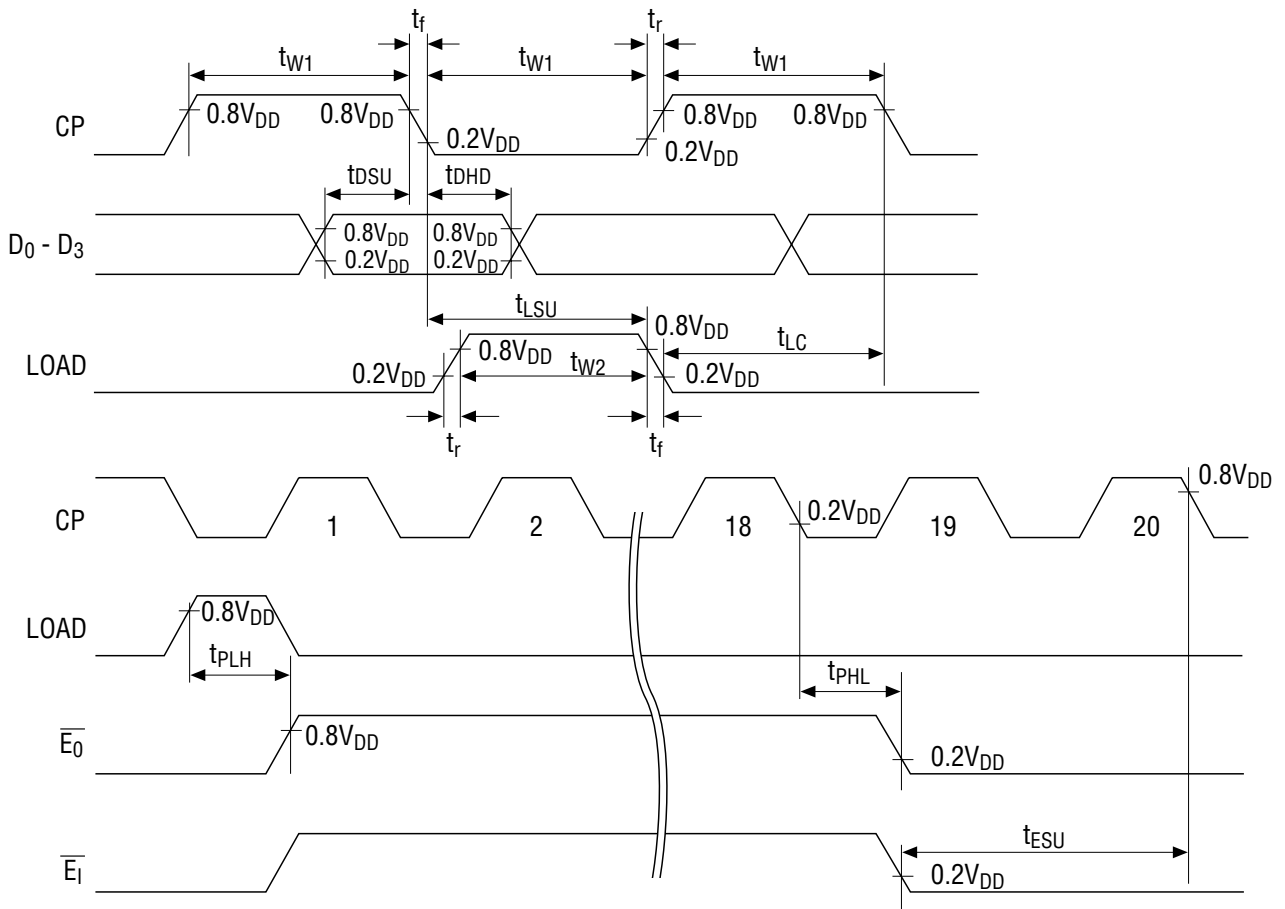
\*7 Display Data 1010  $f_{DF} = 45 Hz, f_{LOAD} = 20 kHz$ , current on  $V_1, V_3$  and  $V_4$ .

Switching Characteristics

( $V_{DD} = 5V \pm 10\%$ .  $T_a = -20$  to  $+75^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	$f_{CP}$	DUTY = 50%	—	—	6.5	MHz
Clock Pulse Width	$t_{W1}$	—	56	—	—	ns
Load Pulse Width	$t_{W2}$	—	70	—	—	ns
Rise/Fall Time	$t_r, t_f$	—	—	—	20	ns
Data Setup Time	$t_{DSU}$	—	50	—	—	ns
Data Hold Time	$t_{DHD}$	—	50	—	—	ns
Load Setup Time	$t_{LSU}$	—	80	—	—	ns
Load-to-Clock Time	$t_{LC}$	—	80	—	—	ns
Propagation Delay Time	$t_{PLH}, t_{PHL}$	$CL=15pF$	—	—	236	ns
$\bar{E}_I$ Setup Time	$t_{ESU}$	—	50	—	—	ns

Note: When display control by the  $\overline{DISPOFF}$  pin is performed, the rise and fall time must be  $\leq 1\mu s$ .



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- **$\overline{E_I}, \overline{E_O}$**   
These are enable pins. When a cascade connection is required, set the first MSM6599B's  $\overline{E_I}$  pin at "L" level and connect  $\overline{E_O}$  pin to the next MSM6599B's  $\overline{E_I}$  pin. When a single MSM6599B is used,  $\overline{E_I}$  should be set at "L" level.
- **CP**  
Clock input pin for display data input. Data is clocked in the latch (I) at the falling edge of the clock pulse. The clock pulse from this pin is active when the enable F/F is set, and inactive when it is not set.
- **LOAD**  
Input pin to latch the display data of one line stored in the latch (I). The latch (I) data is transferred to the latch (II) at the falling edge. At this time, the control circuit to save the power is reset and the display data of the next line can be stored.
- **DF**  
Synchronous signal input pin for alternate signal for LCD driving. Frame inversion signal is input to this pin.
- **V<sub>DD</sub>, V<sub>SS</sub>**  
Power supply pins of the MSM6599B. V<sub>DD</sub> is generally set to 4.5V to 5.5V. V<sub>SS</sub> is the GND pin, which is set to 0V.

- **D<sub>0</sub>, D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>**

Display data input pins for the 80-bit latch (I). The display data is input at the falling edge of clock pulse. Table 1 shows the relationship between display data, DF, LCD driver output, and display.

**Table 1**


Display Data	DF	LCD Driver Output	Display
L	L	Non-select level (V <sub>3</sub> )	OFF
H	L	Select level (V <sub>1</sub> )	ON
L	H	Non-select level (V <sub>4</sub> )	OFF
H	H	Select level (V <sub>EE</sub> )	ON


- **SHL**

Input pin to select the loading direction of display data. Set this pin to "H" or "L" level during power-on. Table 2 shows the relationship between shift direction of data (D<sub>0</sub> to D<sub>3</sub>) and driver output (O<sub>1</sub> to O<sub>80</sub>).

**Table 2**

SHL	Direction of Data Loading
L	D <sub>0</sub> → O <sub>1</sub> → O <sub>5</sub> ----- → O <sub>77</sub>
	D <sub>1</sub> → O <sub>2</sub> → O <sub>6</sub> ----- → O <sub>78</sub>
	D <sub>2</sub> → O <sub>3</sub> → O <sub>7</sub> ----- → O <sub>79</sub>
	D <sub>3</sub> → O <sub>4</sub> → O <sub>8</sub> ----- → O <sub>80</sub>
H	D <sub>0</sub> → O <sub>80</sub> → O <sub>76</sub> ----- → O <sub>4</sub>
	D <sub>1</sub> → O <sub>79</sub> → O <sub>75</sub> ----- → O <sub>3</sub>
	D <sub>2</sub> → O <sub>78</sub> → O <sub>74</sub> ----- → O <sub>2</sub>
	D <sub>3</sub> → O <sub>77</sub> → O <sub>73</sub> ----- → O <sub>1</sub>

  
 Last Data

  
 First Data



- V<sub>1</sub>, V<sub>3</sub>, V<sub>4</sub>, V<sub>EE</sub>**  
 Bias supply voltage pins used to drive the LCD. Use an external bias voltage supply for driving the LCD
- O<sub>1</sub> - O<sub>80</sub>**  
 Output pins for the 4-level driver that directly correspond to each bit of the 80-bit latch (II) contents. One of V<sub>1</sub>, V<sub>3</sub>, V<sub>4</sub> and V<sub>EE</sub> is selected and output by a combination of latched content and DF signals. See the "Truth Table". Connect this output to the segment side of the LCD.
- DISP OFF**  
 Input pin to control O<sub>1</sub> to O<sub>80</sub> outputs. The V<sub>1</sub> level is output from O<sub>1</sub> to O<sub>80</sub> pins regardless of the display data during "L" level input. See the "Truth Table".

**Truth Table**

DF	Latch Data	<u>DISPOFF</u>	Driver Output (O <sub>1</sub> to O <sub>80</sub> )
L	L	H	V <sub>3</sub>
L	H	H	V <sub>1</sub>
H	L	H	V <sub>4</sub>
H	H	H	V <sub>EE</sub>
X	X	L	V <sub>1</sub>

X : Don't Care

**NOTES ON USE**

Precautions when turning power ON/OFF:

The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC.

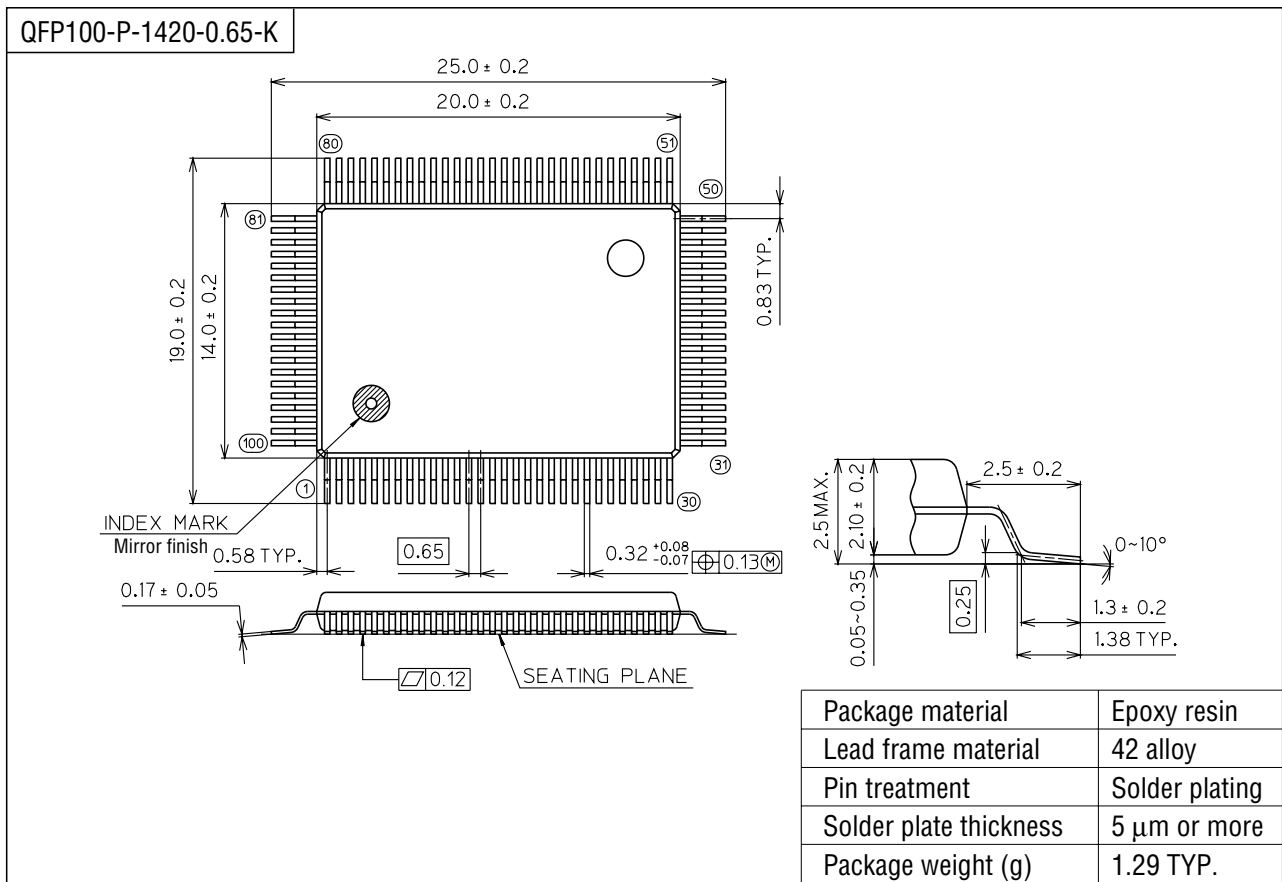
Be sure to follow the sequence below when turning the power ON or OFF.

Power ON : Logic circuits ON → LCD drivers ON, or both ON at a time

Power OFF : LCD drivers OFF → logic circuits OFF, or both OFF at a time

PACKAGE DIMENSIONS

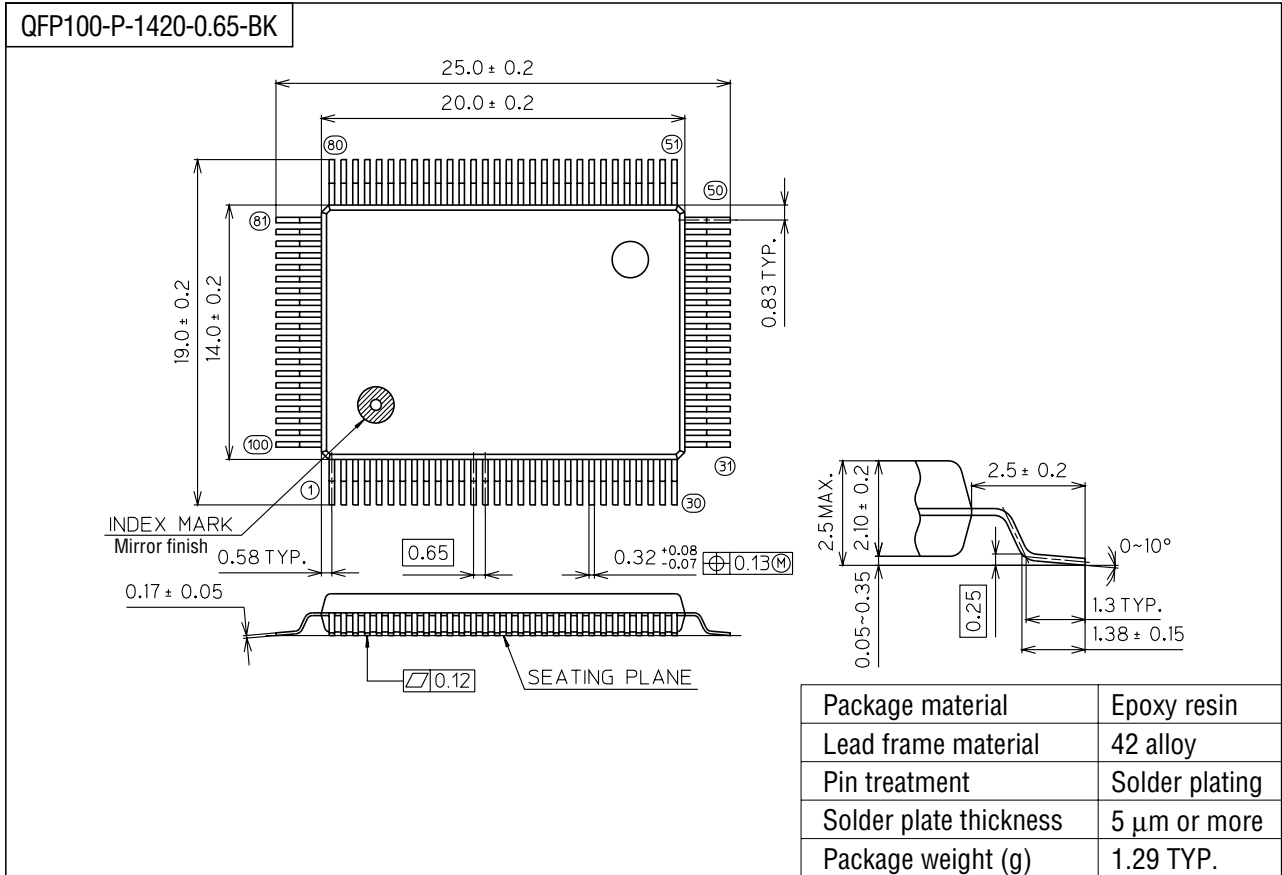
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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