OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65X227

8-Bit Microcontroller (with 4K-Byte EEPROM)

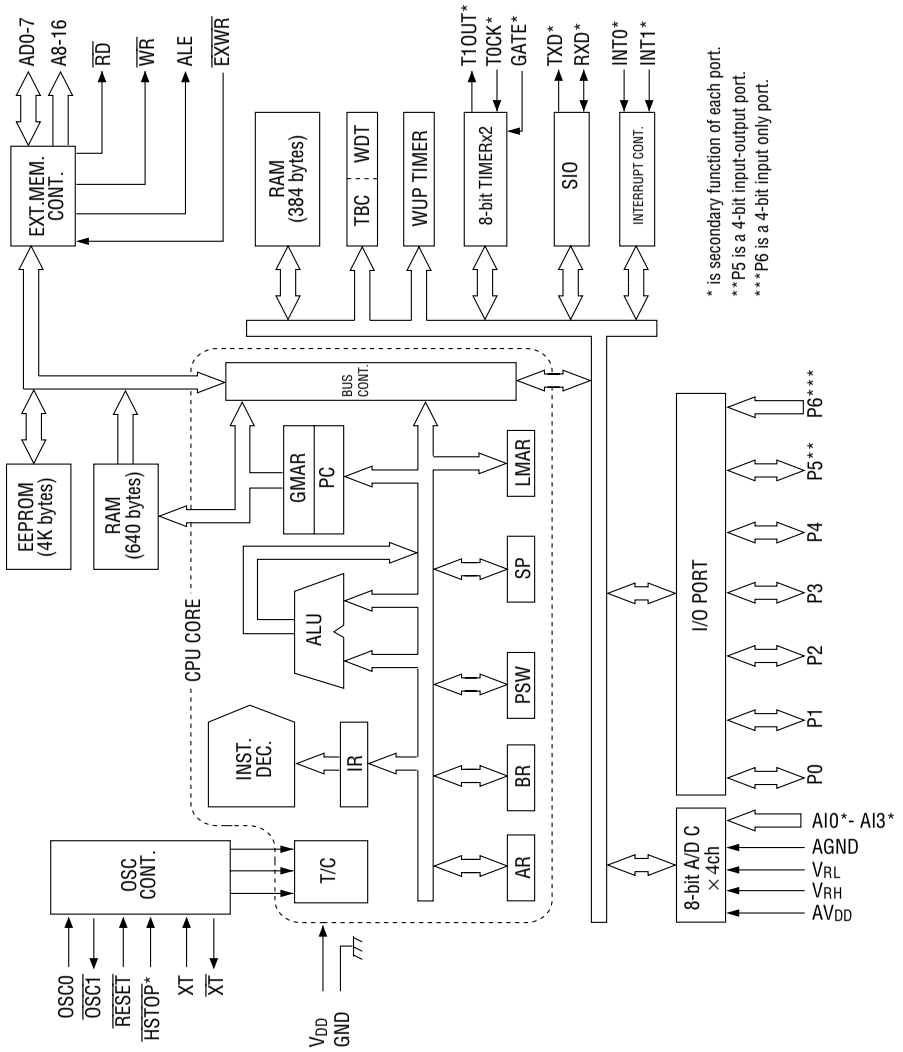
GENERAL DESCRIPTION

The MSM65X227 is a high-performance, 8-bit microcontroller that employs OKI original CPU core, the nX-8/50. The MSM65X227 includes a minimum instruction execution time of 667 ns (@6 MHz) that enables high-speed processing. It has 60K-byte program memory space, internal 4K bytes of EEPROM (general memory space), 1K-byte data memory (384 bytes for local memory space and 640 bytes for general memory space), a timer, a serial port and an A/D converter. The MSM65X227, which has no internal program ROM, is provided with the special time-division data/address bus that can be connected to an extrernal program ROM.

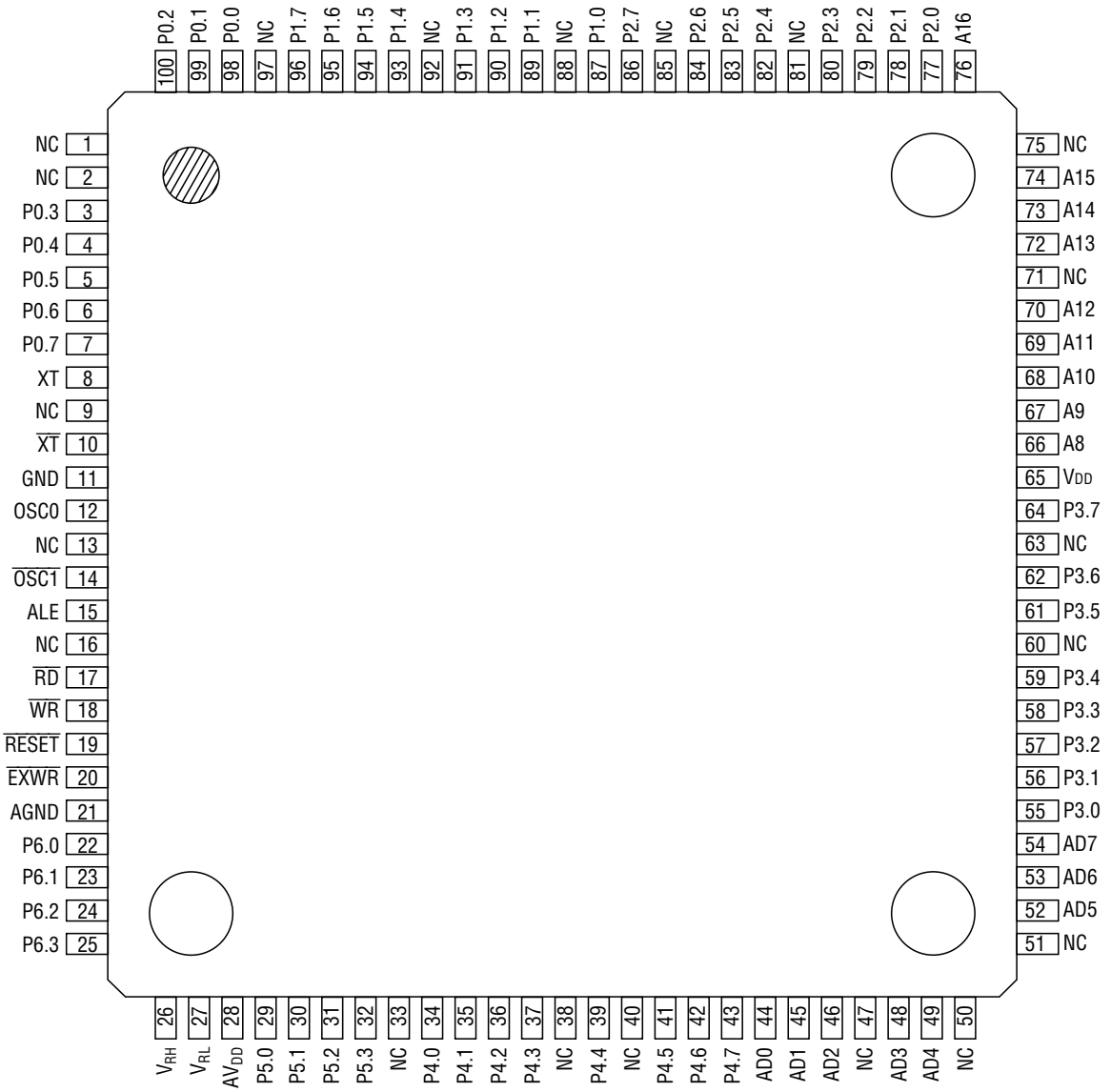
FEATURES

- Operating range
  - Operating frequency : 0 to 6MHz
  - Operating voltage : 4.5 to 5.5V
  - Operating temperature : – 40 to +85°C
- Memory space : 128K bytes
  - Program memory space : 60K bytes
  - Internal EEPROM : 4K bytes
  - Internal data memory : 1K bytes
- Minimum instruction execution time : 667ns @ 6MHz
- Ample instruction set : 81 basic instructions
  - 8/16-bit operation instructions
  - Bit manipulation instructions
  - Complex function instructions
- Ample addressing modes
- Timer : 8-bit auto-reload timer × 2 (one is shared with the baud rate generator)
  - Watchdog timer × 1
- Counter : Time base counter × 1
- Serial port : Serial port × 1 (UART/clock synchronous system)
- A/D converter : 8 bits × 4 channels
- I/O port : 7 ports, 48 bits
  - Input-output port : 5 ports × 8 bits, 1 port × 4 bits
  - Input-port : 1 port × 4 bits
- External interrupts : 2
- Interrupt sources : 10
- Package:
  - 100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (Product name: MSM65X227TS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection Pin

100-Pin Plastic TQFP

PIN DESCRIPTION

Basic Functions

Function	Symbol	Type	Description
Power Supply	V_{DD}	—	Digital power supply (5V)
	GND	—	Digital ground
	AV_{DD}	—	Analog power supply (5V)
	AGND	—	Analog ground
	V_{RH}	—	Analog reference voltage (5V)
	V_{RL}	—	Analog reference voltage (ground)
Oscillation	OSC0	I	CPU oscillation input pin
	$\overline{OSC1}$	O	CPU oscillation output pin
	XT	I	CPU start-up timer oscillation input pin
	$\overline{XT}$	O	CPU start-up timer oscillation output pin
Control	$\overline{RESET}$	I	System reset input: When this pin goes into the "L" state, the internal state is initialized and the execution of an instruction starts from address 0040H. The input is pulled up to V_{DD} with an internal pull-up resistor.
	$\overline{EXWR}$	I	External write enable pin : Sampled at a system reset and enables external EEPROM write and read during the "L" level.
	$\overline{RD}$	O	Read signal at external memory access: Read cycle in memory is indicated when the signal goes into the "L" level during external memory access.
	$\overline{WR}$	O	Write-signal during external memory access: Write cycle in memory is indicated when the signal goes into the "L" level during external memory access.
	ALE	O	Address latch signal at external memory access: The MSM65X227 uses a time dividing address/data bus. This signal uses the lower 8 bits of the address as a strobe signal to latch the external latch circuit.
	AD0 - AD7	I/O	8-bit address/data bus: Address/data bus performs lower 8-bit address output, instruction fetch or data read/write along with the ALE, $\overline{RD}$ and $\overline{WR}$ pins.
	A8 - A16	O	9-bit address bus: Address bus for the upper 9 bits.

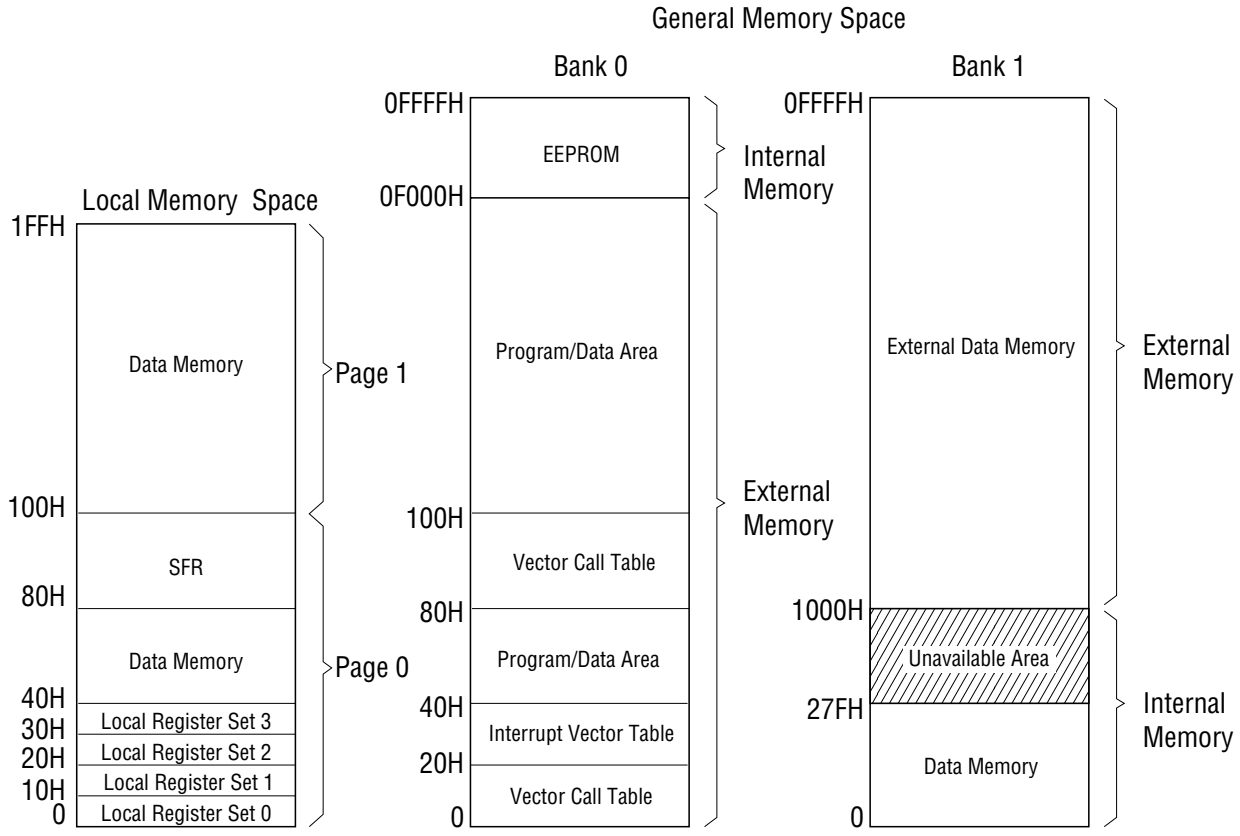
Basic Functions (Continued)

Function	Symbol	Type	Description
Port	P0.0 - P0.7	I/O	8-bit input-output port (Port 0): Users can specify input or output at each bit with the port 0 direction register (P0DIR).
	P1.0 - P1.7	I/O	8-bit input-output port (Port 1): Users can specify input or output at each bit with the port 1 direction register (P1DIR). In the input mode, ports can be set as inputs with a pull-up resistor at each bit. A secondary function shown in the next table is assigned at the P1.7 pin.
	P2.0 - P2.7	I/O	8-bit input-output port (Port 2): Users can specify input or output at each bit by the port 2 direction register (P2DIR). Each pin of Port 2 is assigned a secondary function shown in the next table.
	P3.0 - P3.7	I/O	8-bit input-output port (Port 3): Users can specify input or output at each bit by the port 3 direction register (P3DIR). A secondary function shown in the next table is assigned at the P3.0 pin.
	P4.0 - P4.7	I/O	8-bit input-output port (Port 4): Users can specify input or output at each bit with the port 4 direction register (P4DIR).
	P5.0 - P5.3	I/O	4-bit input-output port (Port 5): Users can specify input or output at each bit with the port 5 direction register (P5DIR).
	P6.0 - P6.3	I	4-bit input port (Port 6): Each pin of Port 6 functions as an analog input channel during A/D conversion.

Secondary Functions

Function	Symbol	Type	Description
External Interrupt	INT0	I	Secondary function of P1.7: Input pin of external interrupt 0. "Receive" is enabled at rising/falling edges or at the "L" level.
	INT1	I	Secondary function of P2.0: Input pin of external interrupt 1. "Receive" is enabled at rising/falling edges or at the "L" level. Can also be used as a gate signal input pin that enables/disables the count of Timer 0.
Control	$\overline{\text{HSTOP}}$	I	Secondary function of P3.0: Hardware stop mode input pin. Changes to hardware stop mode by setting this pin to the "L" level when the HSTP bit of SBYCON is 1. In hardware stop mode, the oscillation of OSC is halted to reduce power consumption.
Timer 0	T0CK	I	Secondary function of P 2.1: External clock input pin of Timer 0.
Timer 1	T1OUT	O	Secondary function of P 2.2: This pin outputs a waveform with a period equal to two times of overflow of Timer 1.
Serial Port	RXD	I/O	Secondary function of P 2.3: As UART: Receive data input pin of asynchronous communication. As clock synchronization: Send/receive data input-output pin of clock synchronous communication.
	TXD	O	Secondary function of P 2.4: As UART: Send data output pin of asynchronous communication. As clock synchronization: Synchronized clock output pin of clock synchronous communication.
A/D Converter	AI0 - AI3	I	Secondary function of P 6.0 to P 6.3: Functions as an analog input channel at A/D conversion.

MEMORY MAPS


General Memory Space
Bank 0
Bank 1
Local Memory Space
0FFFFH
EEPROM
Internal Memory
0F000H
Program/Data Area
External Memory
1FFH
Data Memory
Page 1
100H
Vector Call Table
80H
Program/Data Area
1000H
Unavailable Area
External Memory
SFR
Data Memory
Page 0
40H
Interrupt Vector Table
27FH
Internal Memory
30H
Local Register Set 3
20H
Local Register Set 2
Data Memory
10H
Local Register Set 1
0
Vector Call Table
Local Register Set 0

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}=AV_{DD}	Ta=25°C	–0.3 to 7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Analog Reference Voltage	V_{RH}, V_{RL}	GND=AGND=0V	–0.3 to V_{DD}+0.3	
Analog Input Voltage	V_{AI}		–0.3 to V_{DD}+0.3	
Maximum Power Dissipation	P_D	Ta=25°C (per package)	400	mW
		Ta=25°C (per output pin)	50	
Storage Temperature	T_{STG}	Excluding EEPROM data storage	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	f_{OSC}≤6MHz	4.5 to 5.5	V
Analog Supply Voltage	AV_{DD}	V_{DD}=AV_{DD} V_{RL}=AGND=GND=0V	4.5 to 5.5	
Analog Reference Voltage	V_{RH}*		AV_{DD}–0.5 to AV_{DD}	
Analog Input Voltage	V_{AI}		V_{RL} to V_{RH}	
Memory Hold Voltage	V_{DDMH}	f_{OSC}=0Hz	2.0 to 5.5	
Operating Frequency	f_{OSC}	V_{DD}=4.5V to 5.5V	1 to 6	MHz
Operating Temperature	T_{op}	—	–40 to +85	°C

* V_{RH} should be connected to V_{RL} if A/D converter is not used.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=AV_{DD}=4.5 to 5.5V, GND=AGND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V_{IH1}	CPUCLK=1MHz	2.4	—	—	V
"H" Input Voltage 2 *2	V_{IH2}	CPUCLK=1MHz	0.7V_{DD}	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	0.8	
"H" Output Voltage	V_{OH1}	I_{OH}=–200µA	0.75V_{DD}	—	—	
"L" Output Voltage	V_{OL1}	I_{OL}=1.6mA	—	—	0.4	
Input Leakage Current 1 *3	I_{LI1}	V_I=V_{DD}/0V	—	—	±1	µA
Input Leakage Current 2 *4	I_{LI2}	V_I=V_{DD}/0V	—	—	±10	
"L" Input Current *5	I_{IL}	V_I=0V	–100	–250	–500	
"L" Input Current *6	I_{IL}	V_I=0V	–40	–100	–200	
Input Capacitance	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Current Consumption at Standby	I_{DDS}	Sleep mode**	—	50	100	µA
Current Consumption during Writing to EEPROM	I_{DDE}	Sleep mode, no load	—	4	10	mA
Operating Current Consumption	I_{DD}	f_{OSC}=6MHz, no load See Figure 15-1	—	20	40	

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 OSC0 and $\overline{\text{RESET}}$
*3 $\overline{\text{EXWR}}$ and P6
*4 Excluding $\overline{\text{EXWR}}$ and P6
*5 P1 in pull-up input
*6 $\overline{\text{RESET}}$
** When the input ports and V_{REF} are at 0V and the output ports are unloaded.

AC Characteristics

• External memory control

(V_{DD}=AV_{DD}=V_{RH}=4.5 to 5.5V, GND=AGND=V_{RL}=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Cycle	t_C	—	167	—	ns
"L" Clock Pulse Width	t_{CLW}		75	—	
"H" Clock Pulse Width	t_{CHW}		75	—	
ALE Pulse Width	t_{AW}	C_L=100pF	$t_C+t_{CHW}-40$	—	
ALE Pulse Delay Time 1	t_{ALD1}		$t_{CLW}-20$	—	
ALE Pulse Delay Time 2	t_{ALD2}		$t_{CLW}-20$	—	
$\overline{RD}$ Pulse Width	t_{RW}		$t_C+t_{CHW}-40$	—	
$\overline{RD}$ Pulse Delay Time	t_{RD}		$t_{CLW}-20$	$t_{CLW}+40$	
$\overline{WR}$ Pulse Width	t_{WW}		$t_C+t_{CHW}-40$	—	
$\overline{WR}$ Pulse Delay Time	t_{WD}		$t_{CLW}-20$	$t_{CLW}+40$	
"L" Address Setup Time	t_{LAS}		t_C-40	—	
"H" Address Setup Time	t_{HAS}		$t_C+t_{CHW}-40$	—	
"L" Address Hold Time	t_{LAH}		$t_{CLW}-20$	—	
Bus Floating Time	t_{LAZ}		—	20	
"H" Address Hold Time	t_{HAHR}		$t_{CLW}-20$	—	
"H" Address Hold Time	t_{HAHW}		$t_{CLW}-20$	—	
Read Data Access Time	t_{RDAA}		—	$t_C+t_{CLW}-15$	
Read Data Access Time	t_{RDAR}		—	$t_{CHW}+10$	
Read Data Hold Time	t_{RDH}		0	—	
Write Data Hold Time	t_{WDS}		$t_C+t_{CHW}-40$	—	
Write Data Hold Time	t_{WDH}		$t_{CLW}-20$	—	

• CPU control

(V_{DD}=AV_{DD}=4.5 to 5.5V, GND=AGND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{RESET}$ Pulse Width *1	t_{RESW1}	—	20	—	ns
$\overline{RESET}$ Pulse Width *2	t_{RESW2}	—	oscillation stabilization time	—	—

*1 Except during power-on, sleep, and hardware stop modes

*2 During power-on, sleep, and hardware stop modes

• Peripheral control 1

(V_{DD} = AV_{DD} = 4.5 to 5.5V, GND = AGND = 0V, Ta = –40 to +85°C)

Parameter		Symbol	Condition	MIN	MAX	Unit
OSC	Clock Cycle	t_C	—	167	—	ns
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4 t_C	—	
T0	External Clock Pulse Width	t_{T0CW}		4 t_C	—	
	GATE Pulse Width	t_{T0GW}		1 t_{T0CLK} *	—	

* t_{T0CLK}: Cycle time of timer 0 count clock selected by T0CON.

• Peripheral control 2

(V_{DD}=AV_{DD}=4.5 to 5.5V, GND=AGND=0V, Ta=–40 to +85°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	—	167	—	ns
SIO (Clock Synchro-nous Mode)	Synchronous Clock Cycle	t_{SIC}		8 t_C	—	
	Synchronous Clock "L" Pulse Width	t_{SICLW}		4 t_C–20	—	
	Synchronous Clock "H" Pulse Width	t_{SICHW}		4 t_C–20	—	
	Output Data Setup Time	t_{SIOS}		6 t_C–100	—	
	Output Data Hold Time	t_{SIOH}		2 t_C–100	—	
	Input Data Setup Time	t_{SIIS}		t_C+t_{CLW}+100	—	
	Input Data Hold Time	t_{SIIH}		0	—	

• A/D converter characteristics

(V_{DD} = AV_{DD} = V_{RH} = 4.5 to 5.5V, GND = AGND = V_{RL} = 0V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the recommended circuit. Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Linearity Error	E_L		—	—	+1.5 –1.5	LSB
Differential Linearity Error	E_D		—	—	±0.5	LSB
Zero Scale Error	E_{ZS}		—	—	+1.5	LSB
Full Scale Error	E_{FS}		—	—	–1.5	LSB
Crosstalk	E_{CT}	Refer to the measuring circuit.	—	—	±0.5	LSB
Conversion Time*	t_{CONV}	f_{OSC} = 6MHz	—	26.7	—	µs/CH

* The conversion time immediately after G0 bit is set to "I" is 24.7µs/CH.

Definition of Terms

Resolution → Recognizable minimum input analog value.
This can be resolved into 2^8 = 256, that is (V_{RH} – V_{RL}) ÷ 256

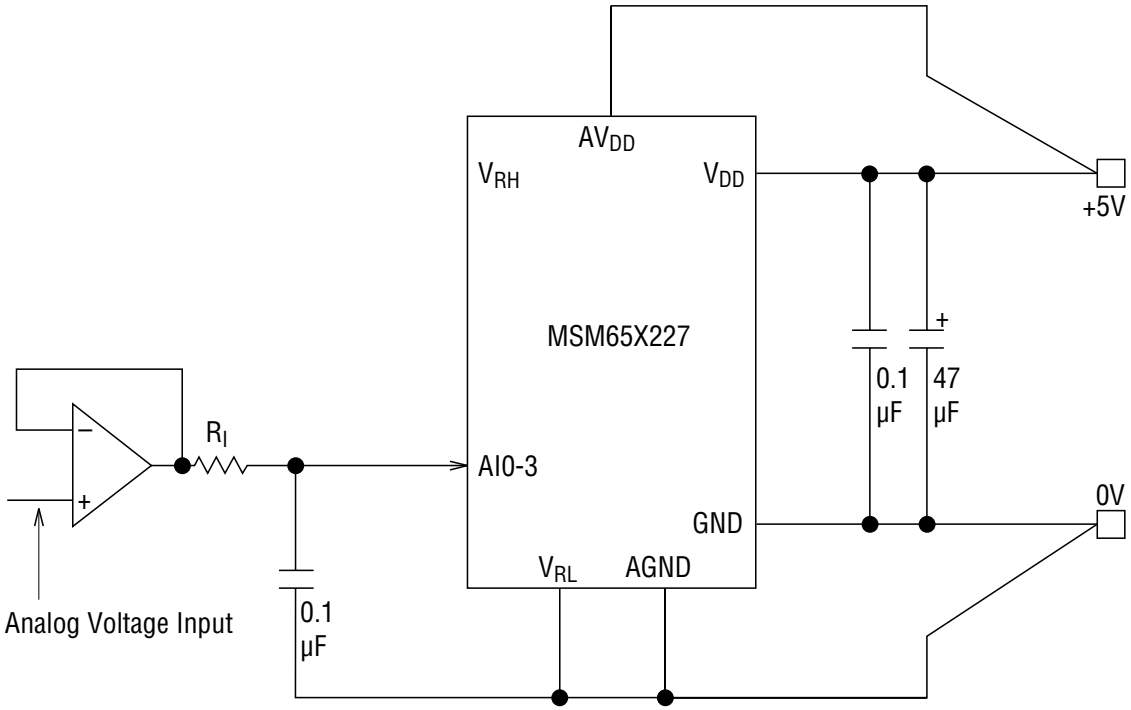
Linearity Error → Deviation between ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics. (Not including quantization error.)
Ideal conversion characteristics means a step which divides voltage between V_{RH} and L_{RL} into 256.

Differential Linearity Error → Shows the smoothness of conversion characteristics.
1LSB = (V_{RH} – V_{RL}) ÷ 256 is ideal for analog input voltage width corresponding to change per 1 bit of digital output. The differential linearity error is the deviation between this ideal bit size and a bit size at arbitrary point in conversion range.

Zero Scale Error → Deviation between ideal conversion characteristics of transfer point for digital outputs "000H" to "001H" and actual conversion characteristics.

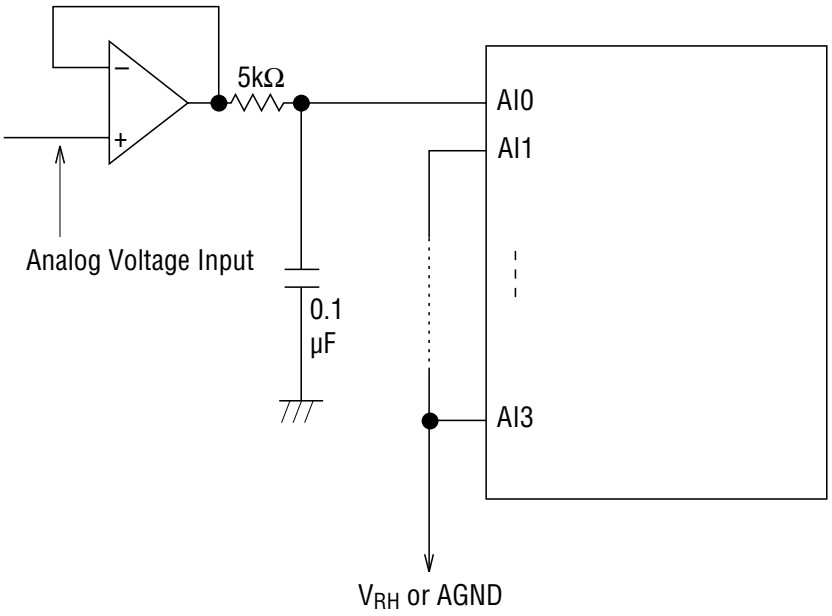
Full Scale Error → Deviation between ideal conversion characteristics of transfer point for digital outputs "0FEH" to "0FFH" and actual conversion characteristics.

Recommended circuit



R_I (Analog input source impedance) ≤ 5kΩ

Crosstalk measuring circuit



Crosstalk is defined as the difference of A/D conversion result between supplying the same voltage to AI0 to AI3 and supplying voltage shown in this left diagram.

EEPROM Characteristics

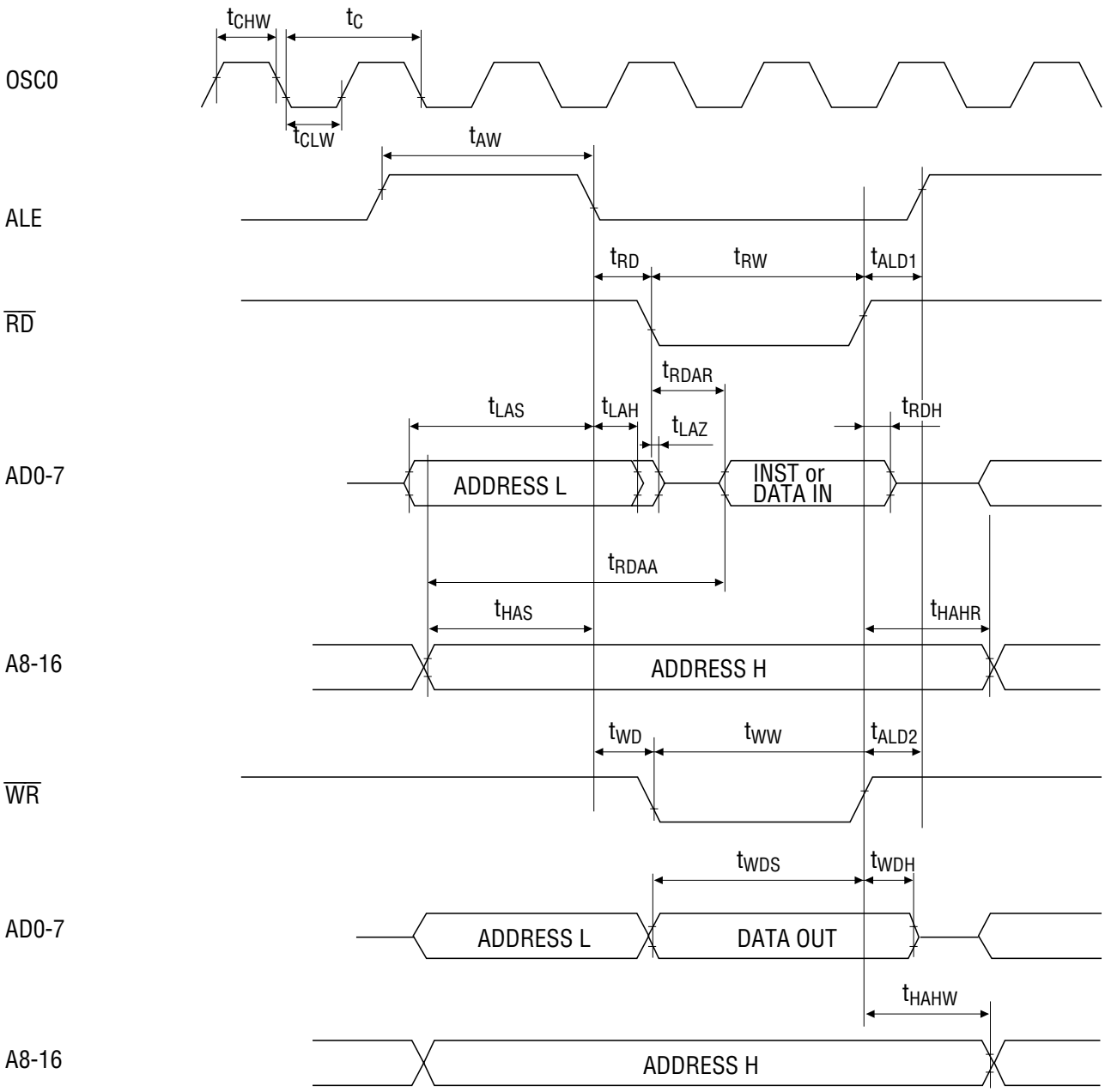
Parameter	Rating	Condition	
Number of rewrites	10,000	100 bytes	Failure rate < 1%
	100	3,996 bytes	
Data storage time	10 years	Storage between –40 and 85°C	

(V_{DD}=AV_{DD}=4.5 to 5.5V, GND=AGND=0V, Ta=–40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Write disable time after reset	t_{INHWR}	—	5	—	µs
Write time	t_{EEWR}	—	6	8	ms

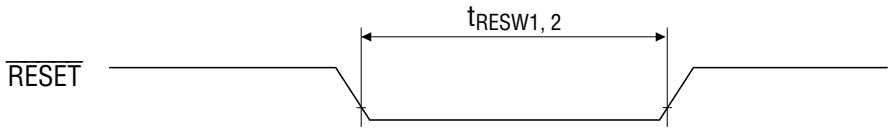
TIMING DIAGRAM

External Memory Control

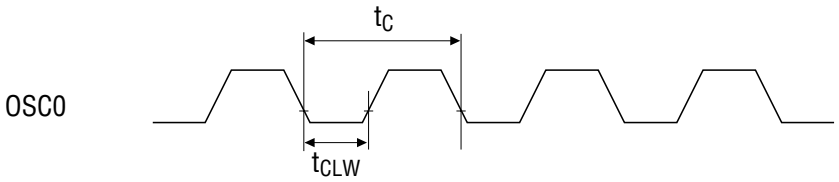


CPU Control

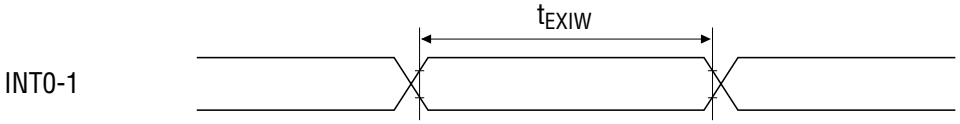
1) $\overline{\text{RESET}}$ pulse width



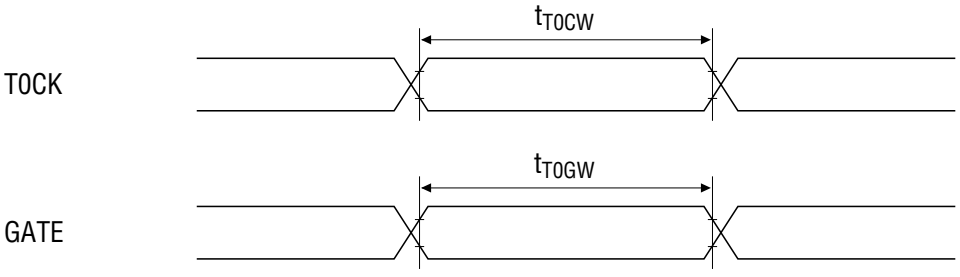
Peripheral control 1



1) EXI Pulse width

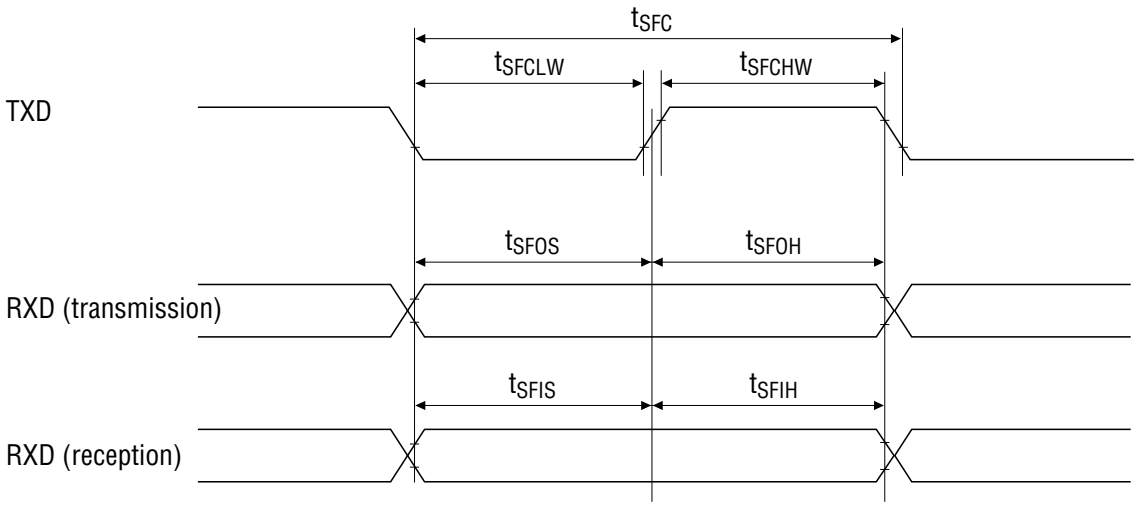


2) T0



Peripheral control 2

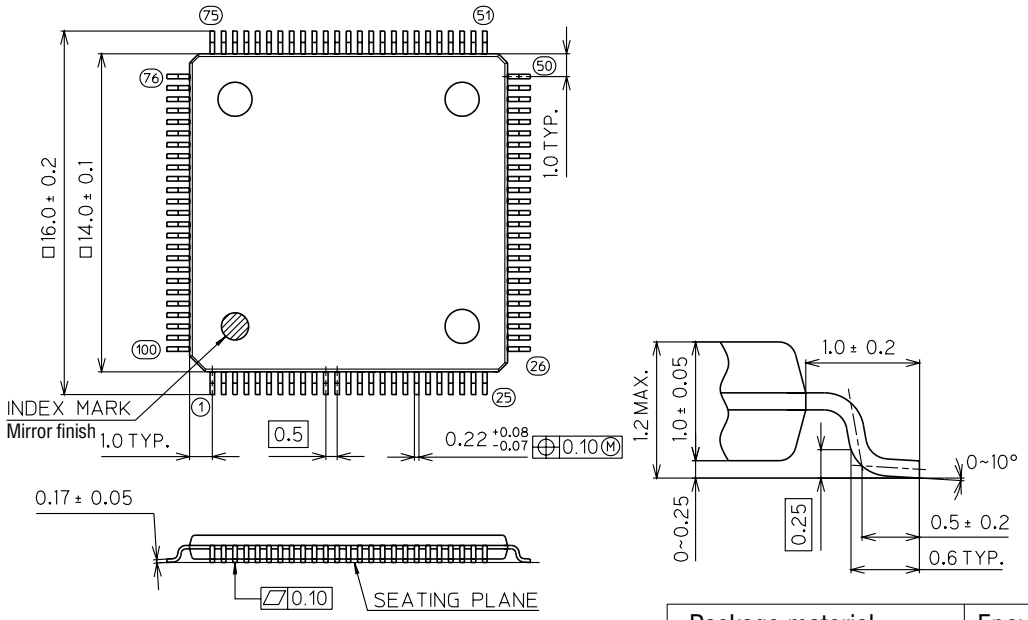
1) SIO
(Clock synchronous mode)



PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).