OKI Semiconductor

MSM6636

SAE-J1850 Communication Protocol Conformity Transmission Controller for Automotive LAN

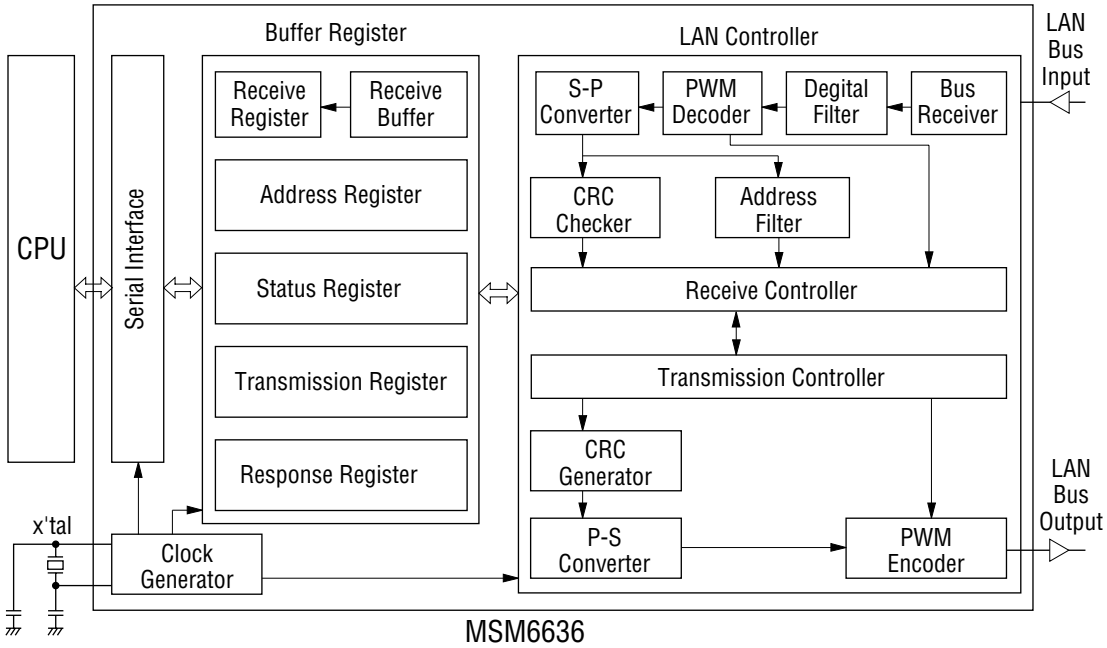
GENERAL DESCRIPTION

The MSM6636 is a transmission controller for automotive LAN based on data communication protocol SAE-J1850. This LSI can realize a data bus topology bus LAN system with a PWM bit encoding method (41.6 K bps). In addition to a protocol control circuit, MSM6636 has an enclosed quartz oscillation circuit, host CPU interface (clock synchronous serial / UART), a transmit/receive buffer, and a bus receiver circuit that decreases the burden on the host CPU.

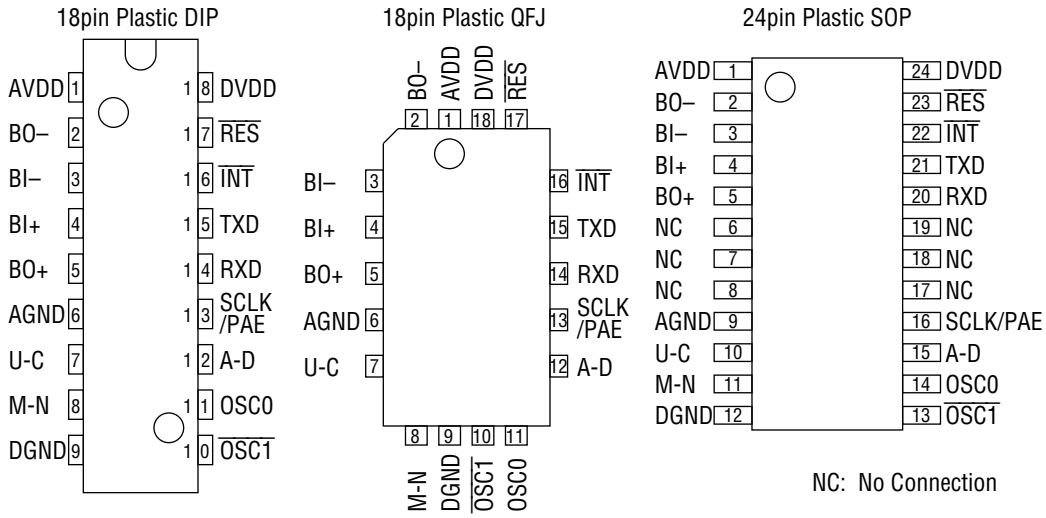
FEATURES

- Based on SAE-J1850 CLASS B DATA COMMUNICATION NETWORK INTERFACE (issued August 12, 1991)
- CSMA/CD (Carrier-sense multiple access with collision detection)
- Internal transmit buffer (1 frame) and receive buffer (2 frames)
- Bit encoding: PWM (Pulse Width Modulation)
- Transmission Speed: 41.6K bps
- Multi-address setting with physical addressing: 1 type / functional addressing: 15 types
- Address filter function by multi-addressing (broadcasting possible)
- Automatic retransmission function by arbitration loss and non ACK
- 3 types of in-frame response support:
  ① Single-byte response from a single recipient
  ② Multi-byte response from a single recipient (with CRC code)
  ③ Single-byte response from multiple recipients (ID response as ACK)
- Error detection by cyclic redundancy check (CRC)
- Various communication error detections
- Dual-wire bus abnormality detection by internal bus receiver and fault tolerance function
- Host CPU interface is LSB first / serial, 4 modes supported
  ① Clock synchronous serial (no parity)
  Normal mode: 8-bit data
  MPC Mode: 8-bit data + MPC bit (1: address / 0: data select bit)
  ② UART (yes/no parity selectable)
  Normal mode: 1 start bit + 8-bit data + (parity) + 1 stop bit
  MPC mode: 1 start bit + 8-bit data + MPC bit + (parity) + 1 stop bit
- Sleep Function
  Low current consumption mode by oscillation stop (IDS Max < 50µA)
  SLEEP / WAKE UP control from host CPU, WAKE UP via LAN bus
- Available package 18pin DIP, 18 pin QFJ (PLCC) and 24pin SOP.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Pin Name	Pin # DIP/QFJ	Pin # SOP	I/O	Function
AVDD	1	1	—	Analog power supply pin
BO –	2	2	O	LAN - BUS output –
BI –	3	3	I	LAN - BUS input –
BI +	4	4	I	LAN - BUS input +
BO +	5	5	O	LAN - BUS output +
AGND	6	9	—	Analog ground pin
U - C	7	10	I	0: UART 1: clock synchronous serial select pin
M - N	8	11	I	0: MPC mode 1:normal mode select pin
DGND	9	12	—	Digital ground pin
$\overline{\text{OSC 1}}$	10	13	O	Crystal oscillation output
OSC 0	11	14	I	Crystal oscillation input
A - D	12	15	I	0: data communication 1: address communication
SCLK / PAE	13	16	I	Serial clock input/Parity select pin
RXD	14	20	I	Serial data input pin
TXD	15	21	O	Serial data output pin
$\overline{\text{INT}}$	16	22	O	Interrupt output pin
$\overline{\text{RES}}$	17	23	I	Reset input pin
DVDD	18	24	—	Digital power supply pin

ABSOLUTE MAXIMUM RATINGS

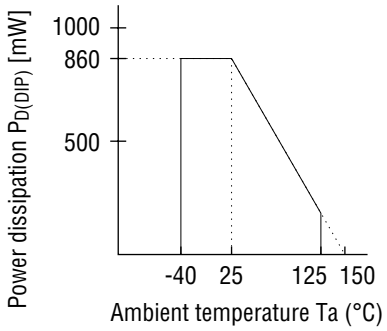
DGND = AGND = 0V

Parameter	Symbol	Condition	Rated Value	Unit
Power Supply Voltage	DVDD, AVDD		-0.3~7.0	V
Input Voltage	V_I	AVDD = DVDD	-0.3~DVDD+0.3	V
Output Voltage	V_O	AVDD = DVDD	-0.3~DVDD+0.3	V
Power Dissipation	$P_{D(DIP)}$*1	Ta = 25°C	860	mW
	$P_{D(QFJ)}$*2	Ta = 25°C	960	mW
	$P_{D(SOP)}$*3	Ta = 25°C	830	mW
Storage Temperature	T_{STG}		-55~150	°C

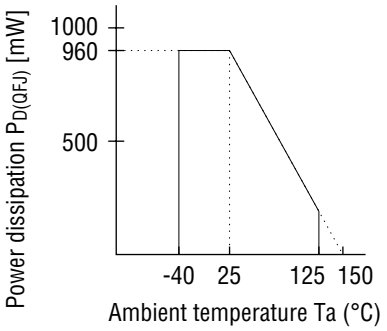
$P_{D(DIP)}$*1: 18PIN DIP package power dissipation
$P_{D(QFJ)}$*2: 18PIN QFJ package power dissipation
$P_{D(SOP)}$*3: 24PIN SOP package power dissipation

Power Dissipation Curve

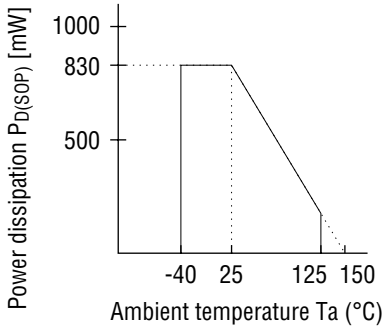
< 18PIN DIP package >



< 18PIN QFJ package >



< 24PIN SOP package >



OPERATION RANGE

DGND = AGND = 0V

Parameter	Symbol	Condition	Rated Value	Unit
Power Supply Voltage	DVDD, AVDD	AVDD = DVDD	4.5~5.5	V
Operating Frequency	f_{OSC}	DVDD = AVDD = 5V±10%	2~16	MHz
Operating Temperature	Ta		-40~+125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

DVDD = AVDD = 5V±10%, DGND = AGND = 0V, Ta = -40 ~ +125°C

Parameter	Symbol	Condition	Application	MIN	TYP	MAX	Unit
H Level Input Voltage	V_{IH1}	—	A	DVDD × 0.8	—	DVDD + 0.3	V
L Level Input Voltage	V_{IL1}	—	A	DGND - 0.3	—	DVDD × 0.2	V
H Level Input Voltage	V_{IH2}	—	F	DVDD - 2.0	—	DVDD + 1.0	V
L Level Input Voltage	V_{IL2}	—	F	DGND - 1.0	—	DGND + 2.0	V
Receiver Hysteresis Width	V_H	—	F	100	—	400	mV
H Level Input Current	I_{IH1}	$V_I = V_{DD}$	B	—	—	+ 1	µA
L Level Input Current	I_{IL1}	V_I = 0V	B	—	—	- 1	µA
H Level Input Current	I_{IH2}	$V_I = V_{DD}$	C	—	—	+ 1	µA
L Level Input Current	I_{IL2}	V_I = 0V	C	—	—	- 100	µA
H Level Input Current	I_{IH3}	$V_I = V_{DD}$	BI (+)	—	—	+ 100	µA
L Level Input Current	I_{IL3}	V_I = 0V	BI (-)	—	—	- 100	µA
H Level Output Voltage	V_{OH1}	I_O = -400µA	D	DVDD - 0.4	—	—	V
L Level Output Voltage	V_{OL1}	I_O = +3.2mA	D	—	—	DGND + 0.4	V
H Level Output Voltage	V_{OH2}	I_O = -4.0mA	E	DVDD - 0.4	—	—	V
L Level Output Voltage	V_{OL2}	I_O = +4.0mA	E	—	—	DGND + 0.4	V
GND Offset Voltage	V_{OFF}	—	—	—	—	±1	V
Current Consumption 1	I_{DS}	During sleep	—	—	—	50	µA
Current Consumption 2	I_{DD}	f = 16MHz, no load	—	—	—	10	mA

A: $\overline{RES}$, SCLK/PAE, RXD, U-C, M-N, A-D, OSC0

B: SCLK/PAE, RXD, U-C, M-N, A-D

C: $\overline{RES}$

D: TXD, $\overline{INT}$

E: BO-, BO+

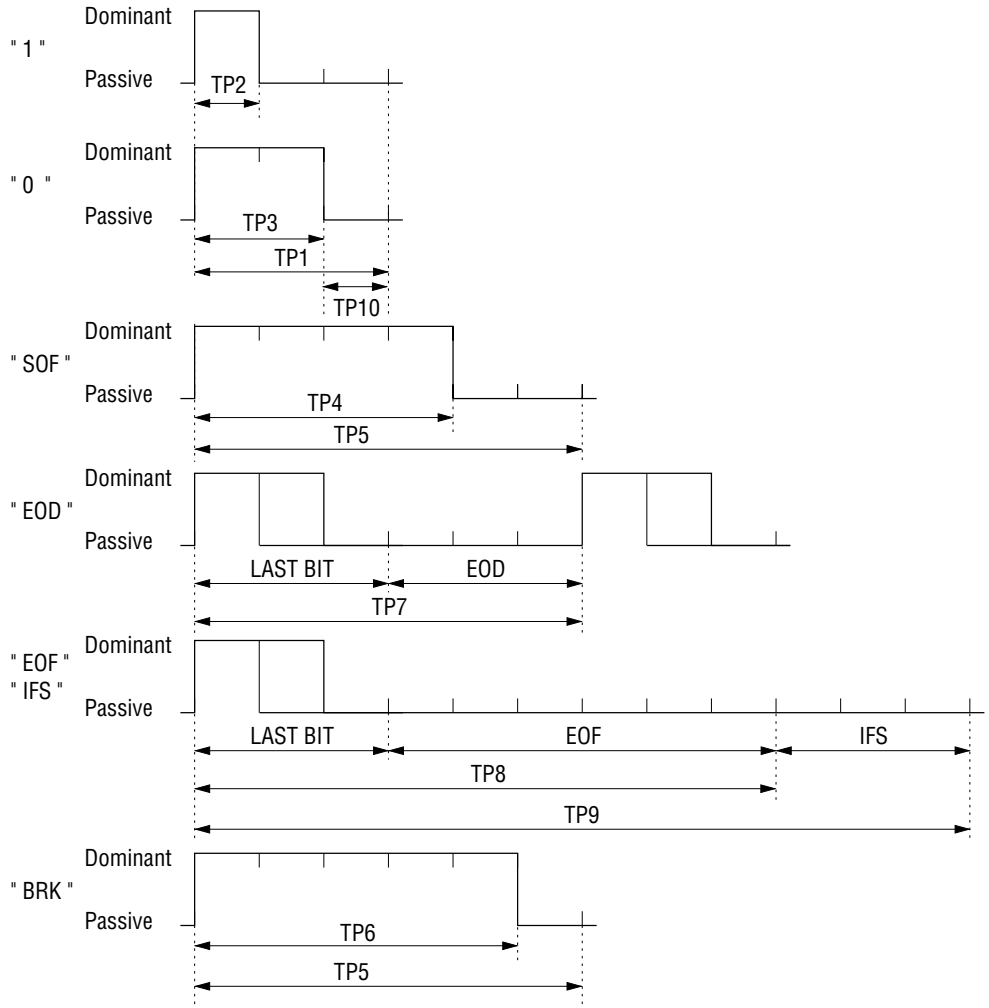
F: BI-, BI+

AC Chacteristics

PWM Bit Timing

Parameter	Symbol	Transmit			Receive		Unit
		min	typ	max	min	max	
Bit Length	TP1	23.64	24.00	24.36	21.00	28.00	µs
"1" Dominant Width	TP2	6.90	7.00	7.11	5.00	12.00	µs
"0" Dominant Width	TP3	14.87	15.00	15.23	13.00	20.00	µs
"SOF" Dominant Width	TP4	30.54	31.00	31.47	29.00	36.00	µs
"SOF,BRK" Length	TP5	47.28	48.00	48.72	45.00	52.00	µs
"BRK" Dominant Width	TP6	38.42	39.00	39.59	37.00	44.00	µs
"EOD" + Bit Length	TP7	47.28	48.00	48.72	43.00	51.00	µs
"EOF" + Bit Length	TP8	70.92	72.00	—	69.00	76.00	µs
"EOF + IFS" + Bit Length	TP9	94.56	96.00	—	86.00	—	µs
"0" Passive Width	TP10	8.86	9.00	9.14	4.00	15.00	µs

Note: DVDD = AVDD = 5 V ± 10%, Ta = -40 ~ +125℃, In setting 41.6 K bps



CPU Serial Interface Timing

❍Clock synchronous Serial

DVDD=AVDD=5V±10%, Ta =-40~+125°C

Parameter	Symbol	Min	Typ	Max	Unit
OSCO (source oscillation) Pulse Cycle	tø	62	—	500	ns
SCLK-L Interval Width	t_{CKLW}	8tø	—	—	ns
SCLK-H Interval Width	t_{CKHW}	8tø	—	—	ns
SCLK ↑ - RXD Setup Time	t_{SRS}	4tø	—	—	ns
SCLK ↑ - RXD Hold Time	t_{SRH}	4tø	—	—	ns
SCLK ↑ - TXD Output Delay Time	t_{STD}	4tø	—	6tø + 100	ns
A-D - SCLK ↑ Setup Time	t_{AS}	0	—	—	ns
SCLK ↑ - A-D Hold Time	t_{AH}	8tø	—	—	ns
SCLK Frame Interval Time *1	t_{INT1}	8tø	—	—	ns
SCLK Frame Interval Time *2	t_{INT2}	16tø	—	—	ns

SCLK Frame Interval Time *1

Between “Communication type (WR) and address setting” frame and “WR data” frame.
Between “WR data” frame and “WR data” frame during continuous WR.

SCLK Frame Interval Time *2

Between “Communication type (RD) and address setting” frame and “RD data” frame.
Between “RD data” frame and “RD data” frame during continuous RD.

❍UART

DVDD=AVDD=5V±10%, Ta =-40~+125°C

Parameter	Symbol	Min	Typ	Max	Unit
A-D - STOP bit ↑ Setup Time	t_{UAS}	0	—	—	ns
STOP bit ↓ – A-D Hold Time	t_{UAH}	0	—	—	ns
START bit ↓ – TXD Output Delay Time	t_{UTD}	48tø	—	50tø + 100	ns
Write Frame Interval Time *3	t_{INT3}	0	—	—	ns
Read Frame Interval Time *4	t_{INT4}	10tø	—	—	ns

Write Frame Interval Time *3

Between “Communication type (WR) and address setting” frame and “WR data” frame.

Between “WR data” frame and “WR data” frame during continuous WR.

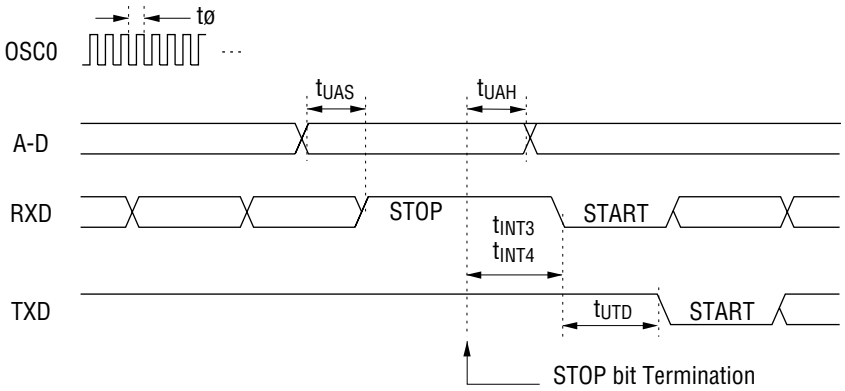
Read Frame Interval Time *4

Between “Communication type (RD) and address setting” frame and “RD data” frame.

Wakeup Input Signal

DVDD=AVDD=5V±10%, Ta =-40~+125°C

Parameter	Symbol	Min	Typ	Max	Unit
LAN bus Passive → Dominant Change Pulse Width	t_{WD}	7	—	—	µs
RXD Terminal Input Pulse Width	t_{WR}	300	—	—	ns
Bus Receiver Stable Time *5	t_{RS}	1	—	—	µs



Note: The time chart shows the wakeup input signals from each sleep status

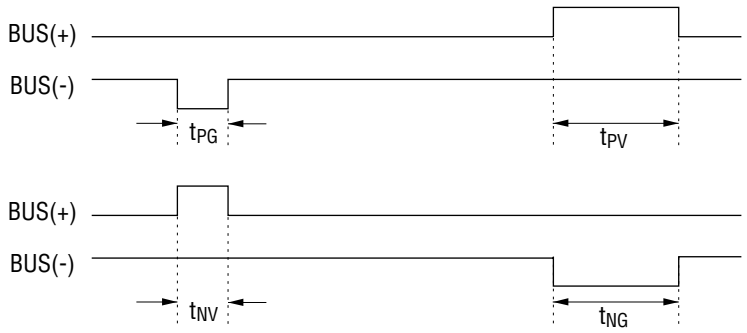
Bus Receiver Stable Time *5

The stable time of the bus receiver is from just after wakeup to the restart of message transmission and reception. However, the clock oscillation source should use an external clock. (A clock is input even in the sleep status.)

Fault Tolerant Function Operation Conditions

DVDD=AVDD=5V±10%, Ta =-40~+125°C, In setting 41.6Kbps

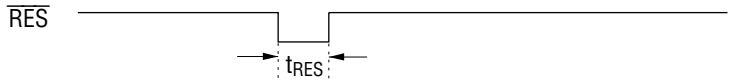
Parameter	Symbol	Min	Typ	Max	Unit
LAN bus (+) GND Short Circuit Detection Pulse Width	t_{PG}	5	—	—	µs
LAN bus (+) VDD Short Circuit Detection Pulse Width	t_{PV}	48	—	—	µs
LAN bus (-) GND Short Circuit Detection Pulse Width	t_{NG}	48	—	—	µs
LAN bus (-) VDD Short Circuit Detection Pulse Width	t_{NV}	5	—	—	µs



Reset Input Pulse Width

DVDD=AVDD=5V±10%, Ta=–40~+125°C

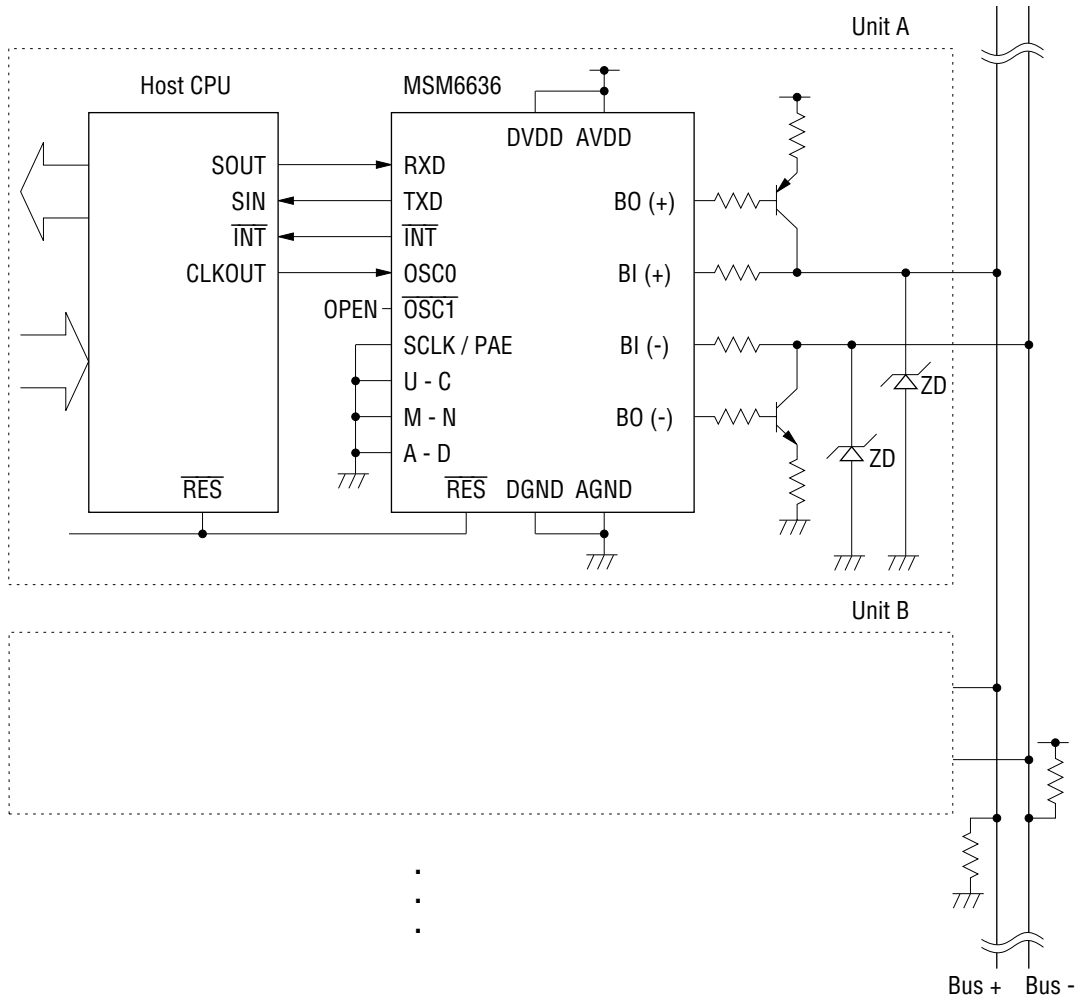
Parameter	Symbol	Min	Typ	Max	Unit
Reset Input Pulse Width	t_{RES}	0.1	—	—	µs



APPLICATION EXAMPLE

Host CPU and LAN bus Connection Example

Host CPU and LAN bus connection example of MSM6636 is shown below.



The above connection example is when "UART, MPC and parity no mode" was used as the "host CPU interface, and when CLKOUT output of the host CPU" was used as the clock for MSM6636.

Depending on the control target, an optimum host CPU (number of ports, A/D converter yes / no) can be selected, and an optimum system can be constructed.