OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM6648

100-DOT COMMON DRIVER

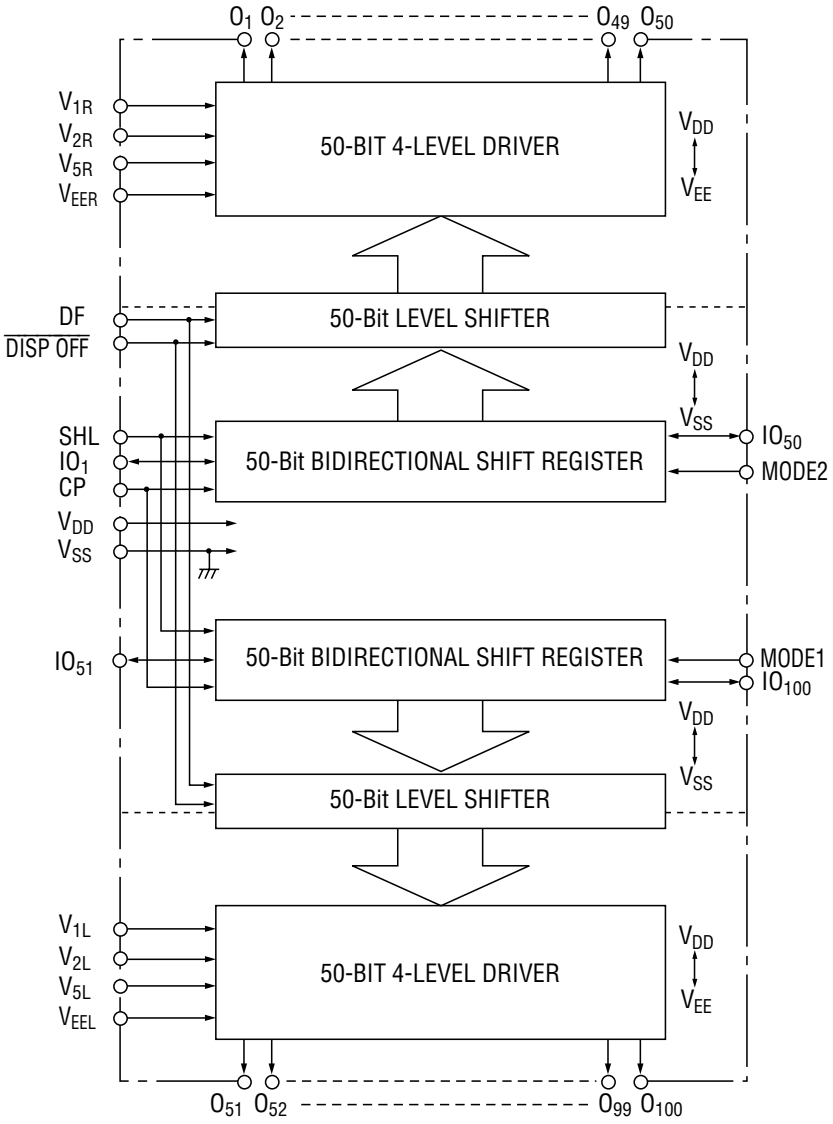
GENERAL DESCRIPTION

The MSM6648 is a dot matrix LCD common driver. Fabricated in CMOS technology, the device consists of two 50-bit bidirectional shift registers, two 50-bit level shifters, and two 50-bit 4-level drivers.
The MSM6648 is equipped with 100 LCD output pins. By connecting more than two MSM6648s in cascade, this LSI is applicable to a wide LCD panel.

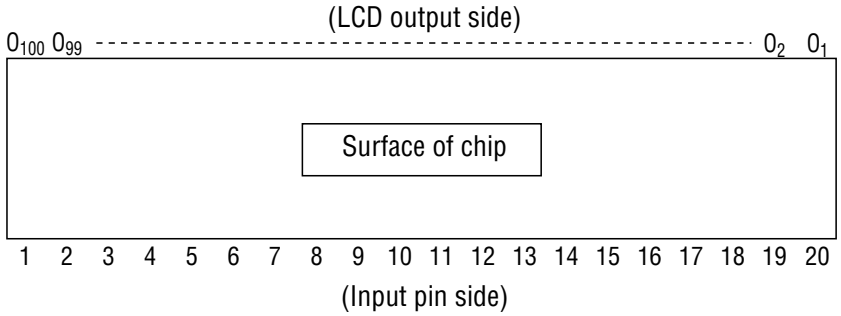
FEATURES

- Logic supply voltage : 2.7 to 5.5 V
- LCD drive voltage : 18 to 28 V
- Applicable LCD duty : 1/64 to 1/240
- Suitable for bath panel sizes of 400 (200 × 2) and 480 (240 × 2) in common numbers by the use of intermediate data input and 10-bit bypass function.
- Structure:
  Tape Carrier Package (TCP) mounting with 35 mm wide film
  (Product name : MSM6648AV-Z-01)
  Sn-plated

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Pin	Symbol	Pin	Symbol
1	V_{1L}	11	IO_{50}
2	V_{2L}	12	V_{SS}
3	V_{5L}	13	DF
4	V_{EEL}	14	CP
5	MODE1	15	IO_1
6	IO_{100}	16	MODE2
7	$\overline{\text{DISP OFF}}$	17	V_{EER}
8	V_{DD}	18	V_{5R}
9	SHL	19	V_{2R}
10	IO_{51}	20	V_{1R}

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage (1)	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage (2)	V_{DD}–V_{EE} *1	Ta = 25°C	0 to 30	V
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–30 to +85	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_{DD} \geq V_1 > V_2 \geq V_{DD} - 10V$, $V_{EE} + 10V \geq V_5 > V_{EE}$
$V_1 = V_{1L} = V_{1R}$, $V_2 = V_{2L} = V_{2R}$, $V_5 = V_{5L} = V_{5R}$, $V_{EE} = V_{EEL} = V_{EER}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage (1)	V_{DD}	—	2.7 to 5.5	V
Power Supply Voltage (2)	$V_{DD} - V_{EE}$ *1	No load	14 to 28	V
		During LCD drive	18 to 28	V
Operating Temperature	Top	—	–20 to +75	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_{DD} \geq V_1 > V_2 \geq V_{DD} - 7V$, $V_{EE} + 7V \geq V_5 > V_{EE}$
$V_1 = V_{1L} = V_{1R}$, $V_2 = V_{2L} = V_{2R}$, $V_5 = V_{5L} = V_{5R}$, $V_{EE} = V_{EEL} = V_{EER}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8V_{DD}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	V_{SS}	—	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	V_I = V_{DD}, V_{DD} = 5.5V	—	—	1	µA
"L" Input Current	I_{IL} *1	V_I = 0V, V_{DD} = 5.5V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O = –0.2mA, V_{DD} = 2.7V	V_{DD} – 0.4	—	—	V
"L" Output Voltage	V_{OL} *2	I_O = 0.2mA, V_{DD} = 2.7V	—	—	0.4	V
ON Resistance	R_{ON} *4	V_{DD} – V_{EE} = 25V, | V_N – V_O | = 0.25V *3	—	—	2	kΩ
Supply Current	I_{SS}	f_{CP} = 28kHz, V_{DD} = 3.0V	—	—	50	µA
	I_{EE}	V_{DD} – V_{EE} = 25V, No load	—	—	300	
Input Capacitance	C_I	f = 1MHz	—	5	—	pF

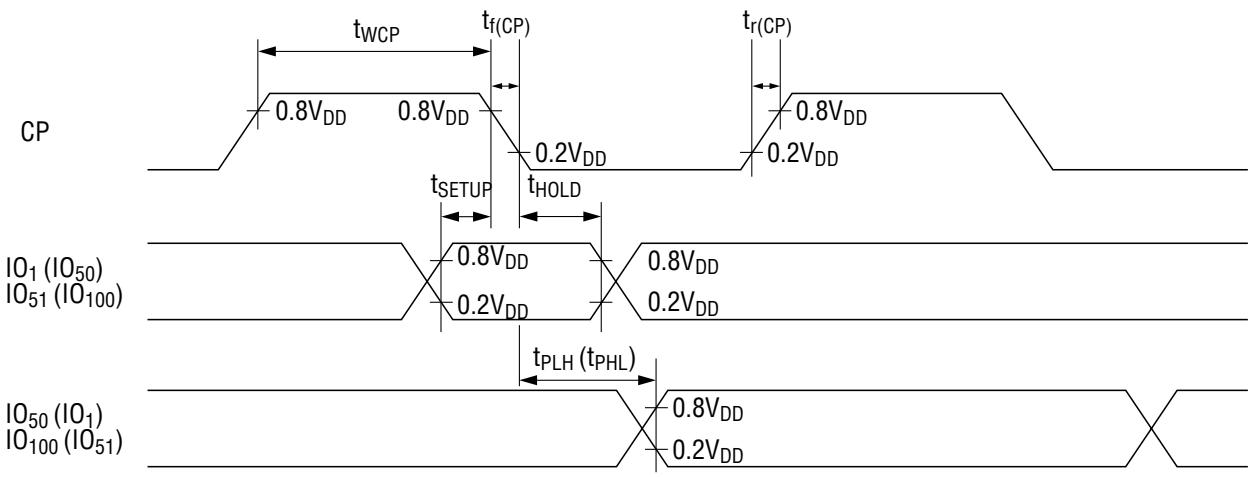
*1 Applicable to CP, IO_1, IO_{50}, IO_{100}, SHL, DF, $\overline{\text{DISP OFF}}$, MODE1, MODE2.
*2 Applicable to IO_1, IO_{50}, IO_{51}, IO_{100}
*3 V_N = V_{DD} to V_{EE}, V_2 = 1/16 (V_{DD} – V_{EE}), V_5 = 15/16 (V_{DD} – V_{EE}), V_{DD} = V1, V_{DD} = 4.5V
*4 Applicable to O_1 to O_{100}

Switching Characteristics

(V_{DD} = 2.7 to 5.5V, Ta = –20 to +75°C, C_L = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	t_{PLH}, t_{PHL}	—	—	—	3	µs
Clock Frequency	f_{CP}	—	—	—	1	MHz
CP Pulse Width	t_{WCP}	—	63	—	—	ns
Data Setup Time	t_{SETUP}	—	100	—	—	ns
Data Hold Time	t_{HOLD}	—	100	—	—	ns
Rise/Fall Time of CP	$t_{r\,(CP)}$, $t_{f\,(CP)}$	—	—	—	20	ns

Note 1 : When display is controlled by $\overline{\text{DISPOFF}}$ pin, CP rise and fall time must be ≤ 1 µs.



FUNCTIONAL DESCRIPTION

Pin Functional Description

• IO, IO_{50}, IO_{51}, IO_{100}

These are I/O pins for the two 50-bit bidirectional shift registers.

• SHL

This is an input pin to select the shift direction of the two 50-bit bidirectional shift registers. Set this pin to "H" or "L" level during power-on.

• MODE1, MODE2

These are input pins to select whether the two 50-bit shift registers are used as a two 50-bit application or a 40-bit and 50-bit application.

Functions of the SHL, MODE1 and MODE2 pins are shown below.

SHL	MODE1	MODE2	Scan direction	Data input pin	Scan output pin	Function
L	—	L	$O_1 \rightarrow O_{50}$	IO_1	IO_{50}	The scan data input into the IO_1, and IO_{51} pins are shifted at the falling edge of CP and are output from the IO_{50} and IO_{100} pins after the lapse of 50 clock pulses.
			$O_{51} \rightarrow O_{100}$	IO_{51}	IO_{100}	
H	L	—	$O_{50} \rightarrow O_1$	IO_{50}	IO_1	The scan data input into the IO_{100} and IO_{50} pins are shifted at the falling edge of CP and are output from the IO_{51} and IO_1 pins after 50 clock pulses.
			$O_{100} \rightarrow O_{51}$	IO_{100}	IO_{51}	
L	—	H	$O_{11} \rightarrow O_{50}$	IO_1	IO_{50}	This condition means a mode of bypassing between the O_1 and O_{10} pins. The scan data input into the IO_1 pin is stored in the O_{11} pin and is output from the IO_{50} pin after 40 clock pulses. The operation in the O_{51} to O_{100} pins is the same as that in setting SHL to "L" and MODE2 to "L".
			$O_{51} \rightarrow O_{100}$	IO_{51}	IO_{100}	
H	H	—	$O_{50} \rightarrow O_1$	IO_{50}	IO_1	This condition means a mode of bypassing between the O_{91} and O_{100} pins. The scan data input into the IO_{100} pin is stored in O_{90} and is output from the IO_{51} pin after 40 clock pulses. The operation in the O_1 to O_{50} pins is the same as that in setting SHL to "H" and MODE1 to "L".
			$O_{90} \rightarrow O_{51}$	IO_{100}	IO_{51}	

- **CP**

  This is a clock pulse input pin for two 50-bit bi-directional shift registers. Scan data is shifted at the falling edge of a clock pulse.

- **DF**

  This is an input pin for an LCD drive waveform AC synchronization signal, which generally inputs a frame inversion signal. See the Truth Table.

- **$\overline{\text{DISP OFF}}$**

  This is an input pin used to control the output pins O_1 to O_{100}. Signals on the V_1 level are output from the output pins O_1 to O_{100}, independent of the shift register data during low signal input. See the Truth Table.

- **O_1 to O_{100}**

  These are 4-level driver output pins, directly corresponding to each bit of the shift register. DF signals combined to shift register data select and output any of four levels V_1, V_2, V_5, and V_{EE}.

- **V_{DD}, V_{SS}**

  These are power supply pins. V_{DD} is normally 2.7 to 5.5 V. V_{SS} is a grounding pin, which is normally set to 0 V.

- **V_{1L}, V_{2L}, V_{5L}, V_{EEL}, V_{1R}, V_{1R}, V_{5R}, V_{EER}**

  These are LCD drive bias voltage pins. The V_1 pin may be separated from the V_{DD} pin. Bias supply voltages are supplied from an external source.

Truth Table

DF	Shift register data	$\overline{\text{DISP OFF}}$	Driver output (O_1 to O_{100})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
×	×	L	V_1

× : Don't care

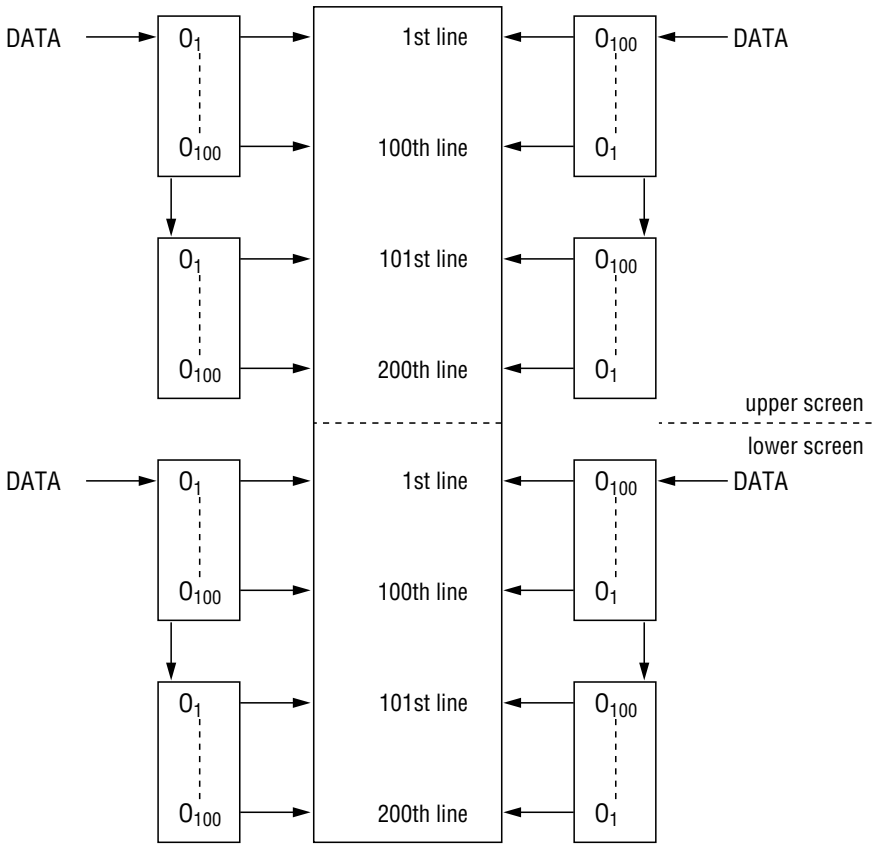
NOTES ON USE

Note the following when turning power on and off:
The LCD drivers of this IC requires a high voltage. If a high voltage is applied to them with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the following power-on and power-off sequences.
When turning power on:
First turn on the logic circuits, then the LCD drivers, or turn on both of them at the same time.
When turning power off:
First turn off the LCD drivers, then the logic circuits, or turn off both of them at the same time.

APPLICATION CIRCUITS

Example of connecting to LCD panel

In the case of 400 (200 × 2) lines



In the case of 480 (240 × 2) lines