OKI Semiconductor

MSM6789A/6789L

SBC Solid-State Recorder IC

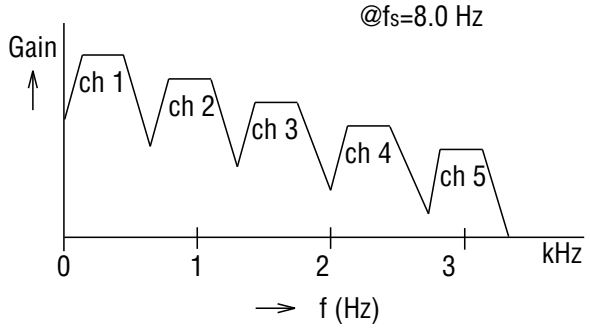
GENERAL DESCRIPTION

The MSM6789A/6789L, an improved version of MSM6788, is a solid-state recorder developed using the Sub Band Coding (SBC) method.
Just like MSM6788, the MSM6789A/6789L has a stand-alone mode and a microcontroller interface mode. In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6789A/6789L can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller, and more functions are available than in the stand-alone mode.
The MSM6789A/6789L can directly drive serial voice ROM as external memory as well as serial register or general-purpose DRAM* (1-bit × or 4-bit × type selectable) as external memories, which allows a recording and playback circuit with fixed messages to be built easily. The method from microcontroller is the same as the MSM6788.
* Only for MSM6789A

- Difference between MSM6788 and MSM6789A

	MSM6788	MSM6789A
General DRAM	Unavailable	Available
Unvoiced-part elimination function	No	Yes
PCM playback	No	Yes

- SBC method:
  The SBC method divides voice frequencies into five bands and codes the component for each of the bands separately, as shown below.



Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

• Difference between MSM6789A and MSM6789L

Parameter	MSM6789A	MSM6789L
Operating voltage	4.5 to 5.5 V	3.0 to 3.6 V
External memory	General-purpose DRAM, 32 Mbits (max.) 1-Mbit DRAM (MSM514256B, MSM511000B) 4-Mbit DRAM (MSM514400C, MSM514100C) 16-Mbit DRAM (MSM511740CA, MSM5116100A) ARAM*, 32 Mbits (max.) Serial register, 32 Mbits (max.) 4 Mbits (MSM6684B) 8 Mbits (MSM6685)	16 Mbits (max.) 4 Mbits (MSM66V84B)

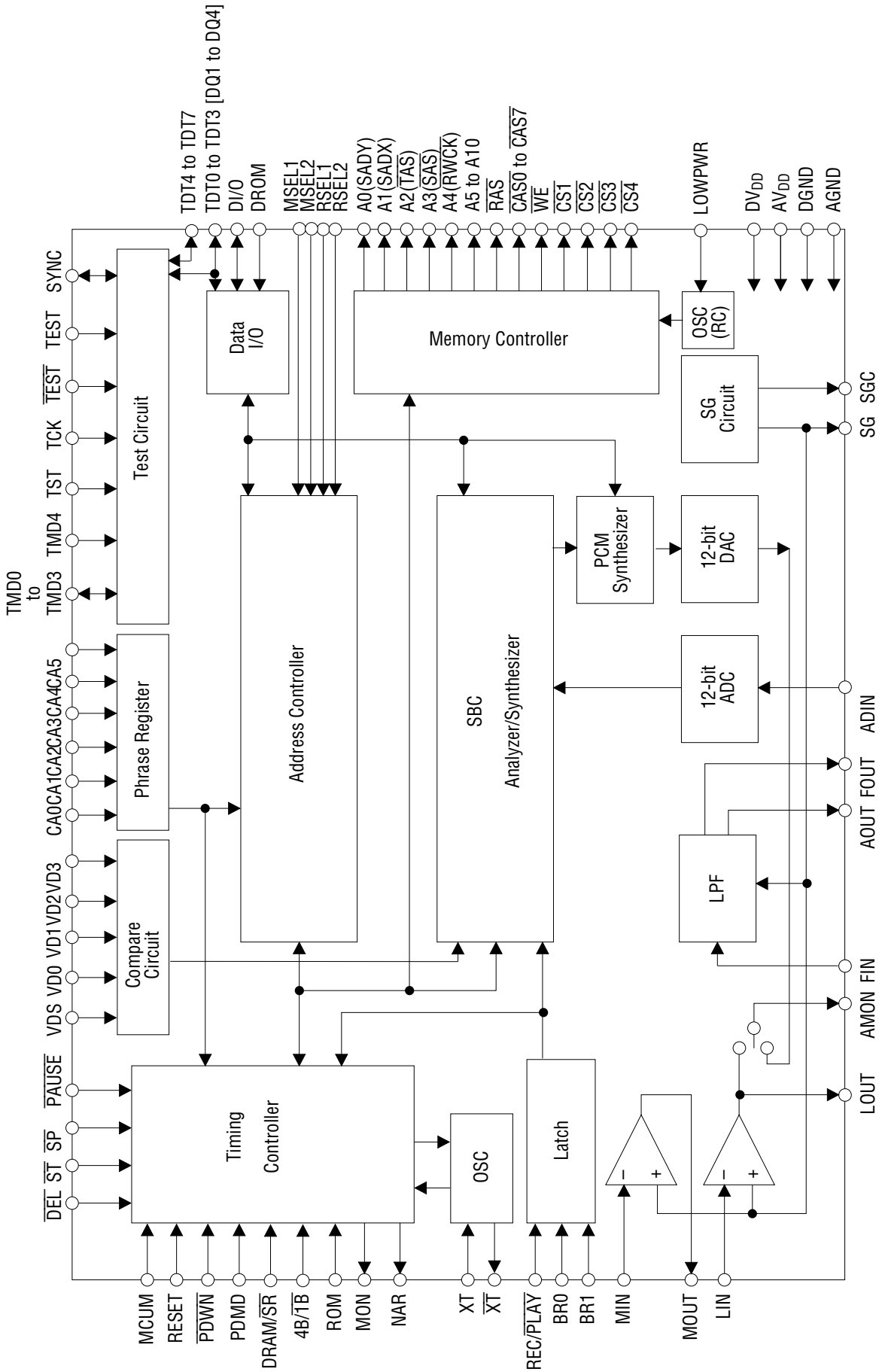
* Use ARAM which has no failed bits in its first 64 Kbits.

STAND-ALONE MODE

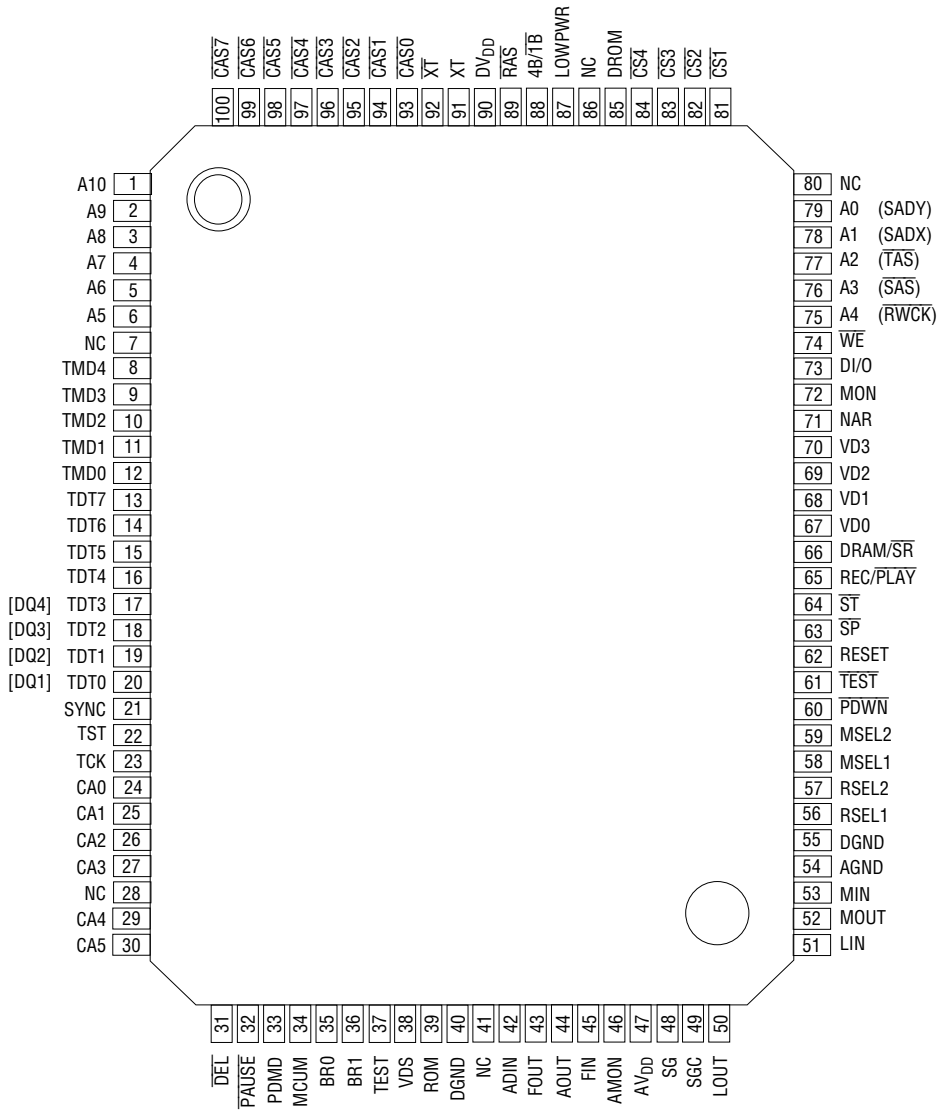
FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  MSM6789A (5 V version)
    General-purpose DRAM, 32 Mbits maximum (for variable messages)
      1-Mbit DRAM : Can be directly driven (MSM514256B, MSM511000B)
      4-Mbit DRAM : Can be directly driven (MSM514400C, MSM514100C)
      16-Mbit DRAM : Can be directly driven (MSM5117400A, MSM5116100A)
    ARAM, 32 Mbits maximum (for variable messages)
      Note :Use the first 64 Kbits with no failed bits for the ARAM.
    Serial register, 32 Mbits maximum (for variable messages)
      4-Mbit serial register : Can be directly driven (MSM6684B)
      8-Mbit serial register : Can be directly driven (MSM6685)
  MSM6789L (3.3 V version)
    Serial register, 16 Mbits maximum (for variable messages)
      4-Mbit serial resister: Can be directly driven (MSM66V84B)
  MSM6789A (5 V version) and MSM6789L (3.3 V version)
    Serial voice ROM, 4 Mbits maximum (for fixed messages)
      1-Mbit serial voice ROM : Can be directly driven (MSM6595A)
      2-Mbit serial voice ROM : Can be directly driven (MSM6596A)
      3-Mbit serial voice ROM : Can be directly driven (MSM6597A)
- Bit rate
  10.0, 12.6, 16.0 kbps (at 8 kHz sampling freq.)
  7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)
- Maximum recording time (when one 8-Mbit serial register is connected)
  13.8 minutes (for 10.0 kbps SBC) 18.4 minutes (for 7.5 kbps SBC)
  11.0 minutes (for 12.6 kbps SBC) 14.6 minutes (for 9.5 kbps SBC)
  8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Unvoiced-part elimination function (voice detect level can be set)
- Pausing function
- Master clock frequency: 6.0 MHz to 8.192 MHz
- Power supply voltage:
    MSM6789A : Single 5 V power supply
    MSM6789L : Single 3.3 V power supply
- Package options:
    MSM6789A : 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK)
    MSM6789L : 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

( ) : Pins for connecting serial voice ROM
[ ] : Pins for connecting 4-bit × type DRAM
NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1 μF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1 μF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	—	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
66	DRAM/$\overline{SR}$	I	This pin selects whether memory to be connected externally is DRAM or serial register. Low level : Serial register High level : DRAM
88	4B/$\overline{1B}$	I	This pin selects either 1-bit × type DRAM or 4-bit × type DRAM. Low level : 1-bit × type High level : 4-bit × type
79 78	A0 (SADY) A1 (SADX)	O	These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also connect to SAD pin of serial register and serial voice ROM at the time of serial register selection. These pins output leading addresses of read/write.
77	A2 ($\overline{TAS}$)	O	This pin connects to A2 of DRAM at the time of DRAM selection. It also connects to $\overline{TAS}$ pin of serial register and serial voice ROM at the time of serial register selection. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	A3 ($\overline{SAS}$)	O	This pin connects to A3 of DRAM at the time of DRAM selection. It also connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM at the time of serial register selection. Clock pin to write serial addresses.
75	A4 ($\overline{RWCK}$)	O	This pin connects to A4 of DRAM at the time of DRAM selection. It also connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM at the time of serial register selection. Clock pin to read data from and write data into the serial register.
1-6	A10-A5	O	This pin connects to pins A5-A10 of DRAM at the time of DRAM selection. This pin outputs addresses of read/write.

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>74</td><td>$\overline{WE}$</td><td>O</td><td>Write Enable. This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.</td></tr>
<tr><td>73</td><td>DI/O</td><td>I/O</td><td>Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data.</td></tr>
<tr><td>85</td><td>DROM</td><td>I</td><td>Data ROM. This pin connects to the DOUT pin of the serial voice ROM.</td></tr>
<tr><td>89</td><td>$\overline{RAS}$</td><td>O</td><td>This is a row address strobe pin of DRAM at the time of DRAM selection.</td></tr>
<tr><td>93-100</td><td>$\overline{CAS0}$-
$\overline{CAS7}$</td><td>O</td><td>These are the column address strobe pins of DRAM at the time of DRAM selection. $\overline{CAS7}$, an addresss output pin, is connected to pin A11 of DRAM at the time 16-Mbit DRAM selection.</td></tr>
<tr><td>81
82
83
84</td><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$
$\overline{CS4}$</td><td>O</td><td>Chip Select. These pins connect to $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.</td></tr>
<tr><td>58
59</td><td>MSEL1
MSEL2</td><td>I
I</td><td>These pins select the capacity of the memory to be connected externally.</td></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>These pins select the number of DRAMs and serial registers to be connected externallly.
• When DRAM is selected (DRAM/$\overline{SR}$ = High level)
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>1M × 4</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>1M × 8</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>1M × 4 + 4M × 1</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>4M × 2</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>4M × 3</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>4M × 4</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>16M × 1</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>4M × 6</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>4M × 6</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td><td>4M × 8</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>4M × 8</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>L</td><td>16M × 2</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>16M × 2</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>• When serial register is selected (DRAM/$\overline{SR}$ = Low level)
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>8M × 1</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>8M × 2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>8M × 3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>8M × 4</td></tr>
</table></td></tr>
<tr><td>87</td><td>LOWPWR</td><td>I</td><td>This pin selects $\overline{CAS}$-before-$\overline{RAS}$ refresh period of DRAM at the time of power down when DRAM is selected.
Low level : 15 µs max.
High level : 125 µs max.</td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789A to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{PDWN}$</td><td>I</td><td>Power Down. When a low level is input, the MSM6789A goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789A to be reset. When a Low level is applied to this pin during recording operation, the MSM6789A is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low level. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>91</td><td>XT</td><td>I</td><td>Oscillator Connection. When an external clock is used, input the clock through this pin. During the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>92</td><td>$\overline{XT}$</td><td>O</td><td>Oscillator Connection. When an external clock is used, this pin must be left open.</td></tr>
<tr><td>37
61</td><td>TEST
$\overline{TEST}$</td><td>I</td><td>MSM6789A Test. Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.</td></tr>
<tr><td>9-12
13-20
21</td><td>TMD3-TMD0
TDT7-TDT0
SYNC</td><td>I/O</td><td>MSM6789A Test. This pin must be left open.</td></tr>
<tr><td>17-20</td><td>TDT3-TDT0
[DQ4]-[DQ1]</td><td>I/O</td><td>Connect these pins to DQ1-DQ4 of DRAM at the time of 4-bit × type DRAM selection. Otherwise these pins must be left open as they are MSM6789A test pins.</td></tr>
<tr><td>22
23
8</td><td>TST
TCK
TMD4</td><td>I</td><td>MSM6789A Test. Input a low level signal.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>39</td><td>ROM</td><td>I</td><td>Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).</td></tr>
<tr><td>65</td><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Recording mode or playback mode selection. This pin is invalid during the ROM playback operation. When set to low, it selects the playback mode. When set to high, it selects the recording mode.</td></tr>
<tr><td>64</td><td>$\overline{\text{ST}}$</td><td>I</td><td>Start Playback. When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>63</td><td>$\overline{\text{SP}}$</td><td>I</td><td>Stop Playback.When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>32</td><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>Playback Pause. When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>31</td><td>$\overline{\text{DEL}}$</td><td>I</td><td>Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00:All phrase deletion
ch01 to ch3F:Specified phrase deletion
After power up, be sure to input a RESET signal and then delete all phrases.
After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>24-30</td><td>CA0-CA5</td><td>I</td><td>Desired Phrase Specification.
A total of 63 phrases can be specified indepedently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phrase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="6">A total of 63 phrases can be used for both record /playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>35
36</td><td>BR0
BR1</td><td>I</td><td>Bit Rate Selection. This pin selects one of the following three types of bit rate (master clock frequency f_{OSC} = 8.192 MHz). This pin is invalid during the ROM playback operation.
<table>
<tr><th>BR1</th><th>BR0</th><th>Bit rate</th></tr>
<tr><td>L</td><td>L</td><td>16.0 kbps</td></tr>
<tr><td>L</td><td>H</td><td>12.6 kbps</td></tr>
<tr><td>H</td><td>L</td><td>10.0 kbps</td></tr>
<tr><td>H</td><td>H</td><td>Unused</td></tr>
</table></td></tr>
<tr><td>33</td><td>PDMD*1</td><td>I</td><td>Transition to the Power-down State.
Low level: The MSM6789A automatically goes to the power-down state, except when the record/playback operation is performed.
High level: The MSM6789A automatically goes to the standby state, instead of the power-down state, except when the record/playback operation is performed. In this case, the MSM6789A can be placed in the power-down state by setting the RESET or PDWN pin to a high level. If an external circuit is used for the built-in LPF, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>67-70</td><td>VD0-VD3</td><td>I</td><td>These pins set the voice detect level for the voice triggered starting and unvoiced-part elimination.</td></tr>
<tr><td>38</td><td>VDS</td><td>I</td><td>This pin selects the voice triggered starting or the unvoiced-part elimination.
Voice triggered starting: Input a High level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Unvoiced-part elimination: Input a Low level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Note: When neither the voice triggered starting nor the unvoiced-part elimination is used, input a Low level to VD0 to VD3.</td></tr>
<tr><td>72</td><td>MON</td><td>O</td><td>This pin outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>71</td><td>NAR</td><td>O</td><td>Output to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after the NAR pin goes to high positively.</td></tr>
</table>

*1 When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*4	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5 V*4
DGND=AGND=0 V, Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=–40 µA	V_{DD}–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current *1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current *2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input currcent *1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low input current *2	I_{IL2}	V_{IL}=GND	–20	—	—	µA
Low input current *3	I_{IL3}	V_{IL}=GND	–400	—	–20	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

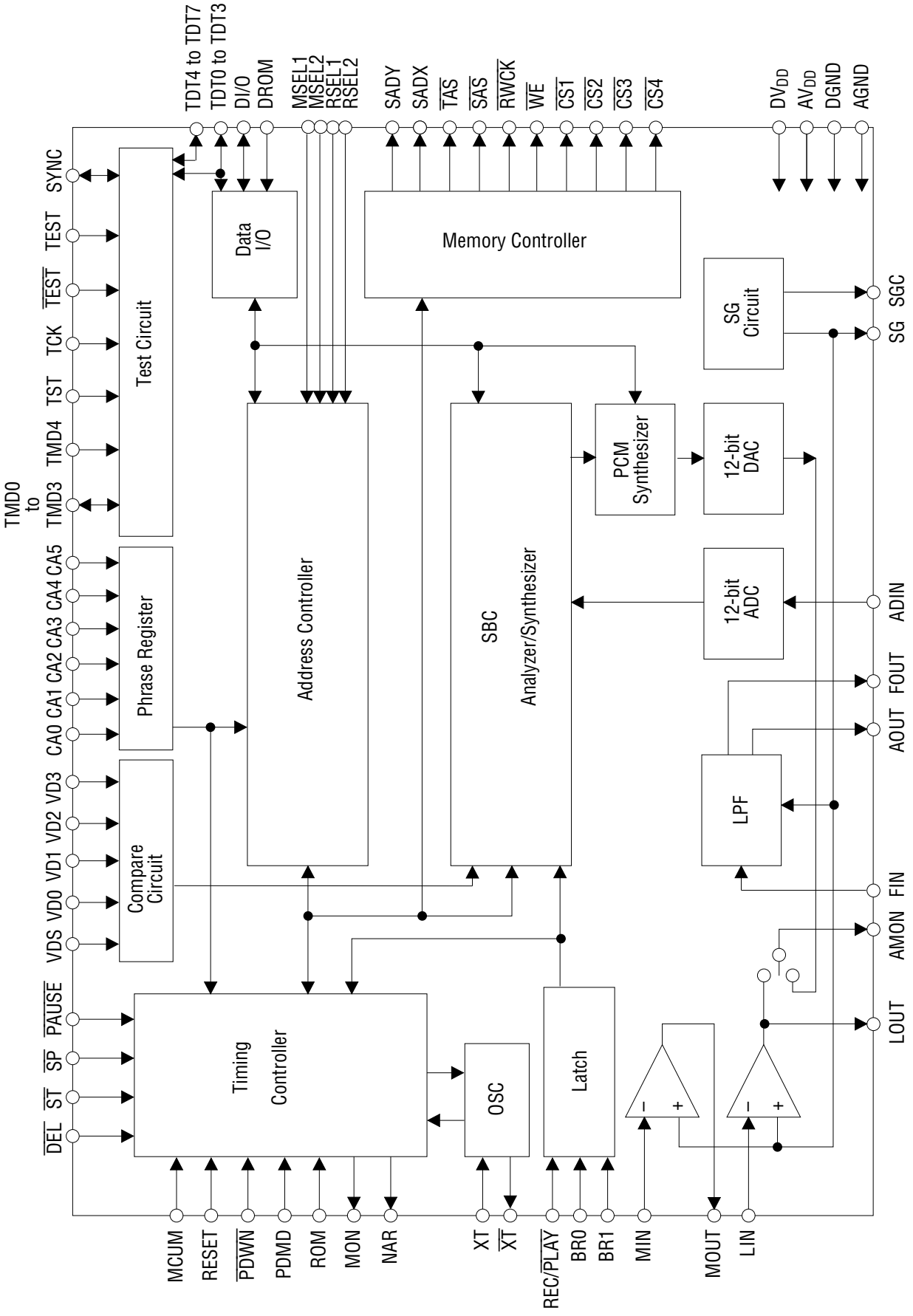
*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.
*3 Applies to the input pins with pull-up resistor ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) excluding the XT pin.
*4 The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

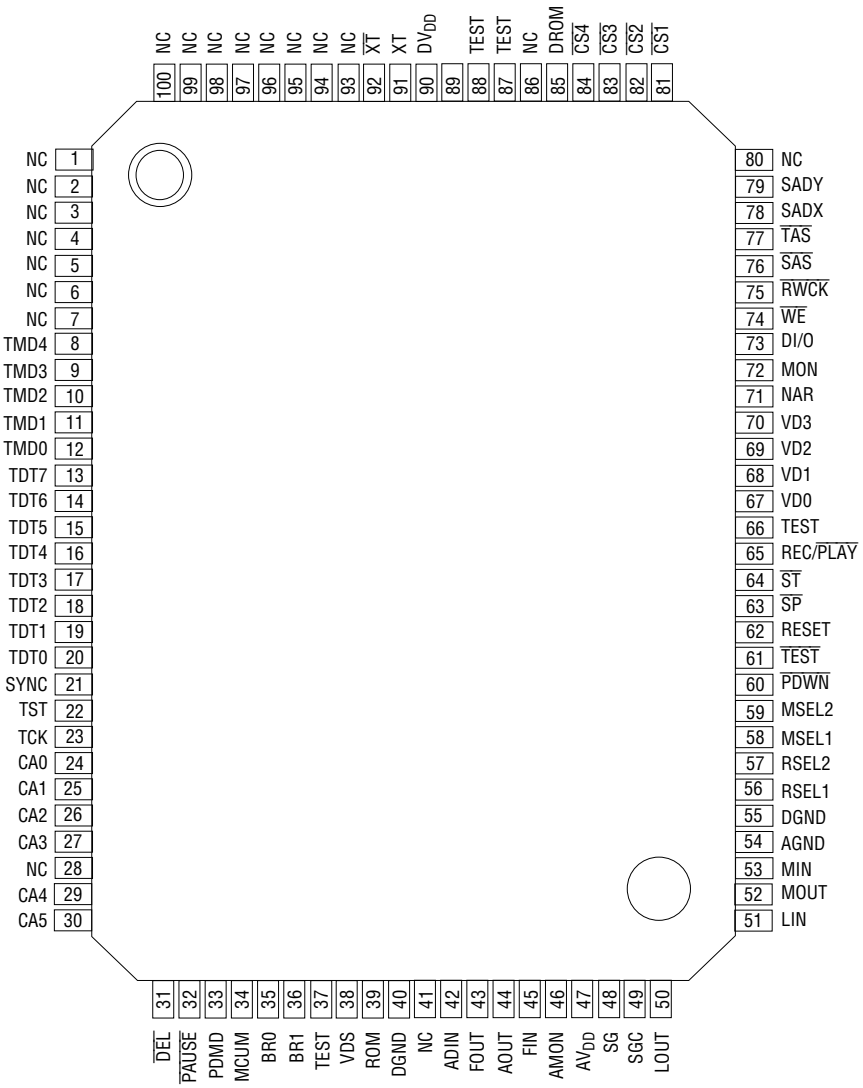
$DV_{DD}=AV_{DD}=4.5$ to 5.5 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	$V_{DD}-1$	V
FIN input impedance	R_{FIN}	—	1	—	—	M Ω
Op-map open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	M Ω
Op-amp load resistance	R_{OUTA}	—	200	—	—	k Ω
AOUT load resistance	R_{AOUT}	—	50	—	—	k Ω
FOUT load resistance	R_{FOUT}	—	50	—	—	k Ω

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3 V Version))



100-Pin Plastic QFP

NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1 μF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1 μF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	—	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
79 78	SADY SADX	O	They also connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write.
77	$\overline{TAS}$	O	This pin connects to $\overline{TAS}$ pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	$\overline{SAS}$	O	This pin connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM. Clock pin to write serial addresses.
75	$\overline{RWCK}$	O	This pin connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM. Clock pin to read data from and write data into the serial register.
74	$\overline{WE}$	O	**Write Enable.** This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	I/O	**Data I/O.** This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin outputs write data and inputs read data.
85	DROM	I	**Data ROM.** This pin connects to the DOUT pin of the serial voice ROM.
81 82 83 84	$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	**Chip Select.** These pins connect to $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>58
59</td><td>MSEL1
MSEL2</td><td>I
I</td><td>These pins select the capacity of the memory to be connected externally.</td></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>These pins select the number of and serial registers to be connected externallly.
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
</table></td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789L to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{\text{PDWN}}$</td><td>I</td><td>Power Down. When a low level is input, the MSM6789L goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789L to be reset. When a Low level is applied to this pin during recording operation, the MSM6789L is halted, and will be maintained in the power down state while $\overline{\text{PDWN}}$ is low level. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>91</td><td>XT</td><td>I</td><td>Oscillator Connection. When an external clock is used, input the clock through this pin. During the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>92</td><td>$\overline{\text{XT}}$</td><td>O</td><td>Oscillator Connection. When an external clock is used, this pin must be left open.</td></tr>
<tr><td>37
61</td><td>TEST
$\overline{\text{TEST}}$</td><td>I</td><td>MSM6789L Test. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.</td></tr>
<tr><td>9-12
13-20
21</td><td>TMD3-TMD0
TDT7-TDT0
SYNC</td><td>I/O</td><td>MSM6789L Test. This pin must be left open.</td></tr>
<tr><td>17-20</td><td>TDT3-TDT0</td><td>I/O</td><td>These pins must be left open as they are MSM6789L test pins.</td></tr>
<tr><td>22
23
8</td><td>TST
TCK
TMD4</td><td>I</td><td>MSM6789L Test. Input a low level signal.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>39</td><td>ROM</td><td>I</td><td>Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).</td></tr>
<tr><td>65</td><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Recording mode or playback mode selection. This pin is invalid during the ROM playback operation. When set to low, it selects the playback mode. When set to high, it selects the recording mode.</td></tr>
<tr><td>64</td><td>$\overline{\text{ST}}$</td><td>I</td><td>Start Playback. When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>63</td><td>$\overline{\text{SP}}$</td><td>I</td><td>Stop Playback.When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>32</td><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>Playback Pause. When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>31</td><td>$\overline{\text{DEL}}$</td><td>I</td><td>Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00:All phrase deletion
ch01 to ch3F:Specified phrase deletion
After power up, be sure to input a RESET signal and then delete all phrases.
After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>24-30</td><td>CA0-CA5</td><td>I</td><td>Desired Phrase Specification.
A total of 63 phrases can be specified indepedently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phrase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="6">A total of 63 phrases can be used for both record /playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>35
36</td><td>BR0
BR1</td><td>I</td><td>Bit Rate Selection. This pin selects one of the following three types of bit rate (master clock frequency f_{OSC} = 8.192 MHz). This pin is invalid during the ROM playback operation.
<table>
<tr><th>BR1</th><th>BR0</th><th>Bit rate</th></tr>
<tr><td>L</td><td>L</td><td>16.0 kbps</td></tr>
<tr><td>L</td><td>H</td><td>12.6 kbps</td></tr>
<tr><td>H</td><td>L</td><td>10.0 kbps</td></tr>
<tr><td>H</td><td>H</td><td>Unused</td></tr>
</table></td></tr>
<tr><td>33</td><td>PDMD*1</td><td>I</td><td>Transition to the Power-down State.
Low level: The MSM6789L automatically goes to the power-down state, except when the record/playback operation is performed.
High level: The MSM6789L automatically goes to the standby state, instead of the power-down state, except when the record/playback operation is performed. In this case, the MSM6789L can be placed in the power-down state by setting the RESET or PDWN pin to a high level. If an external circuit is used for the built-in LPF, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>67-70</td><td>VD0-VD3</td><td>I</td><td>These pins set the voice detect level for the voice triggered starting and unvoiced-part elimination.</td></tr>
<tr><td>38</td><td>VDS</td><td>I</td><td>This pin selects the voice triggered starting or the unvoiced-part elimination.
Voice triggered starting: Input a High level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Unvoiced-part elimination: Input a Low level to the VDS pin. Then set the voice detect level with VD0 to VD3 pins.
Note: When neither the voice triggered starting nor the unvoiced-part elimination is used, input a Low level to VD0 to VD3.</td></tr>
<tr><td>72</td><td>MON</td><td>O</td><td>This pin outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>71</td><td>NAR</td><td>O</td><td>Output to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after the NAR pin goes to high positively.</td></tr>
</table>

*1 When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V
DGND=AGND=0 V, Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.85×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.15×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=–40 µA	V_{DD}–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current *1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current *2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input currcent *1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low input current *2	I_{IL2}	V_{IL}=GND	–20	—	—	µA
Low input current *3	I_{IL3}	V_{IL}=GND	–400	—	–20	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.
*3 Applies to the input pins with pull-up resistor ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) excluding the XT pin.

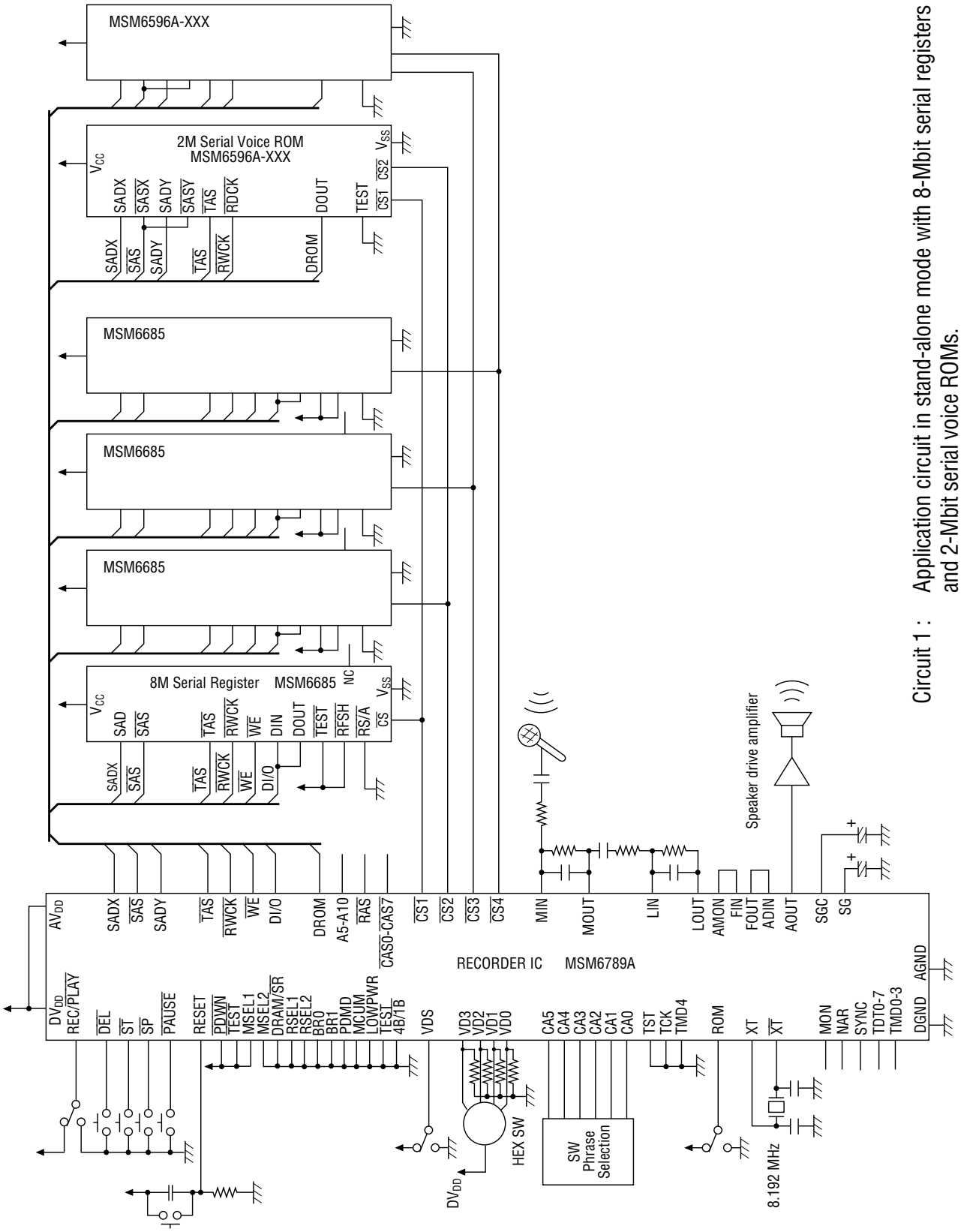
Analog Characteristics

$DV_{DD}=AV_{DD}=3.0$ to 3.6 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	no load	—	—	20	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	V_{DD}–1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-map open loop gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	400	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	100	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	100	—	—	kΩ

APPLICATION CIRCUITS (for MSM6789A (5 V version))

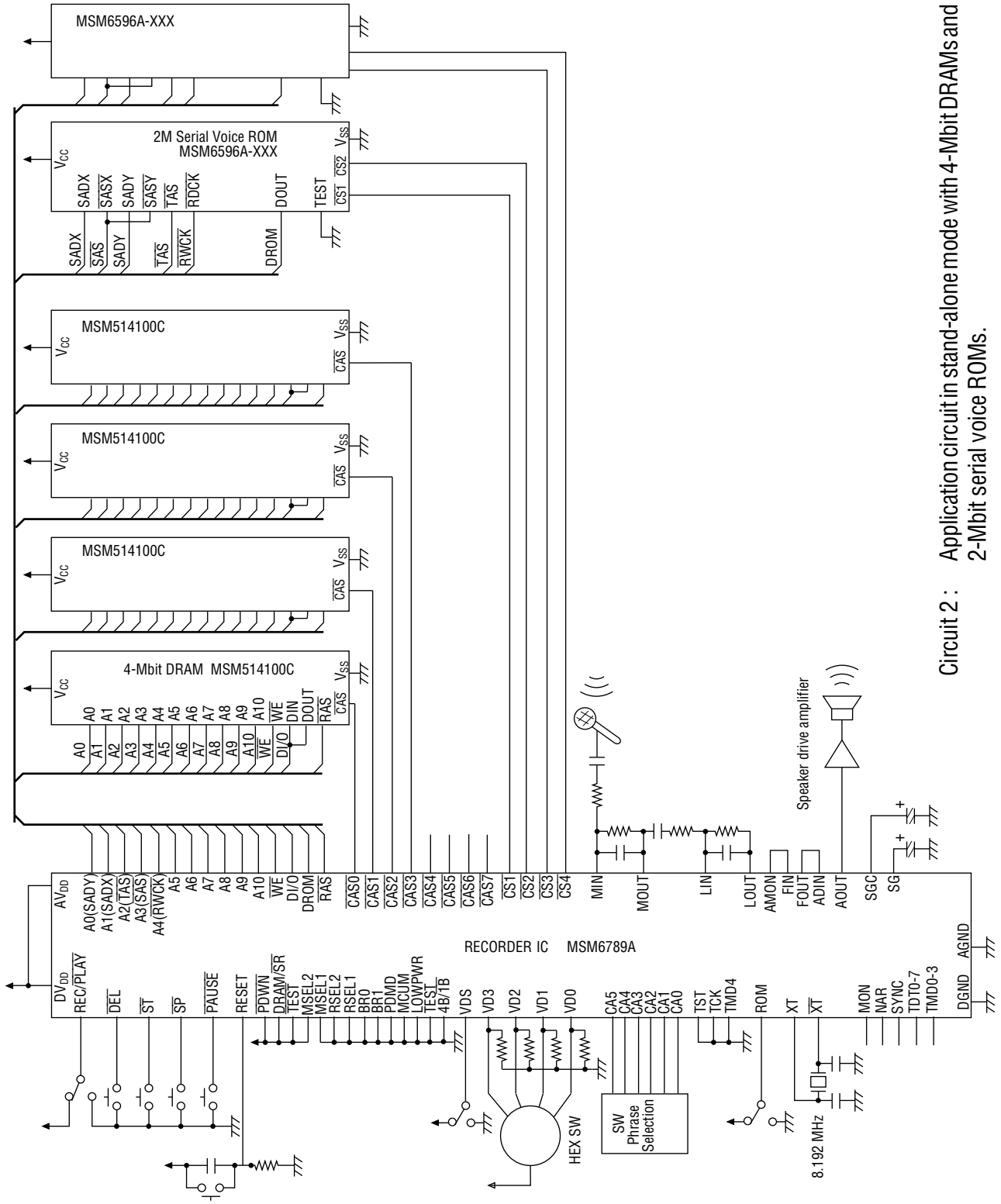
This is an application circuit example when the MSM6789A is used in stand-alone mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.



Circuit 1 : Application circuit in stand-alone mode with 8-Mbit serial registers and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

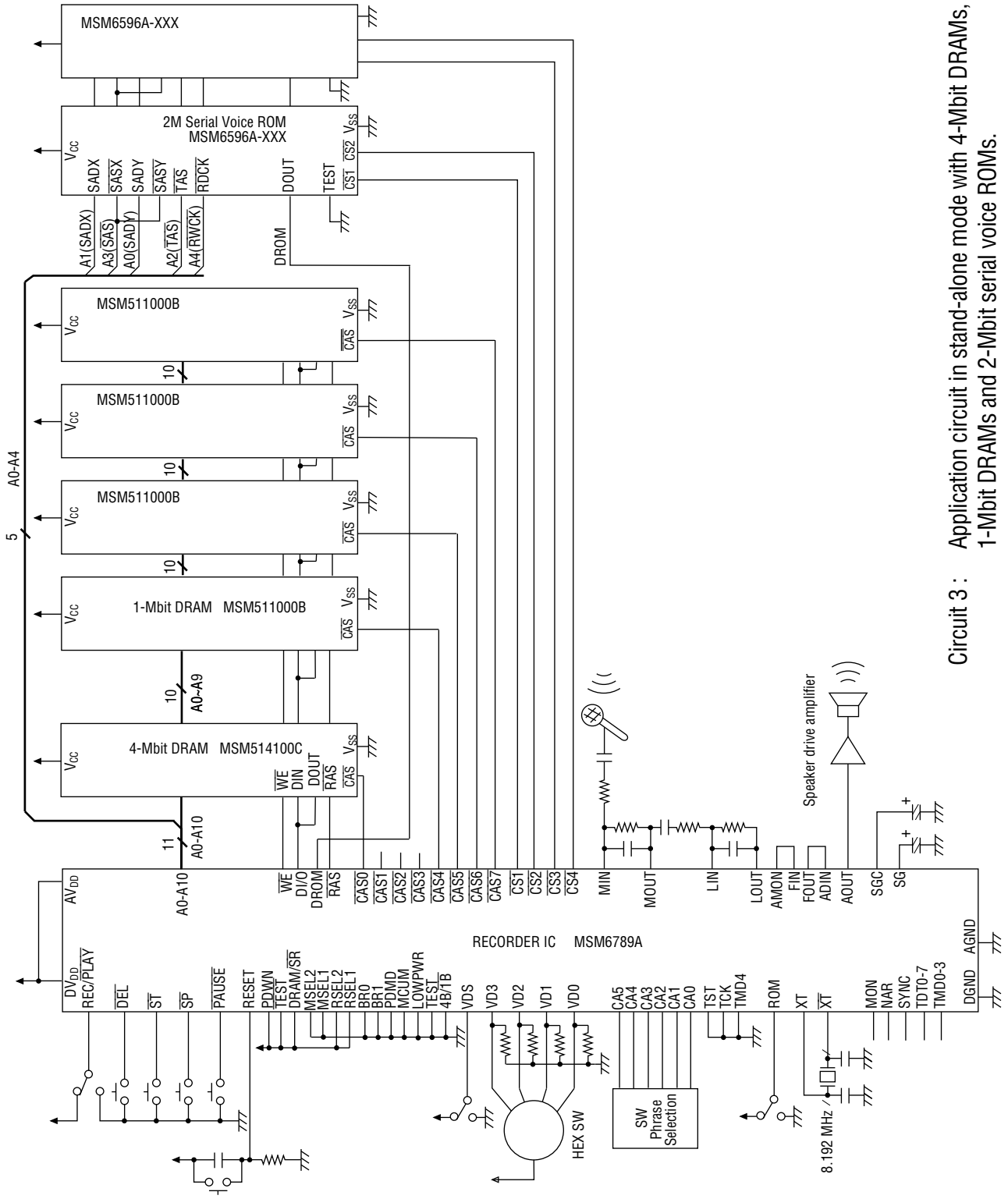
This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 2 : Application circuit in stand-alone mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

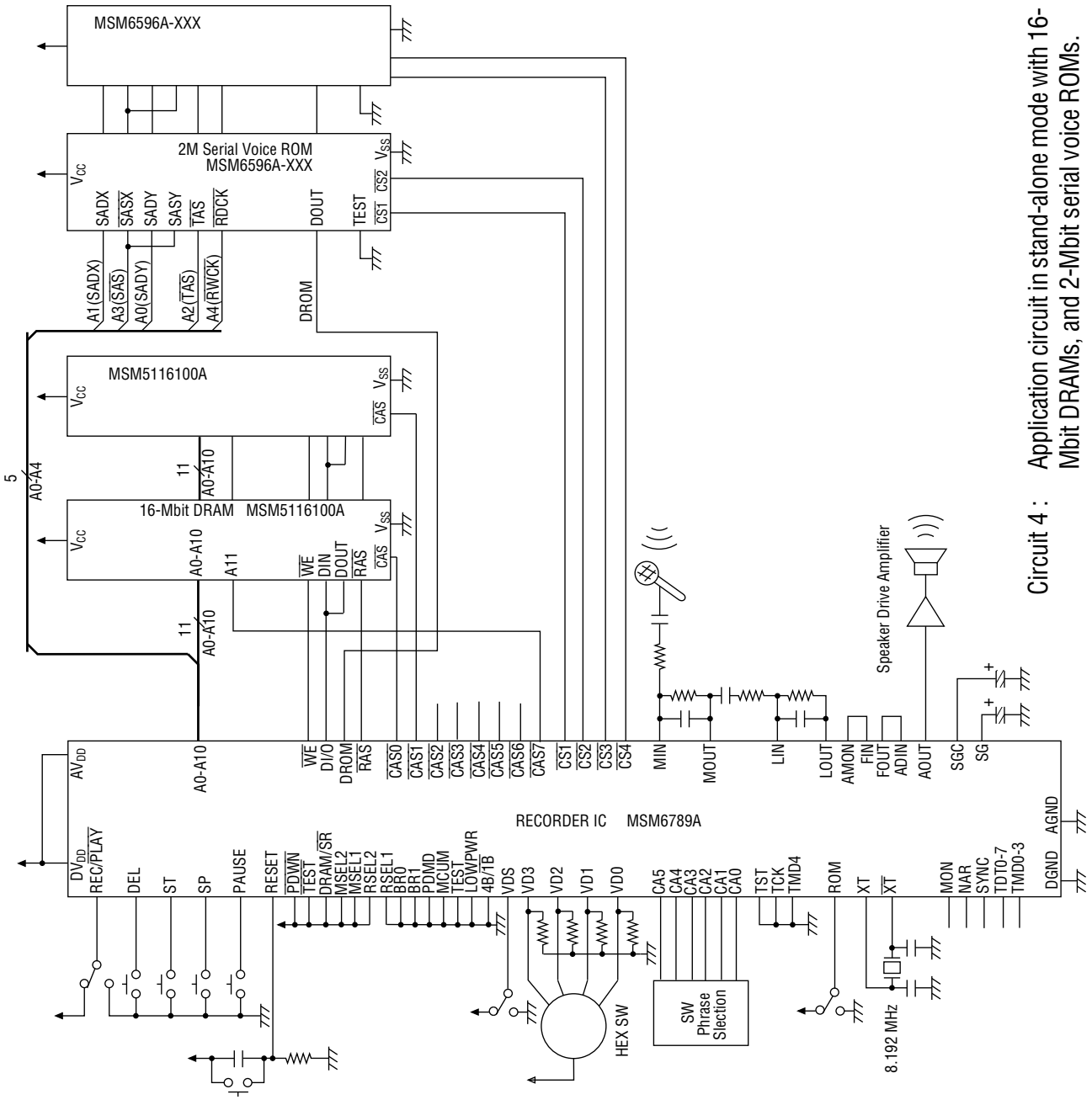
This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 3 : Application circuit in stand-alone mode with 4-Mbit DRAMs, 1-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

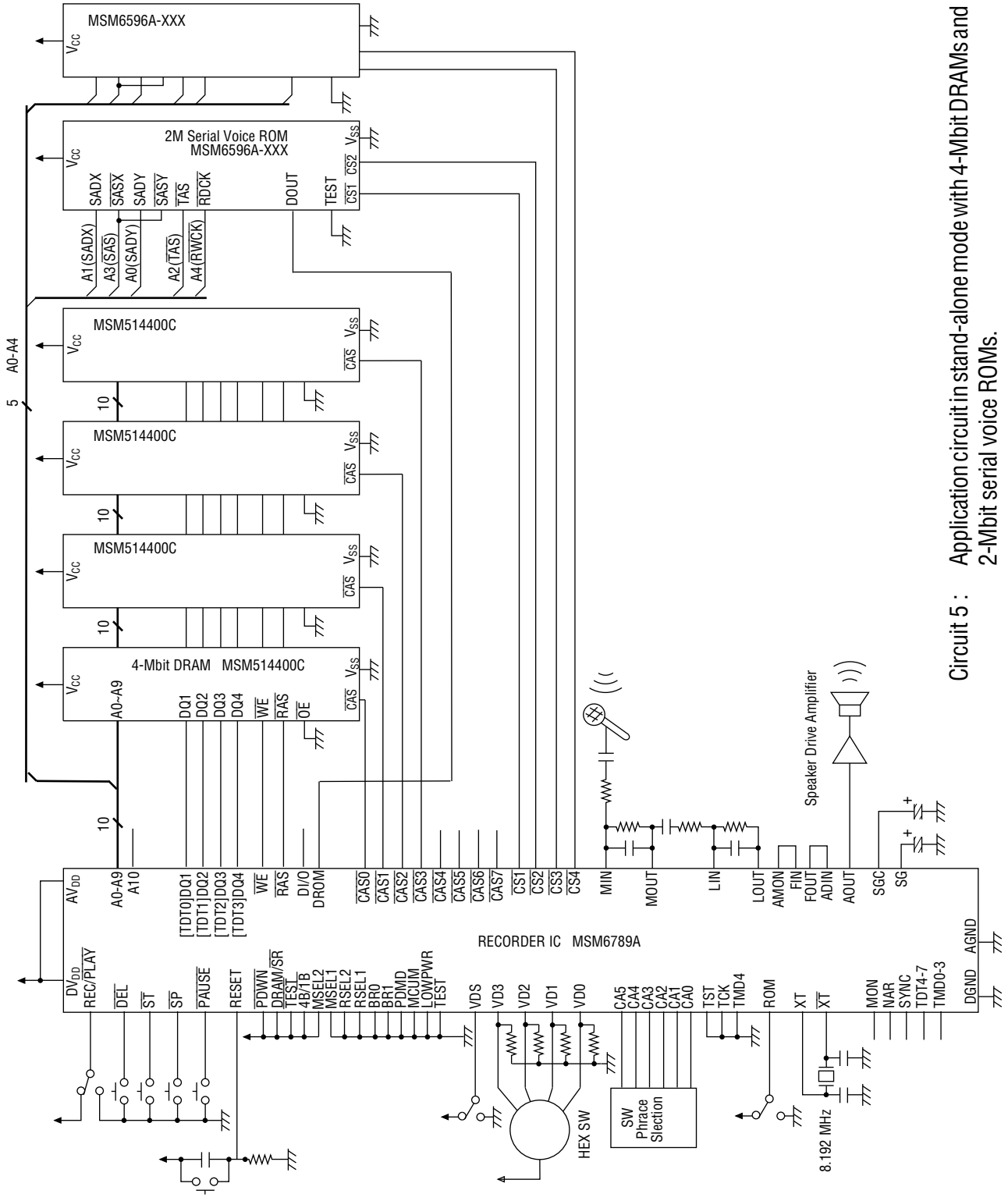
This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 4 : Application circuit in stand-alone mode with 16-Mbit DRAMs, and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

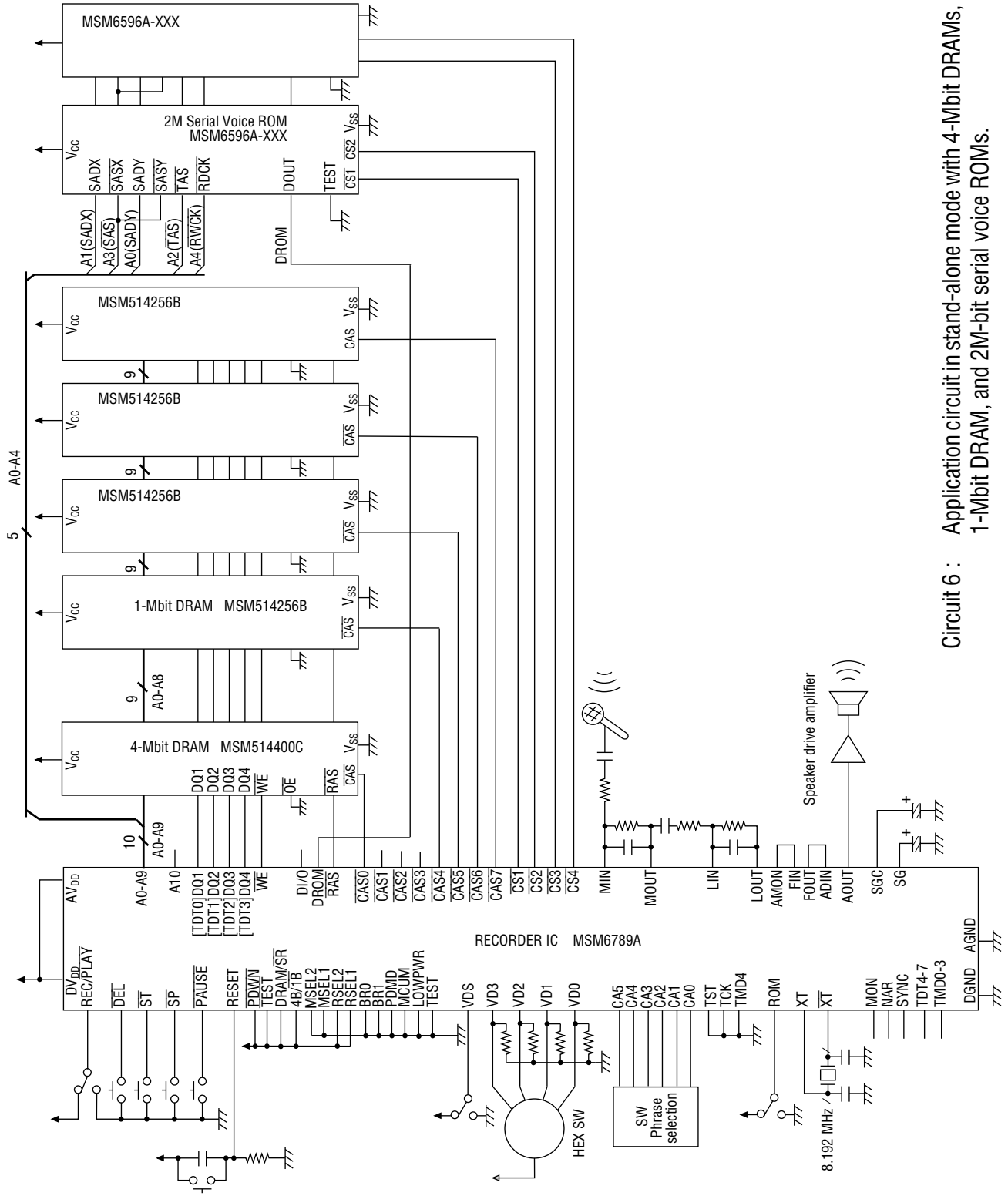
This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 5 : Application circuit in stand-alone mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

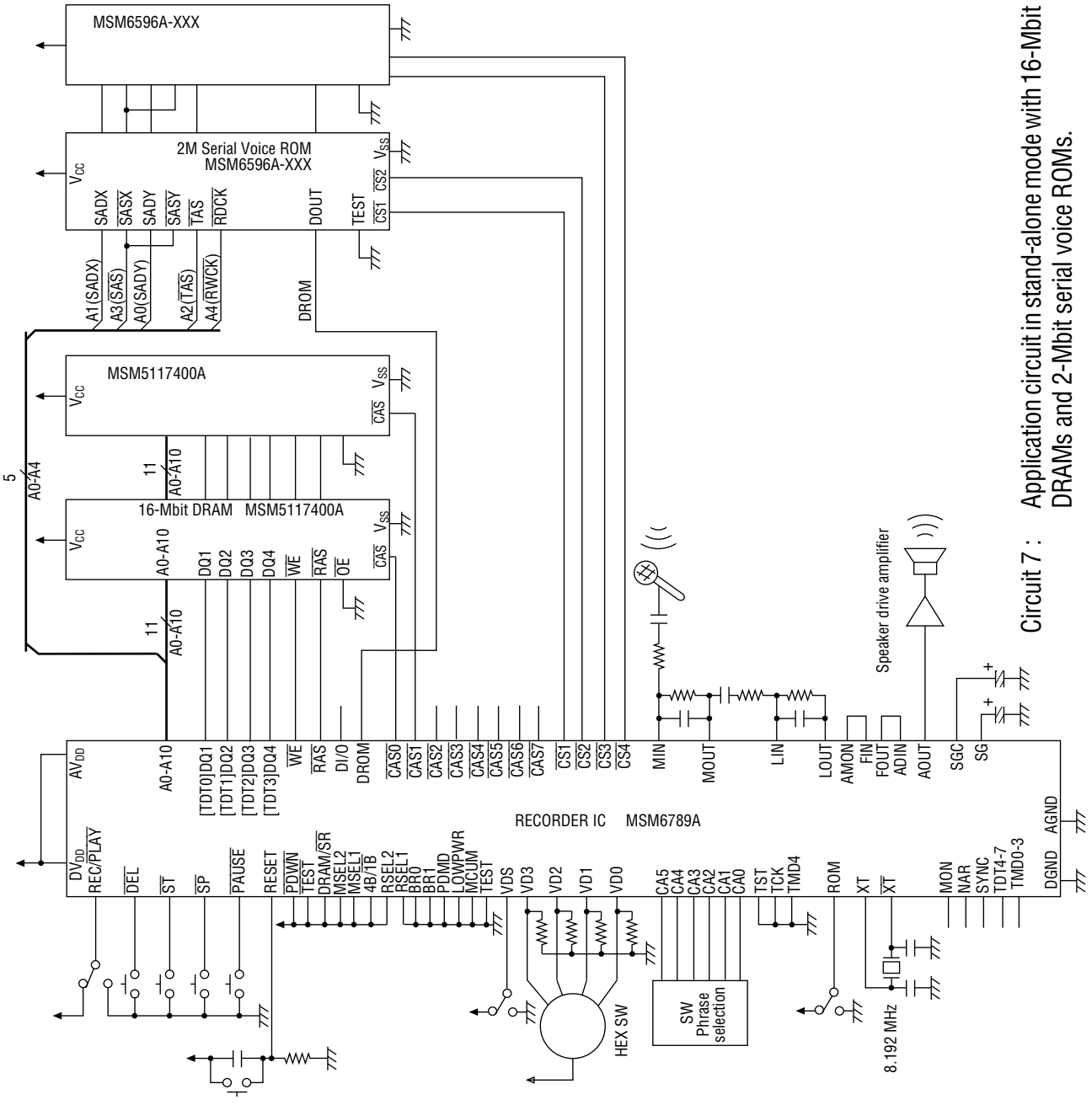
This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.



Circuit 6 : Application circuit in stand-alone mode with 4-Mbit DRAMs, 1-Mbit DRAM, and 2M-bit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

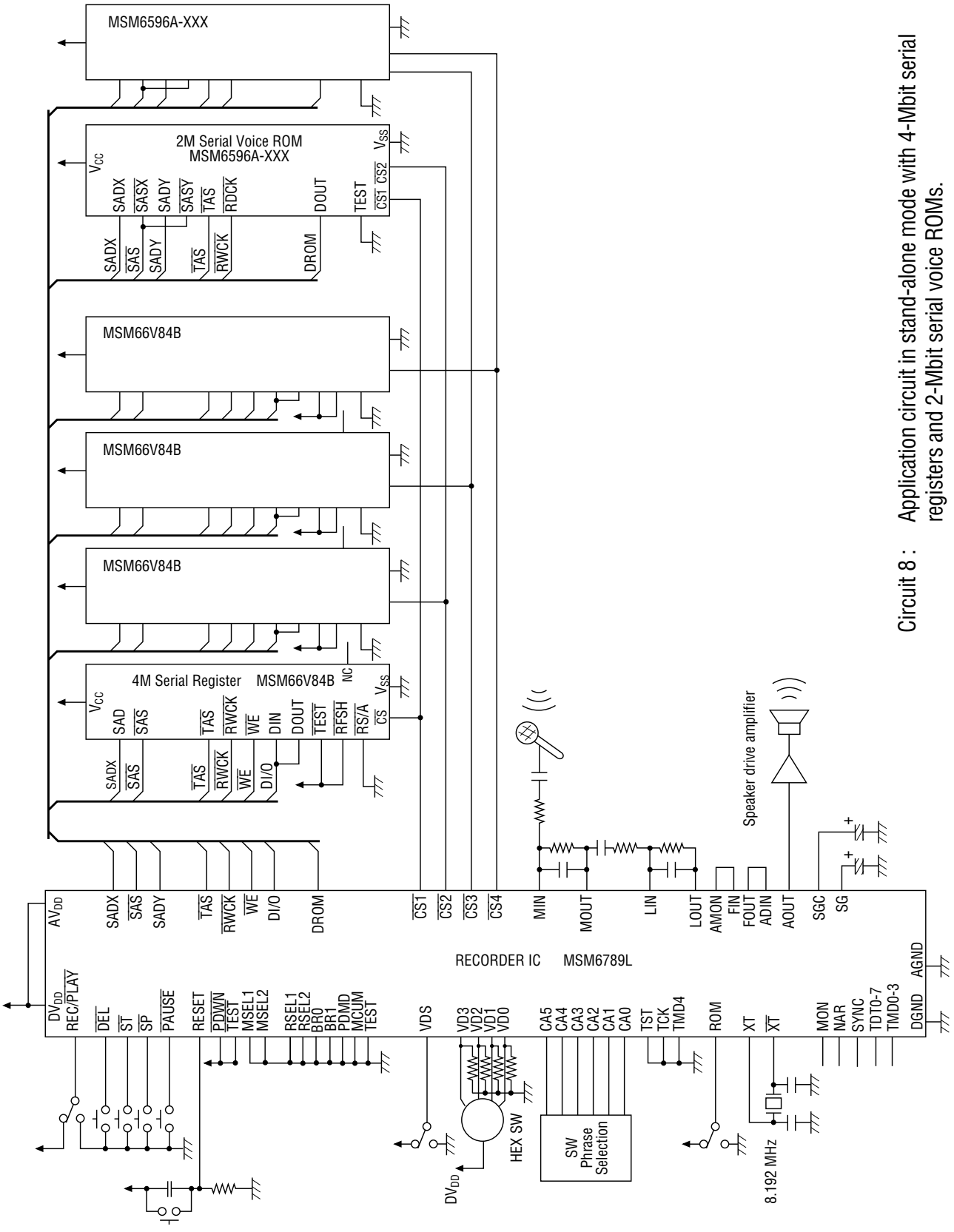
This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 7 : Application circuit in stand-alone mode with 16-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in stand-alone mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.



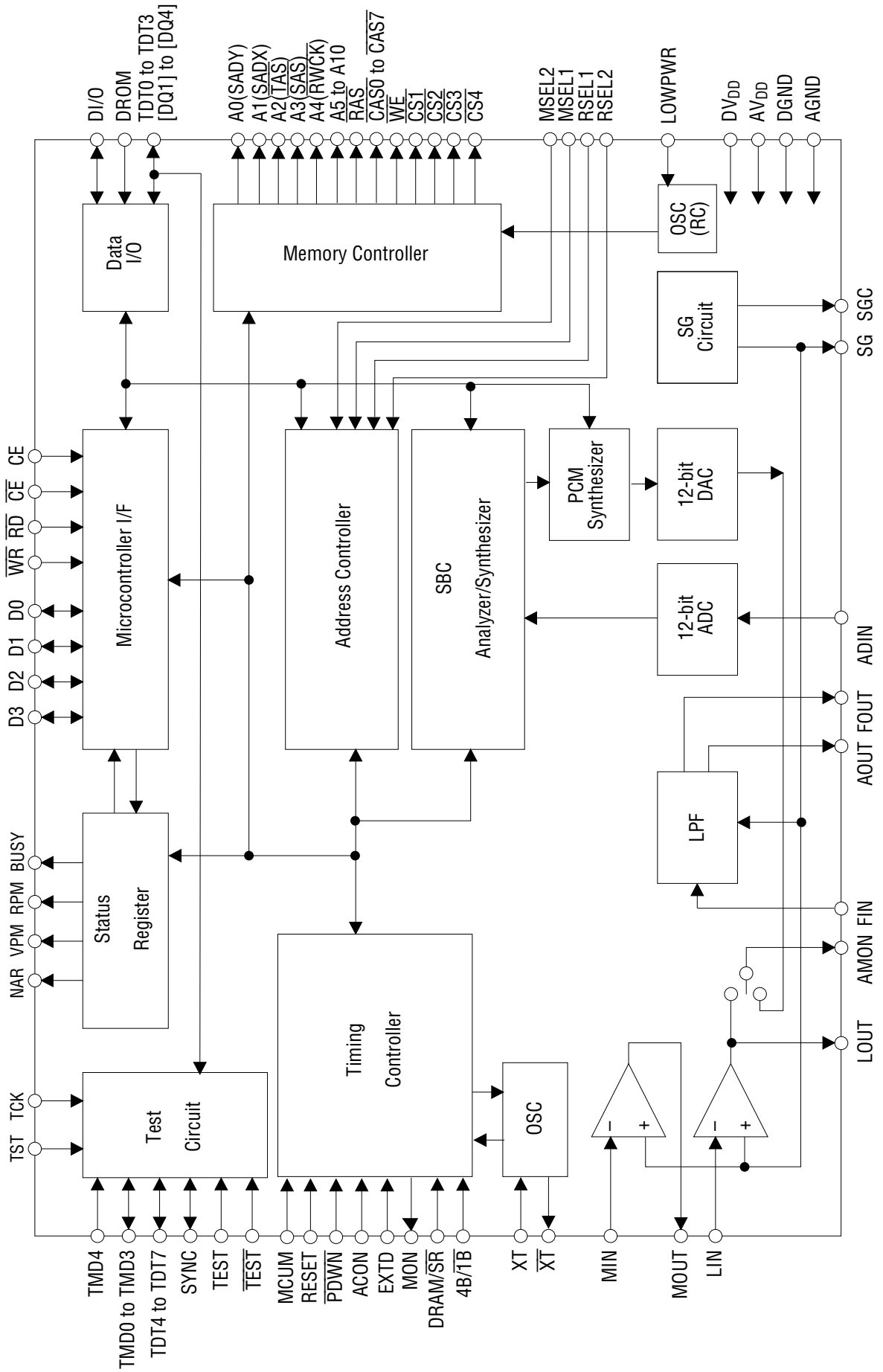
Circuit 8 : Application circuit in stand-alone mode with 4-Mbit serial registers and 2-Mbit serial voice ROMs.

MICROCONTROLLER INTERFACE MODE

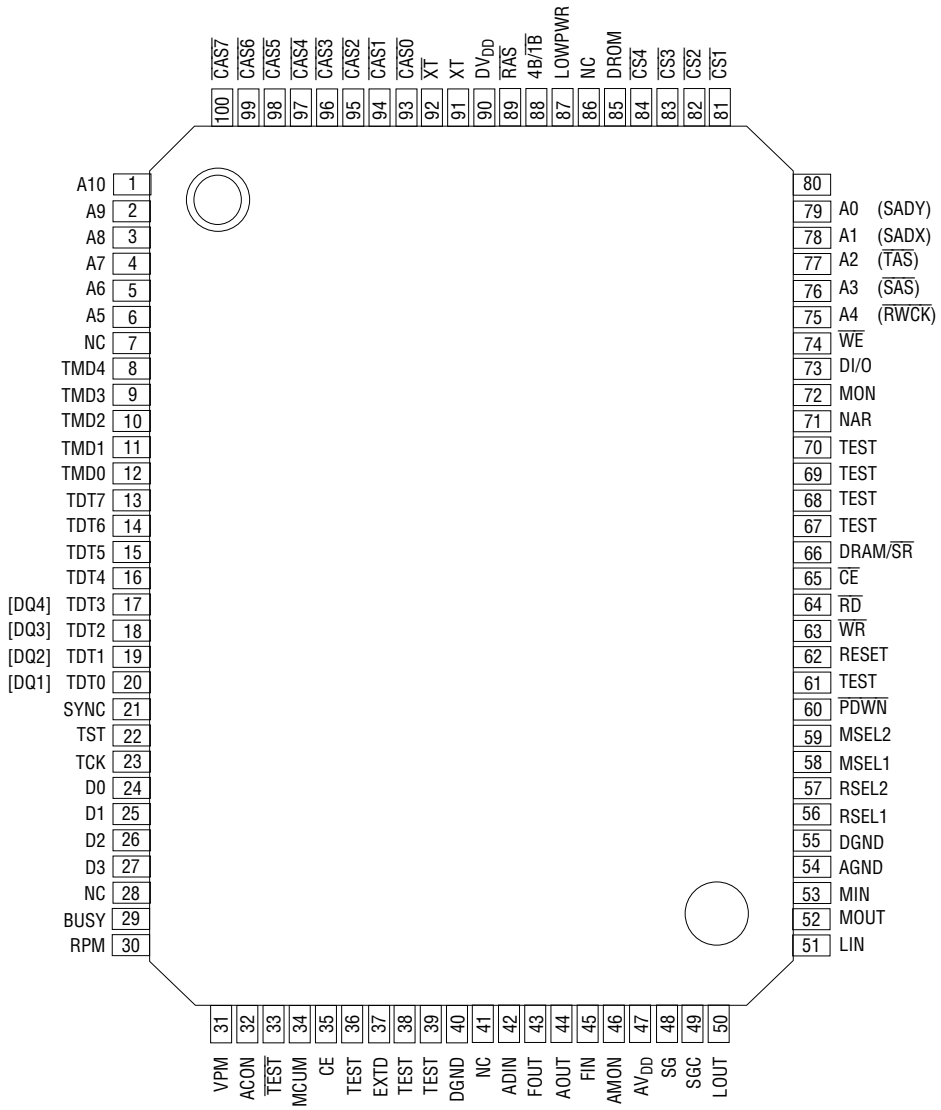
FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  MSM6789A (5 V version)
    General-purpose DRAM, 32 Mbits maximum (for variable messages)
      1-Mbit DRAM : Can be directly driven (MSM514256B, MSM511000B)
      4-Mbit DRAM : Can be directly driven (MSM514400C, MSM514100C)
      16-Mbit DRAM : Can be directly driven (MSM5117400A, MSM5116100A)
    ARAM, 32 Mbits maximum (for variable messages)
      Note: Use the first 64 Kbits with no failed bits for the ARAM.
    Serial register, 32 Mbits maximum (for variable messages)
      4-Mbit serial register : Can be directly driven (MSM6684B)
      8-Mbit serial register : Can be directly driven (MSM6685)
  MSM6789L (3.3 V version)
    Serial register, 16 Mbits maximum (for variable messages)
      4-Mbit serial register: Can be directly driven (MSM66V84B)
  MSM6789A (5 V version) and MSM6789L (3.3 V version)
    Serial voice ROM, 4 Mbits maximum (for fixed messages)
      1-Mbit serial voice ROM : Can be directly driven (MSM6595A)
      2-Mbit serial voice ROM : Can be directly driven (MSM6596A)
      3-Mbit serial voice ROM : Can be directly driven (MSM6597A)
- Bit rate
  10.0, 12.6, 16.0 kbps (at 8 kHz sampling freq.)
  7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)
- Maximum recording time (when one 8-Mbit serial register is connected)
  13.8 minutes (for 10.0 kbps SBC) 18.4 minutes (for 7.5 kbps SBC)
  11.0 minutes (for 12.6 kbps SBC) 14.6 minutes (for 9.5 kbps SBC)
  8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)
- Number of phrases
  63 phrases for variable messages
  255 phrases for fixed messages
- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Uuvoiced-part elimination function (voice detect level can be set)
- Pausing function
- Master clock frequency: 6.0 MHz to 8.192 MHz
- Power supply voltage:
    MSM6789A: Single 5 V power supply
    MSM6789L: Single 3.3 V power supply
- Package options:
    MSM6789A: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK)
    MSM6789L: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

( ) : Pins for connecting serial voice ROM.
[ ] : Pins for connecting 4-bit × type DRAM.
NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	O	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
66	DRAM/$\overline{SR}$	I	This pin selects whether memory to be connected externally is DRAM or serial register. Low level : Serial register High level : DRAM
88	4B/$\overline{1B}$	I	This pin selects either 1-bit × type DRAM or 4-bit × type DRAM. Low level : 1-bit × type High level : 4-bit × type
79 78	A0 (SADY) A1 (SADX)	O	These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also connect to SAD pin of serial register and serial voice ROM at the time of serial register selection. These pins output leading addresses of read/write.
77	A2 ($\overline{TAS}$)	O	This pin connects to A2 of DRAM at the time of DRAM selection. It also connects to $\overline{TAS}$ pin of serial register and serial voice ROM at the time of serial register selection. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	A3 ($\overline{SAS}$)	O	This pin connects to A3 of DRAM at the time of DRAM selection. It also connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM at the time of serial register selection. Clock pin to write serial addresses.
75	A4 ($\overline{RWCK}$)	O	This pin connects to A4 of DRAM at the time of DRAM selection. It also connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM at the time of serial register selection. Clock pin to read data from and write data into the serial register.
1-6	A10-A5	O	These pins connect to pins A5-A10 of DRAM at the time of DRAM selection. These pins output addresses of read/write.

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>74</td><td>$\overline{WE}$</td><td>O</td><td>Write Enable. This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.</td></tr>
<tr><td>73</td><td>DI/O</td><td>I/O</td><td>Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin is used to output write data and inputs read data.</td></tr>
<tr><td>85</td><td>DROM</td><td>I</td><td>Data ROM. This pin connects to the DOUT pin of the serial voice ROM.</td></tr>
<tr><td>89</td><td>$\overline{RAS}$</td><td>O</td><td>This is a row address strobe pin of DRAM at the time of DRAM selection.</td></tr>
<tr><td>93-100</td><td>$\overline{CAS0}$-
$\overline{CAS7}$</td><td>O</td><td>These are the column address strobe pins of DRAM at the time of DRAM selection. CAS7, an addresss output pin, is connected to pin A11 of DRAM at the time of 16-Mbit DRAM selection.</td></tr>
<tr><td>81
82
83
84</td><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$
$\overline{CS4}$</td><td>O</td><td>Chip Slect. These pins connect $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.</td></tr>
<tr><td>58
59</td><td>MSEL1
MSEL2</td><td>I
I</td><td>These pins select the capacity of the memory to be connected externally.</td></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>These pins select the number of DRAMs and serial registers to be connected externallly.
When DRAM is selected (DRAM/$\overline{SR}$ = High level)
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>1M × 4</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>1M × 8</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>1M × 4 + 4M × 1</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>4M × 2</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>4M × 3</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>4M × 4</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>16M × 1</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>4M × 6</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>4M × 6</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td><td>4M × 8</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>4M × 8</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>L</td><td>16M × 2</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>16M × 2</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>• When serial register is selected (DRAM/$\overline{SR}$ = Low level)
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M × 1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M × 2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M × 3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M × 4</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>8M × 1</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>8M × 2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>8M × 3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>8M × 4</td></tr>
</table></td></tr>
<tr><td>87</td><td>LOWPWR</td><td>I</td><td>This pin selects $\overline{CAS}$-before-$\overline{RAS}$ refresh period of DRAM at the time of power down when DRAM is selected.
Low level : 15 µs max.
High level : 125 µs max.</td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789A to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{PDWN}$</td><td>I</td><td>Power Down. When a low level is input the MSM6789A goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789A to be reset.
When an Low level is applied to this pin during recording operation, the MSM6789A is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low level.
After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>24
25
26
27</td><td>D0
D1
D2
D3</td><td>I/O</td><td>Bidirectional data bus to transfer commands and data to and from an external microcontroller.</td></tr>
<tr><td>63</td><td>$\overline{WR}$</td><td>I</td><td>Write Pulse Input. Inputting a low pulse to $\overline{WR}$ pin causes a command or data to be input via D0 to D3 pins.</td></tr>
<tr><td>64</td><td>$\overline{RD}$</td><td>I</td><td>Read Pulse Input. Inputting a low pulse to $\overline{RD}$ pin causes status bits or data to be output via D0 to D3 pins.</td></tr>
<tr><td>65
35</td><td>$\overline{CE}$
CE</td><td>I</td><td>Chip Enable Input. When the $\overline{CE}$ pin is set to low level and the CE pin is set to a high level, the write pulse ($\overline{WR}$) or read pulse ($\overline{RD}$) can be accepted.
When the $\overline{CE}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{WR}$) and read pulse ($\overline{RD}$) cannot be accepted so that data cannot be communicated via D0 to D3 pins.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789A (5 V Version)) (Continued)

Pin	Symbol	Type	Description
29	BUSY	O	**Busy.** This pin outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0 to D3 pins. The state of this pin is the same as the contents of the BUSY bit of the status register.
30	RPM	O	**RPM.** This pin outputs a high level during recording or playback operation. The state of this pin is the same as the contents of the RPM bit of the status register.
31	VPM	O	**VPM.** This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	O	**NAR.** This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	**POP Noise Suppression Select.** This pin selects whether the pop noise suppression circuit is used. Low level : the pop noise suppression circuit is not used. High level : the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	**EXTD.** In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	**Oscillator Connect.** When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	$\overline{XT}$	O	**Oscillator Connect.** When an external clock is uesd, this pin must be left open.
72	MON	O	**MON.** This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70 33	TEST $\overline{TEST}$	I	**MSM6789A Test.** Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.
9-12 13-20 21	TMD3-TMD0 TDT7-TDT0 SYNC	I/O	**MSM6789A Test.** This pin must be left open.
17-20	TDT3-TDT0 [DQ4]-[DQ1]	I/O	Connect these pins to DQ1 to DQ4 of DRAM at the time of 4-bit × type DRAM selection. Otherwise these pins must be left open as they are MSM6789A test pins.
22 23 8	TST TCK TMD4	I	**MSM6789A Test.** Input a low level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	–0.3 ~ V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*3	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5 V*3
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=–40 µA	V_{DD}–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current*1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current*2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input current*1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low input current*2	I_{IL2}	V_{IL}=GND	–20	—	—	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

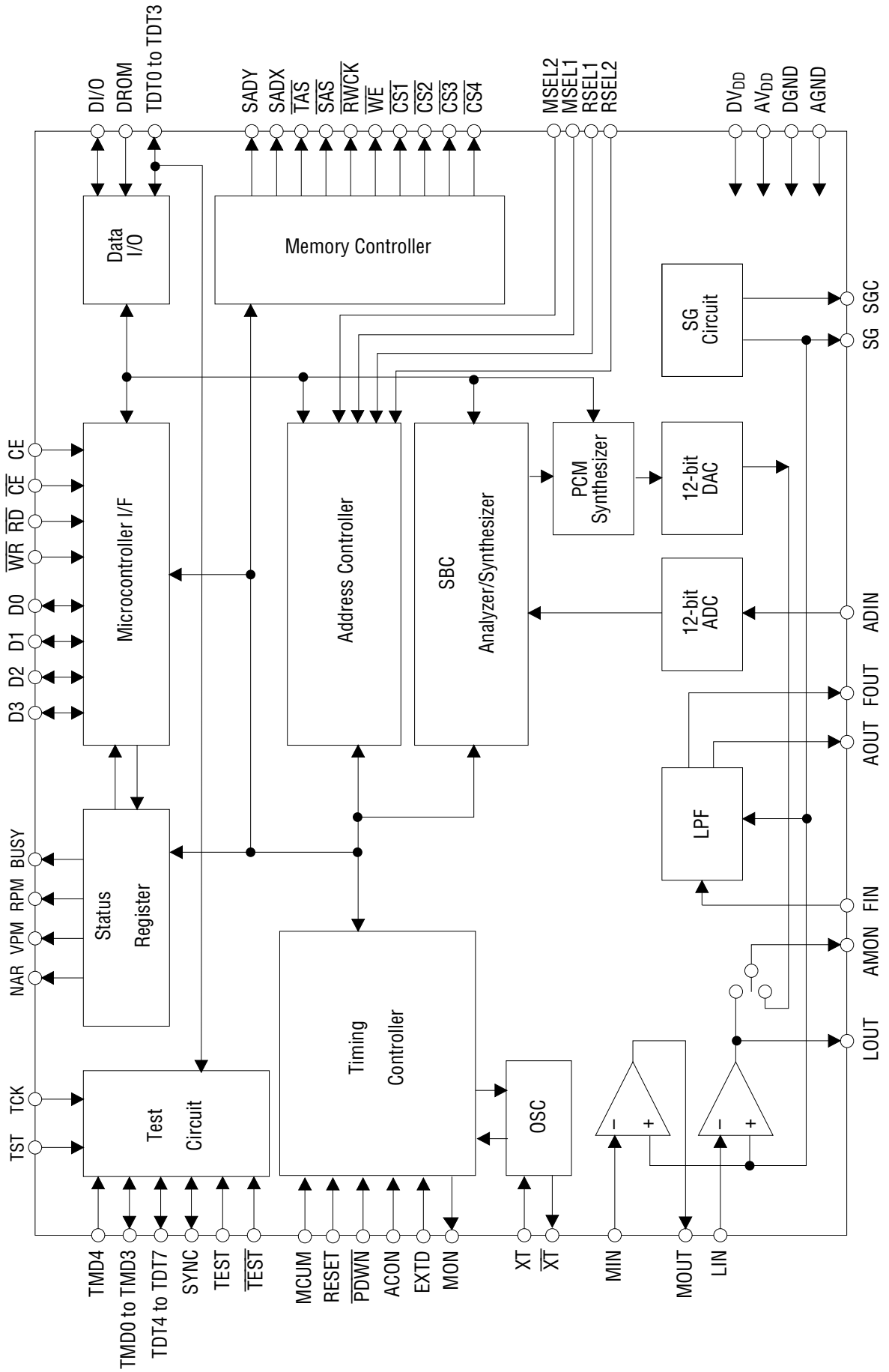
*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.
*3 The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

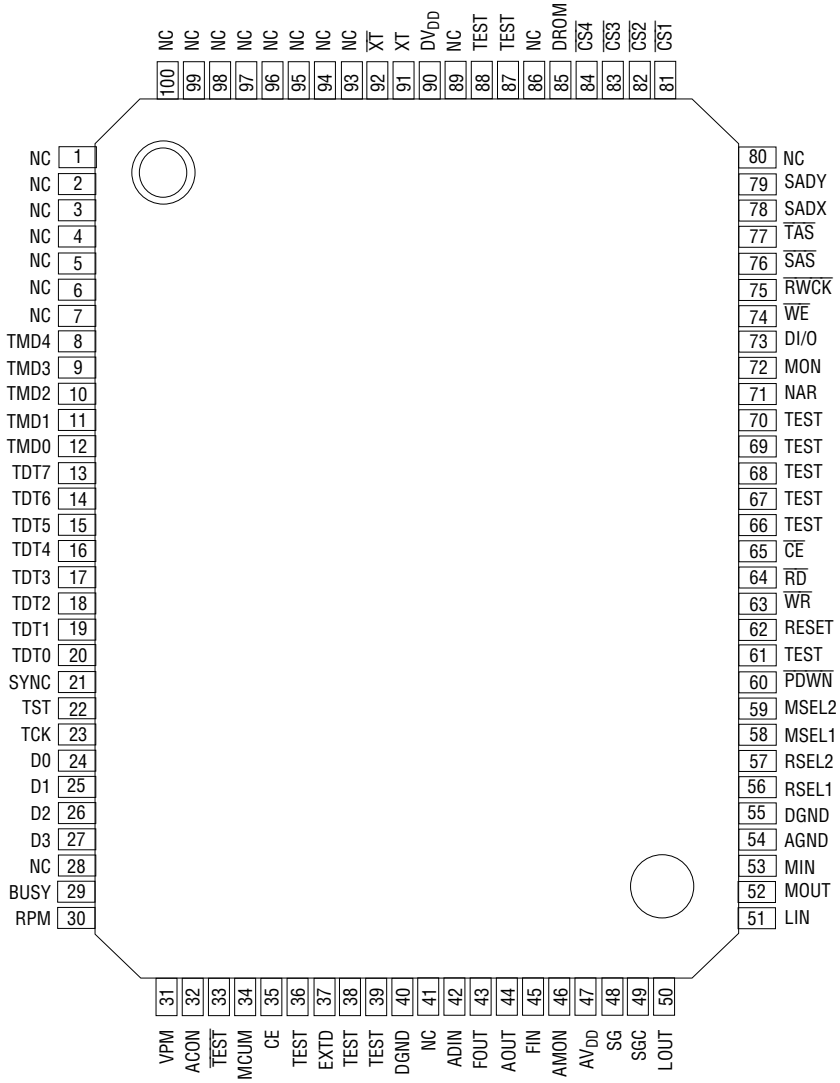
DV_{DD}=AV_{DD}=4.5 to 5.5 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	No load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	V_{DD}–1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
OP-amp open loop gain	G_{OP}	f_{IN}=0 to 4 kHz	40	—	—-	dB
OP-amp input impedance	R_{INA}	—	1	—	—	MΩ
OP-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3V Version))



100-Pin Plastic QFP

NC : No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Type	Description
90	DV_{DD}	—	**Digital power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the DGND pin.
47	AV_{DD}	—	**Analog power supply.** Insert a bypass capacitor of 0.1μF or more between this pin and the AGND pin.
40, 55	DGND	—	**Digital ground.**
54	AGND	—	**Analog ground.**
48, 49	SG, SGC	O	**Output for analog circuit reference voltage (signal ground).**
53 51	MIN LIN	I	**Inverting input of the built-in OP amplifier.** The non-inverting input pin is internally connected to SG (signal ground).
52 50	MOUT LOUT	O	**Output of the built-in OP amplifier for MIN and LIN.**
46	AMON	O	**Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode.** This pin connects the built-in LPF input (FIN pin).
45	FIN	I	**Input of the built-in LPF.**
43	FOUT	O	**Output of the built-in LPF.** This pin connects the AD converter input (ADIN pin).
42	ADIN	I	**Input of the built-in 12-bit AD converter.**
44	AOUT	O	**Output of the built-in LPF.** This pin outputs playback waveforms and connects an external speaker drive amplifier.
79 78	SADY SADX	O	These pins connect to SAD pin of serial register and serial voice ROM. These pins output leading addresses of read/write.
77	$\overline{TAS}$	O	This pin connects to $\overline{TAS}$ pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	$\overline{SAS}$	O	This pin connects to the $\overline{SAS}$ pin of the serial register and the $\overline{SASX}$ and $\overline{SASY}$ pins of the serial voice ROM. Clock pin to write serial addresses.
75	$\overline{RWCK}$	O	This pin connects to the $\overline{RWCK}$ pin of the serial register and the $\overline{RDCK}$ pin of the serial voice ROM. Clock pin to read data from and write data into the serial register.
74	$\overline{WE}$	O	**Write Enable.** This pin connects to the $\overline{WE}$ pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	I/O	**Data I/O.** This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin is used to output write data and inputs read data.
85	DROM	I	**Data ROM.** This pin connects to the DOUT pin of the serial voice ROM.
81 82 83 84	$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	**Chip Slect.** These pins connect $\overline{CS}$ pin of the serial register and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of the serial voice ROM.
58 59	MSEL1 MSEL2	I I	These pins select the capacity of the memory to be connected externally.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>56
57</td><td>RSEL1
RSEL2</td><td>I
I</td><td>These pins select the number of serial registers to be connected externallly.
<table>
<tr><th>MSEL2</th><th>MSEL1</th><th>RSEL2</th><th>RSEL1</th><th>Memory capacity</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>4M ×1</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>4M ×2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>4M ×3</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>4M ×4</td></tr>
</table></td></tr>
<tr><td>34</td><td>MCUM</td><td>I</td><td>Mode Selection.
Low level : Stand-alone mode
High level : Microcontroller interface mode</td></tr>
<tr><td>62</td><td>RESET</td><td>I</td><td>A high input level causes the MSM6789L to be initialized and to go into the power down state.</td></tr>
<tr><td>60</td><td>$\overline{\text{PDWN}}$</td><td>I</td><td>Power Down. When a low level is input the MSM6789L goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789L to be reset.
When an Low level is applied to this pin during recording operation, the MSM6789L is halted, and will be maintained in the power down state while $\overline{\text{PDWN}}$ is low level.
After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>24
25
26
27</td><td>D0
D1
D2
D3</td><td>I/O</td><td>Bidirectional data bus to transfer commands and data to and from an external microcontroller.</td></tr>
<tr><td>63</td><td>$\overline{\text{WR}}$</td><td>I</td><td>Write Pulse Input. Inputting a low pulse to $\overline{\text{WR}}$ pin causes a command or data to be input via D0 to D3 pins.</td></tr>
<tr><td>64</td><td>$\overline{\text{RD}}$</td><td>I</td><td>Read Pulse Input. Inputting a low pulse to $\overline{\text{RD}}$ pin causes status bits or data to be output via D0 to D3 pins.</td></tr>
<tr><td>65
35</td><td>$\overline{\text{CE}}$
CE</td><td>I</td><td>Chip Enable Input. When the $\overline{\text{CE}}$ pin is set to low level and the CE pin is set to a high level, the write pulse ($\overline{\text{WR}}$) or read pulse ($\overline{\text{RD}}$) can be accepted.
When the $\overline{\text{CE}}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{\text{WR}}$) and read pulse ($\overline{\text{RD}}$) cannot be accepted so that data cannot be communicated via D0 to D3 pins.</td></tr>
<tr><td>29</td><td>BUSY</td><td>O</td><td>Busy. This pin outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0 to D3 pins. The state of this pin is the same as the contents of the BUSY bit of the status register.</td></tr>
<tr><td>30</td><td>RPM</td><td>O</td><td>RPM. This pin outputs a high level during recording or playback operation. The state of this pin is the same as the contents of the RPM bit of the status register.</td></tr>
</table>

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

Pin	Symbol	Type	Description
31	VPM	O	**VPM.** This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	O	**NAR.** This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	**P_{OP} Noise Suppression Select.** This pin selects whether the pop noise suppression circuit is used. Low level : the pop noise suppression circuit is not used. High level : the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	**EXTD.** In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	**Oscillator Connect.** When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	$\overline{XT}$	O	**Oscillator Connect.** When an external clock is uesd, this pin must be left open.
72	MON	O	**MON.** This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70 33	TEST $\overline{TEST}$	I	**MSM6789L Test.** Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.
9-12 13-20 21	TMD3-TMD0 TDT7-TDT0 SYNC	I/O	**MSM6789L Test.** This pin must be left open.
17-20	TDT3-TDT0	I/O	These pins must be left open as they are MSM6789L test pins.
22 23 8	TST TCK TMD4	I	**MSM6789L Test.** Input a low level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	–0.3 ~ V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T_{op}	—	0 to +70	°C
Master clock frequencuy	f_{OSC}	—	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.85×V_{DD}	—	—	V
Low input voltage	V_{IL}	—	—	—	0.15×V_{DD}	V
High output voltage	V_{OH}	I_{OH}=–40 µA	V_{DD}–0.3	—	—	V
Low output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.45	V
High input current*1	I_{IH1}	V_{IH}=V_{DD}	—	—	10	µA
High input current*2	I_{IH2}	V_{IH}=V_{DD}	—	—	20	µA
Low input current*1	I_{IL1}	V_{IL}=GND	–10	—	—	µA
Low input current*2	I_{IL2}	V_{IL}=GND	–20	—	—	µA
Operating current consumption	I_{DD}	f_{OSC}=8 MHz, no load	—	20	35	mA
Power down current	I_{DDS1}	No load Serial register connected	—	—	10	µA
	I_{DDS2}	No load DRAM connected	—	200	—	µA

*1 Applies to all inputs excluding the XT pin.
*2 Applies to the XT pin.

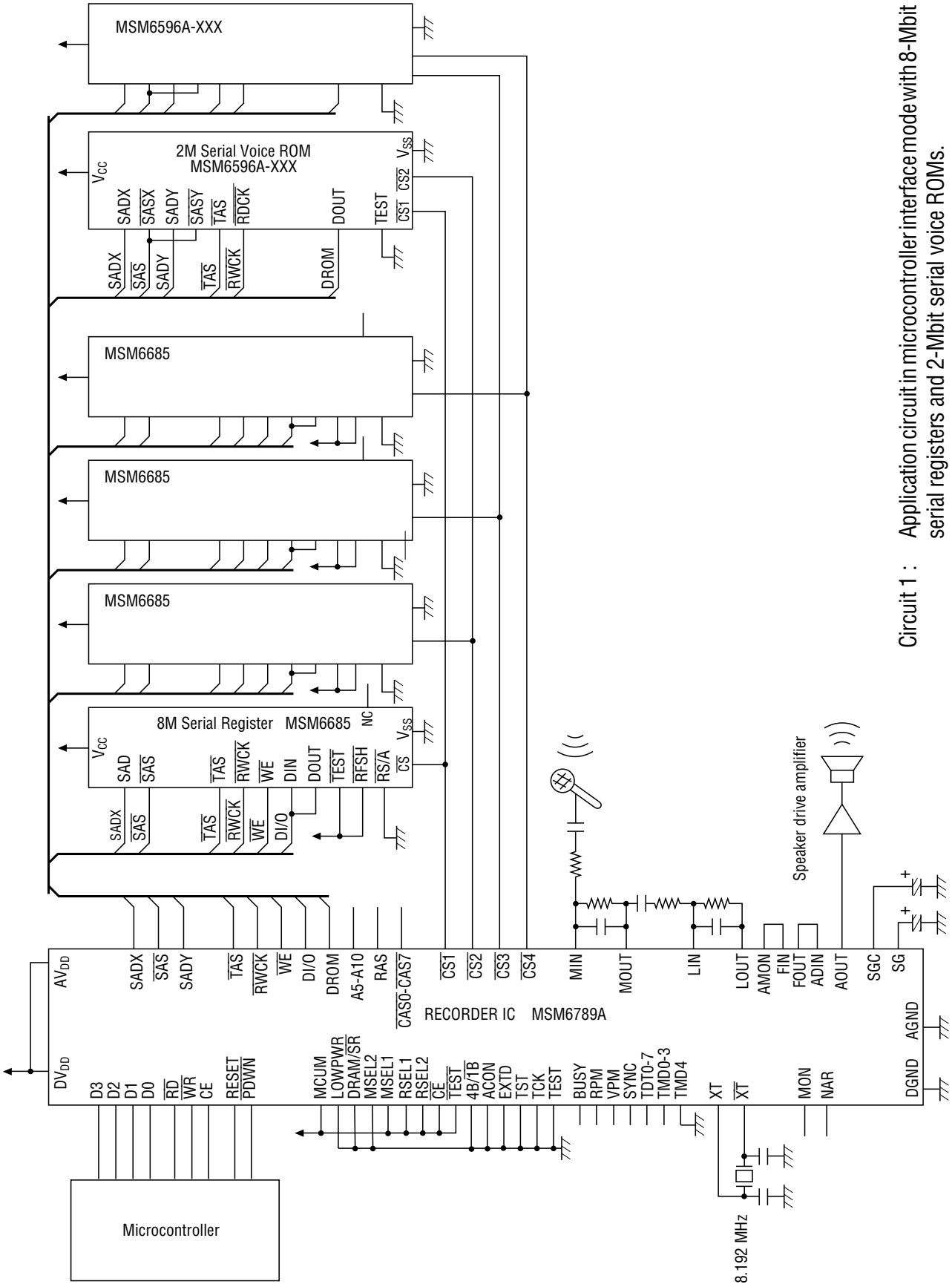
Analog Characteristics

DV_{DD}=AV_{DD}=3.0 to 3.6 V
DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DA output relative error	$\lvert V_{DAE} \rvert$	No load	—	—	20	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	V_{DD}–1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
OP-amp open loop gain	G_{OP}	f_{IN}=0 to 4 kHz	40	—	—-	dB
OP-amp input impedance	R_{INA}	—	1	—	—	MΩ
OP-amp load resistance	R_{OUTA}	—	400	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	100	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	100	—	—	kΩ

APPLICATION CIRCUITS (for MSM6789A (5 V Version))

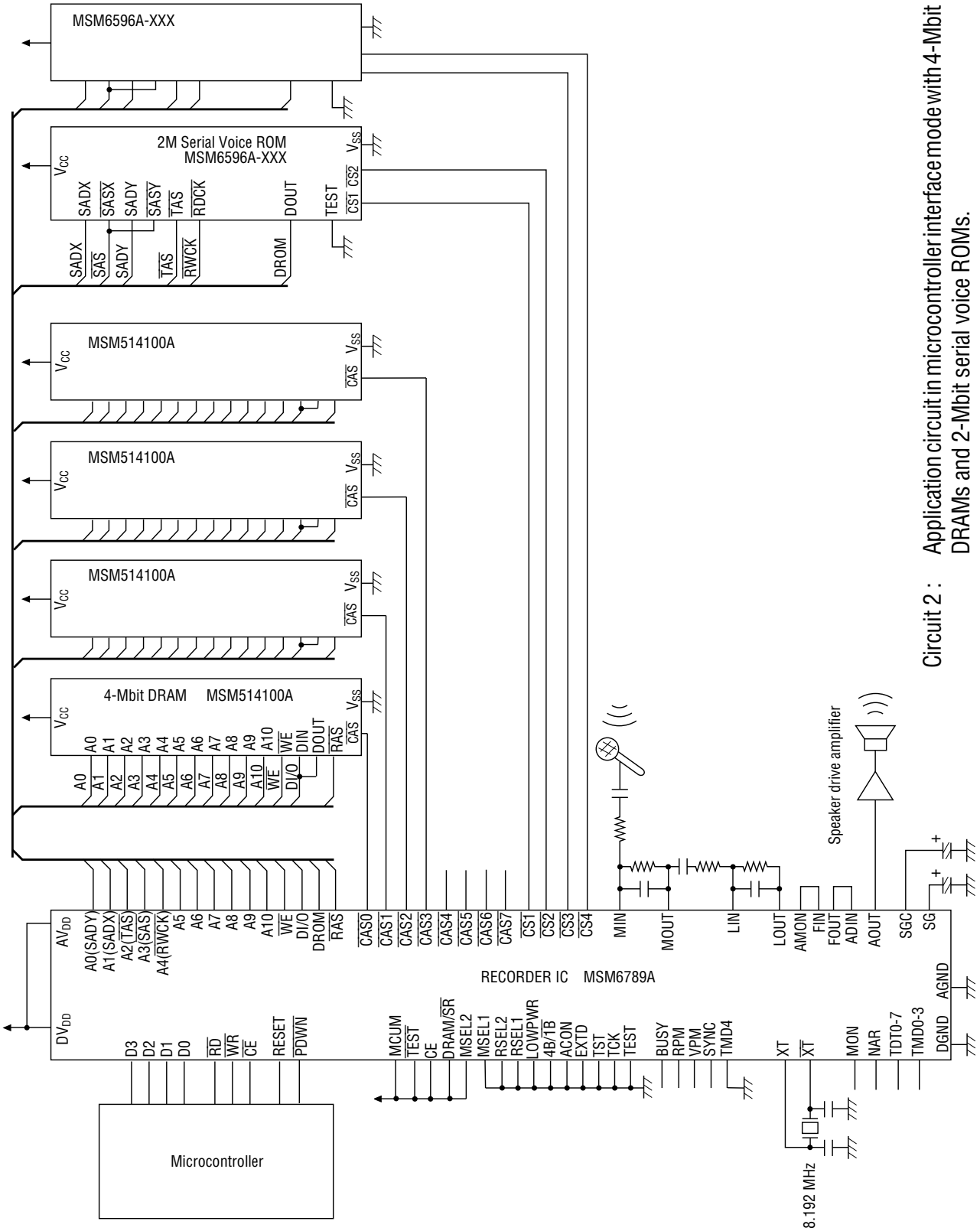
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.



Circuit 1 : Application circuit in microcontroller interface mode with 8-Mbit serial registers and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

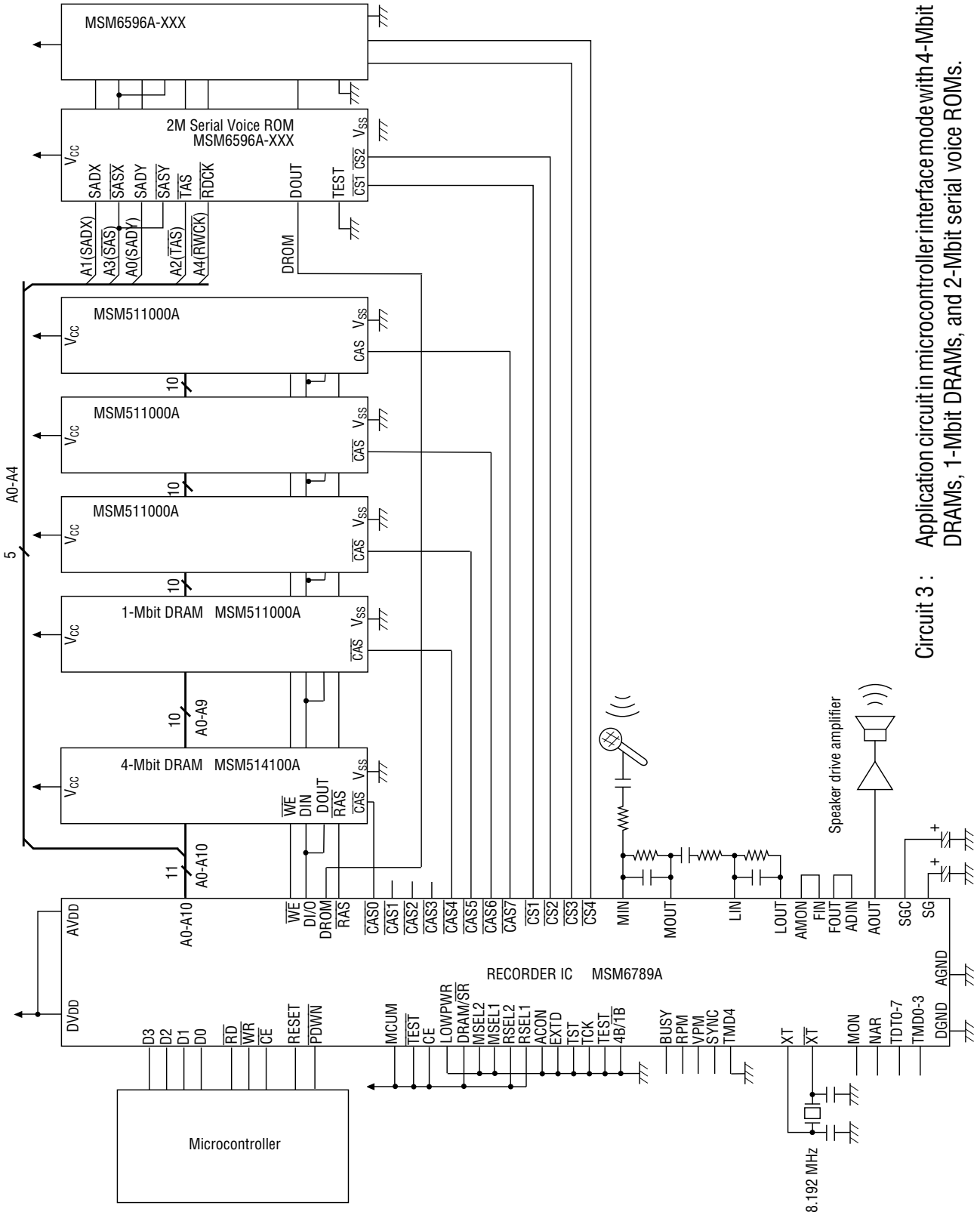
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 2 : Application circuit in microcontroller interface mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

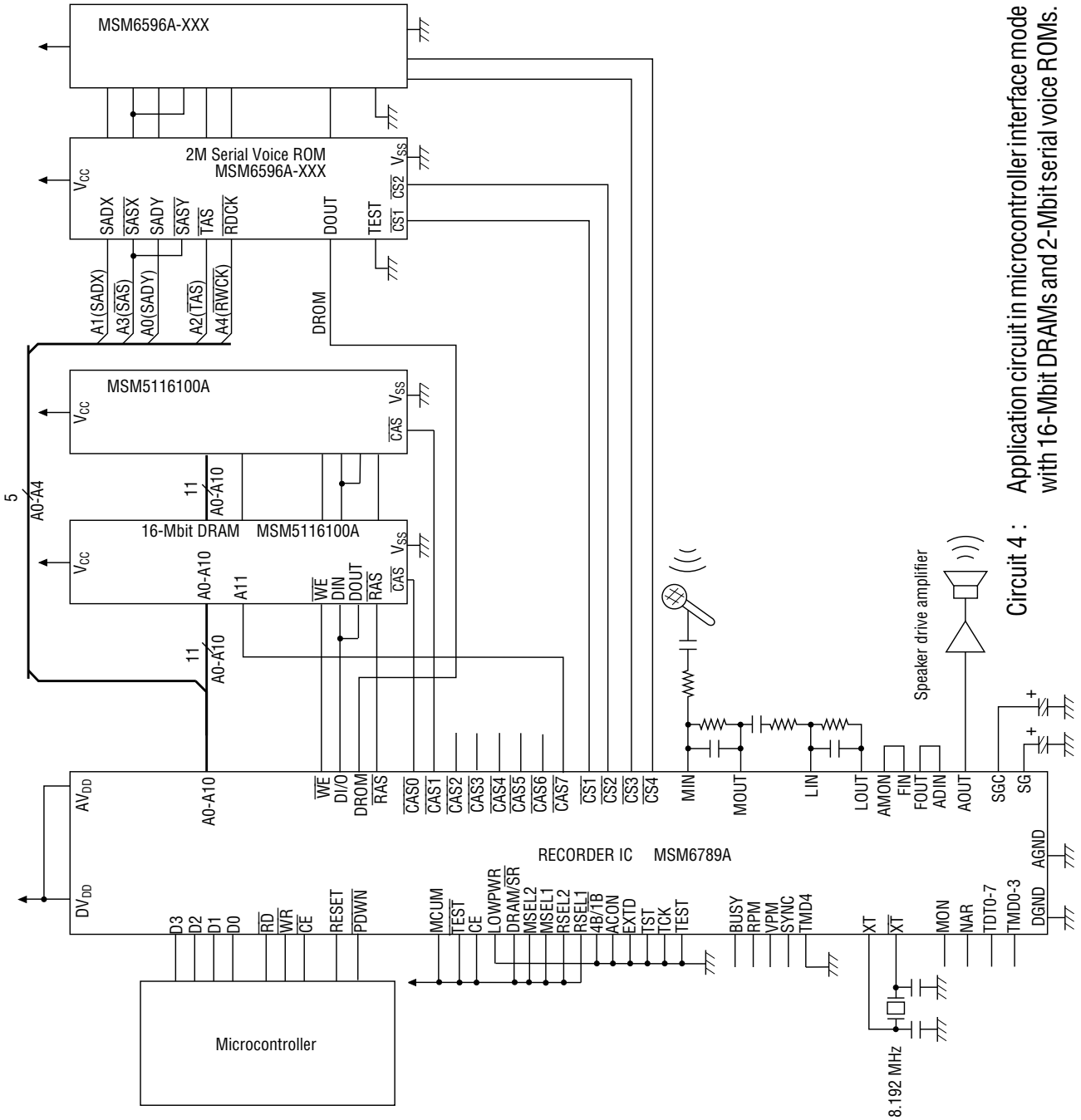
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit × type), and two 2-Mbit serial voice ROMs.



Circuit 3 : Application circuit in microcontroller interface mode with 4-Mbit DRAMs, 1-Mbit DRAMs, and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

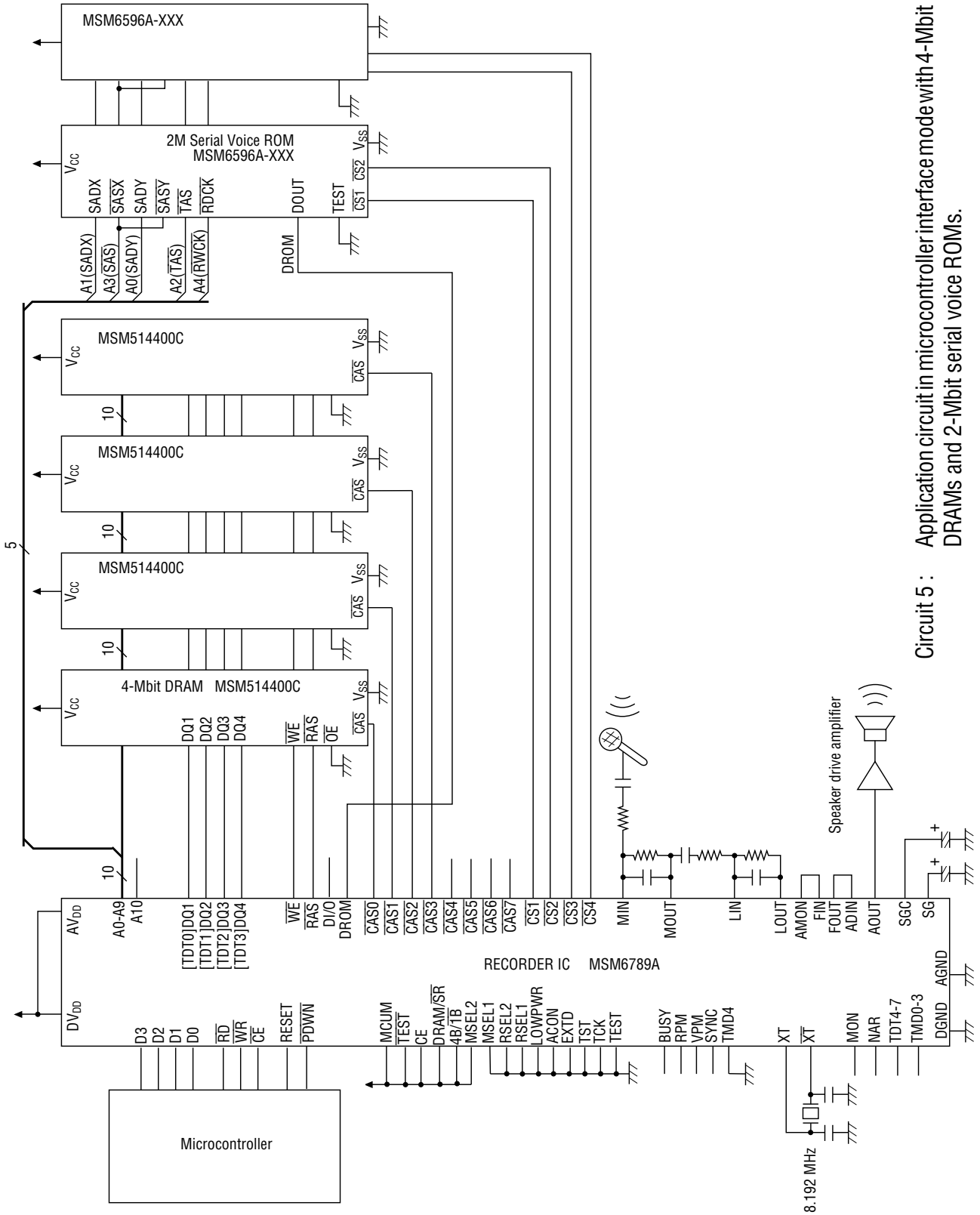
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 4 : Application circuit in microcontroller interface mode with 16-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

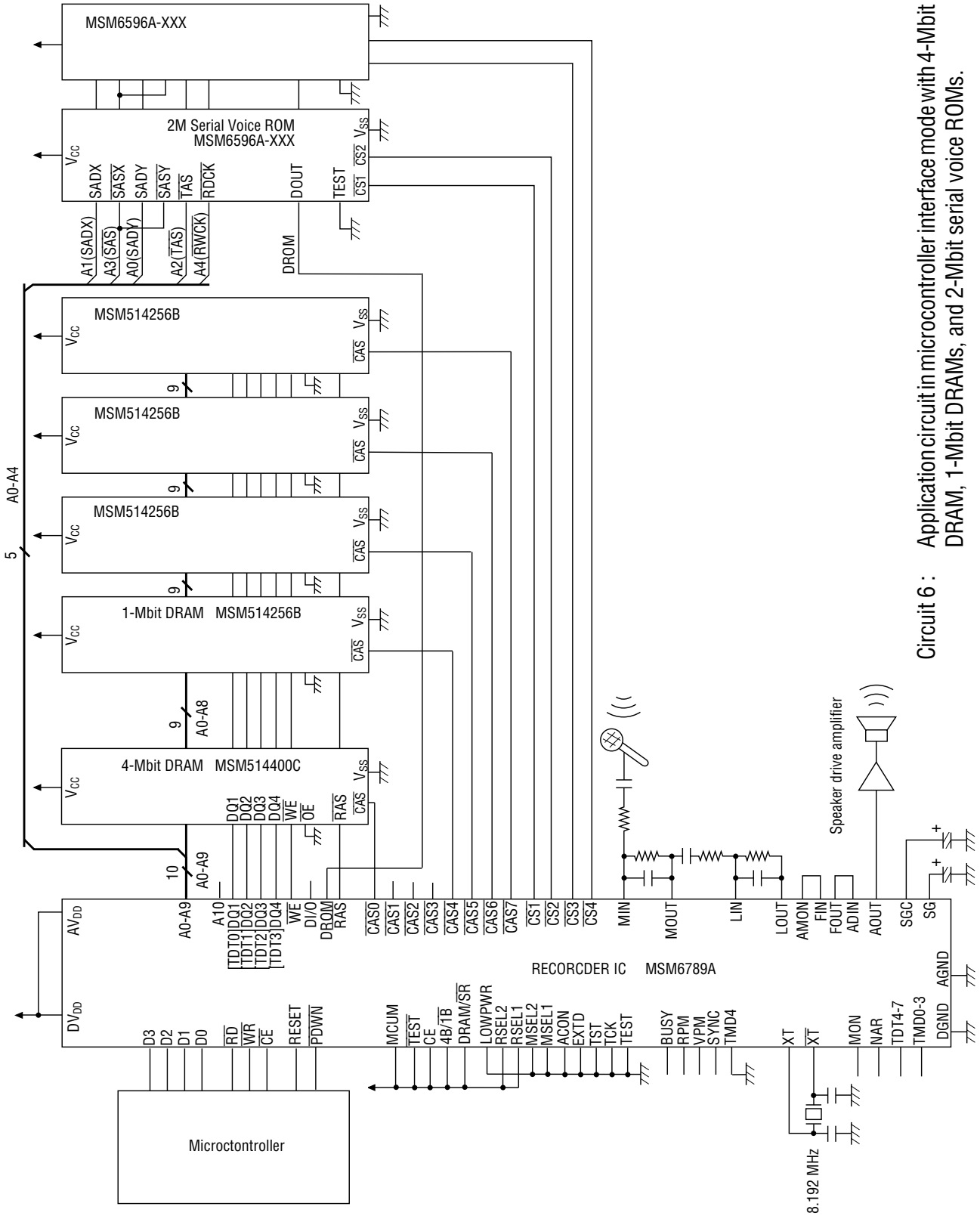
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 5 : Application circuit in microcontroller interface mode with 4-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

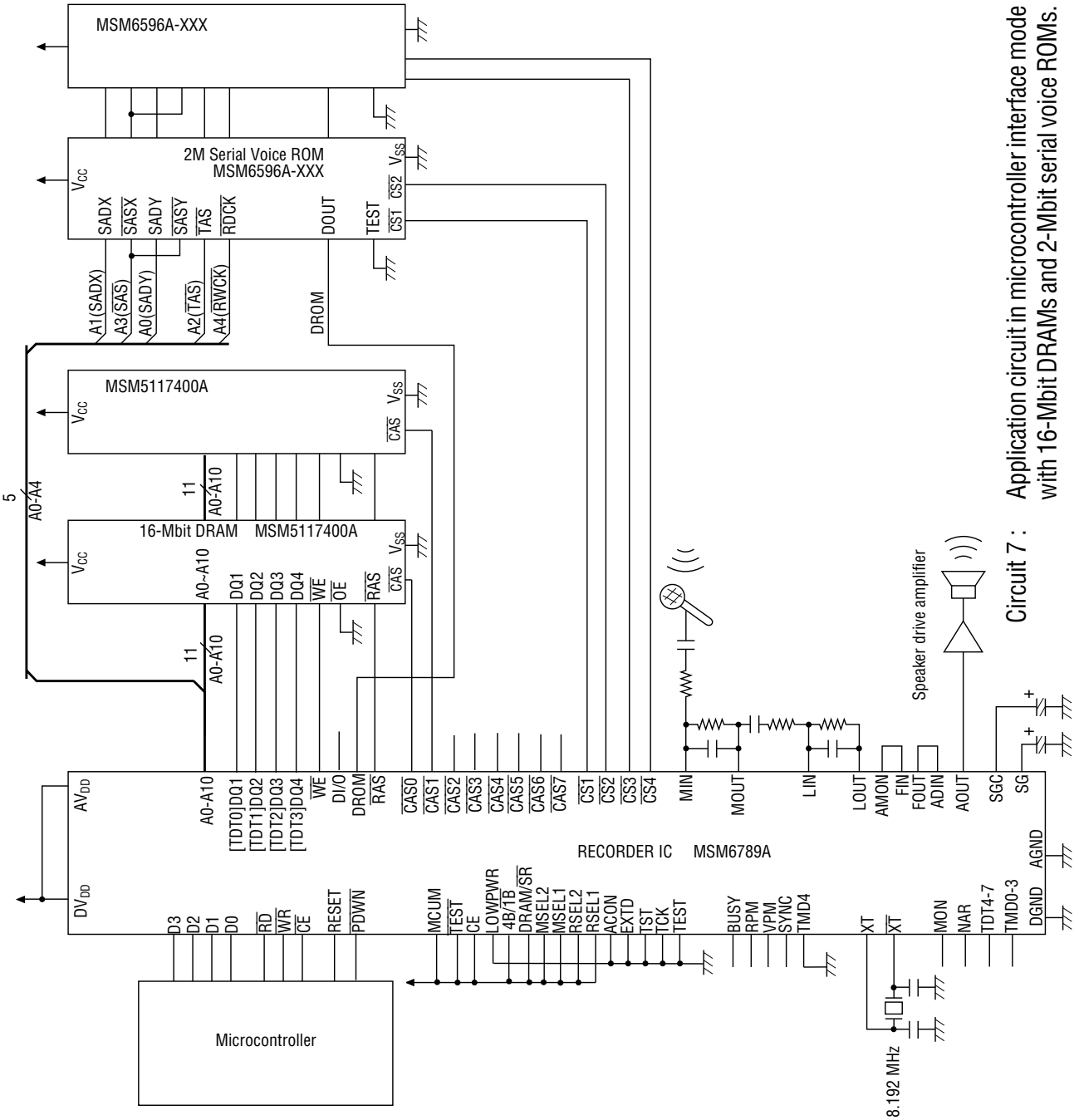
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.



Circuit 6 : Application circuit in microcontroller interface mode with 4-Mbit DRAM, 1-Mbit DRAMs, and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

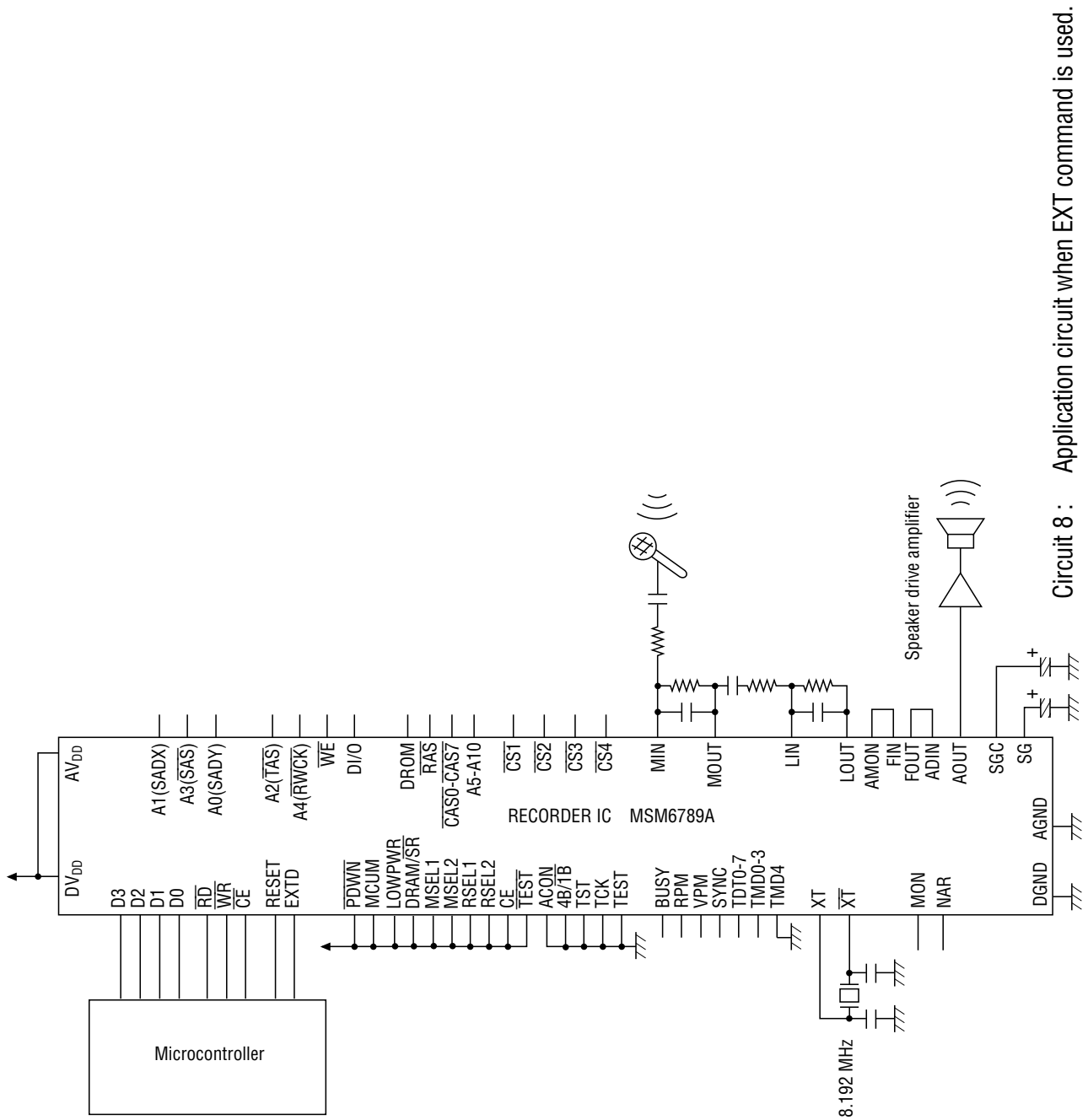
This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



Circuit 7 : Application circuit in microcontroller interface mode with 16-Mbit DRAMs and 2-Mbit serial voice ROMs.

APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

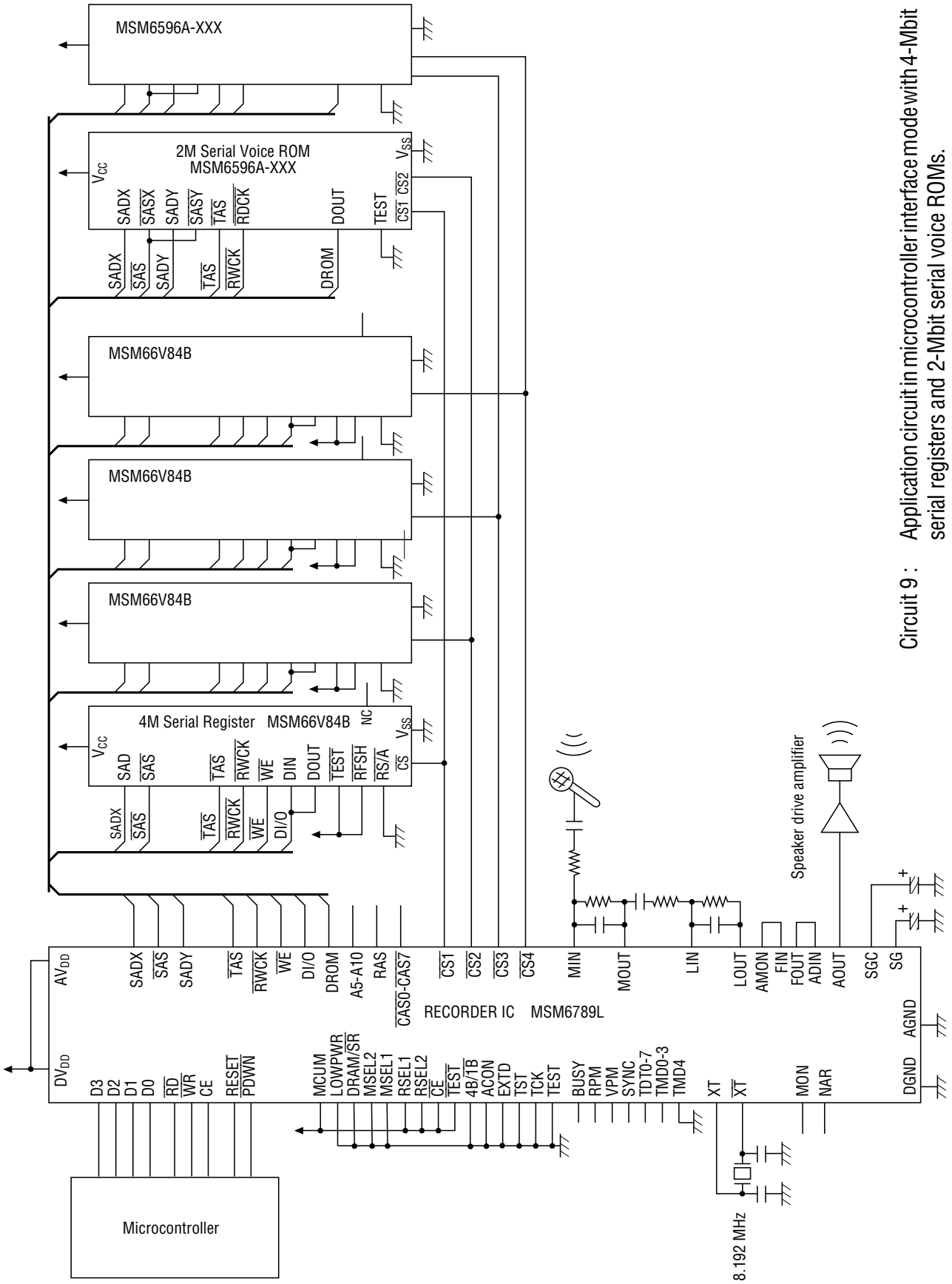
This is an application circuit example when the EXT command is used for recording/playback.



Circuit 8 : Application circuit when EXT command is used.

APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in microcontroller interface mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.



Circuit 9 : Application circuit in microcontroller interface mode with 4-Mbit serial registers and 2-Mbit serial voice ROMs.