OKI Semiconductor

MSM6789A/6789L

SBC Solid-State Recorder IC

GENERAL DESCRIPTION

The MSM6789A/6789L, an improved version of MSM6788, is a solid-state recorder developed using the Sub Band Coding (SBC) method.

Just like MSM6788, the MSM6789A/6789L has a stand-alone mode and a microcontroller interface mode. In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6789A/6789L can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller, and more functions are available than in the stand-alone mode.

The MSM6789A/6789L can directly drive serial voice ROM as external memory as well as serial register or general-purpose DRAM* (1-bit × or 4-bit × type selectable) as external memories, which allows a recording and playback circuit with fixed messages to be built easily. The method from microcontroller is the same as the MSM6788.

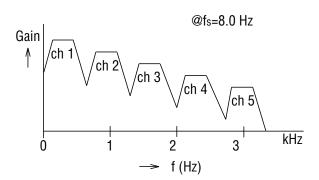
* Only for MSM6789A

• Difference between MSM6788 and MSM6789A

	MSM6788	MSM6789A
General DRAM	Unavailable	Available
Unvoiced-part elimination function	No	Yes
PCM playback	No	Yes

• SBC method:

The SBC method divides voice frequencies into five bands and codes the component for each of the bands separately, as shown below.



Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

• Difference between MSM6789A and MSM6789L

Parameter	MSM6789A	MSM6789L
Operating voltage	4.5 to 5.5 V	3.0 to 3.6 V
External memory	General-purpose DRAM, 32 Mbits (max.)	16 Mbits (max.)
	1-Mbit DRAM (MSM514256B, MSM511000B)	4 Mbits (MSM66V84B)
	4-Mbit DRAM (MSM514400C, MSM514100C)	
	16-Mbit DRAM (MSM511740CA, MSM5116100A)	
	ARAM*, 32 Mbits (max.)	
	Serial register, 32 Mbits (max.)	
	4 Mbits (MSM6684B)	
	8 Mbits (MSM6685)	

^{*} Use ARAM which has no failed bits in its first 64 Kbits.

STAND-ALONE MODE

FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter

Attenuation characteristics -40 dB/oct

External memories

MSM6789A (5 V version)

General-purpose DRAM, 32 Mbits maximum (for variable messages)

1-Mbit DRAM: Can be directly driven (MSM514256B, MSM511000B)

4-Mbit DRAM: Can be directly driven (MSM514400C, MSM514100C)

16-Mbit DRAM: Can be directly driven (MSM5117400A, MSM5116100A)

ARAM, 32 Mbits maximum (for variable messages)

Note: Use the first 64 Kbits with no failed bits for the ARAM.

Serial register, 32 Mbits maximum (for variable messages)

4-Mbit serial register: Can be directly driven (MSM6684B)

8-Mbit serial register: Can be directly driven (MSM6685)

MSM6789L (3.3 V version)

Serial register, 16 Mbits maximum (for variable messages)

4-Mbit serial resister: Can be directly driven (MSM66V84B)

MSM6789A (5 V version) and MSM6789L (3.3 V version)

Serial voice ROM, 4 Mbits maximum (for fixed messages)

1-Mbit serial voice ROM: Can be directly driven (MSM6595A)

2-Mbit serial voice ROM: Can be directly driven (MSM6596A)

3-Mbit serial voice ROM: Can be directly driven (MSM6597A)

• Bit rate

10.0, 12.6, 16.0 kbps (at 8 kHz sampling freq.)

7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)

Maximum recording time (when one 8-Mbit serial register is connected)

13.8 minutes (for 10.0 kbps SBC) 18.4 minutes (for 7.5 kbps SBC)

11.0 minutes (for 12.6 kbps SBC) 14.6 minutes (for 9.5 kbps SBC)

8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)

Number of phrases

63 phrases for variable messages

63 phrases for fixed messages

- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Unvoiced-part elimination function (voice detect level can be set)
- Pausing function

Master clock frequency:
 6.0 MHz to 8.192 MHz

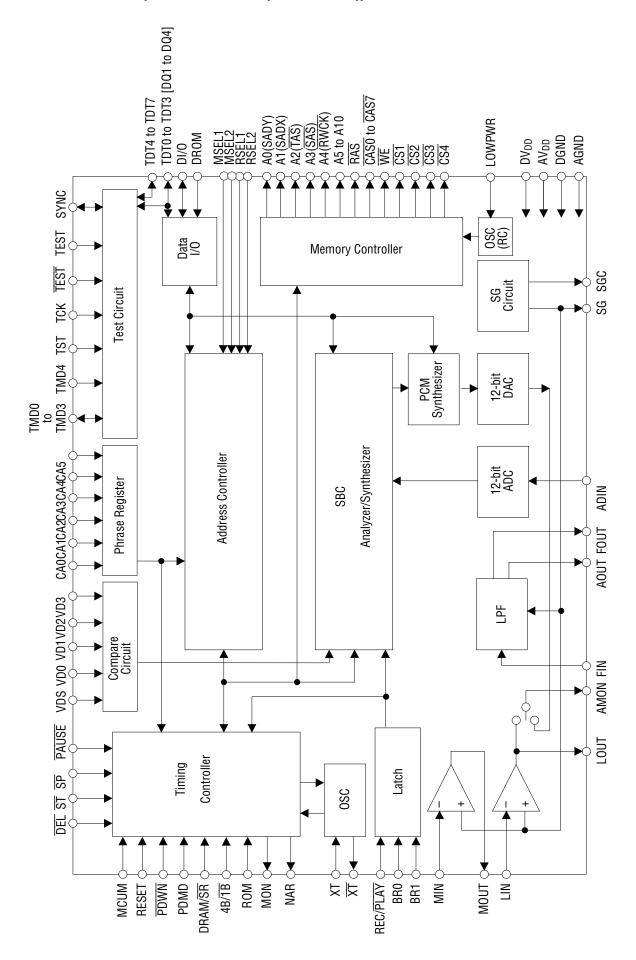
• Power supply voltage:

MSM6789A: Single 5 V power supply MSM6789L: Single 3.3 V power supply

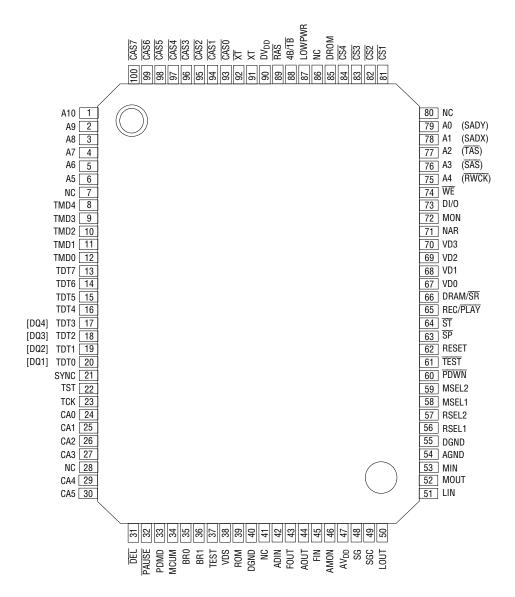
• Package options:

MSM6789A: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK) MSM6789L: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

(): Pins for connecting serial voice ROM[]: Pins for connecting 4-bit × type DRAM

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Symbol	Туре	Description						
DV		Digital power supply. Insert a bypass capacitor of 0.1 µF or more between this						
DADD		pin and the DGND pin.						
۸۷٫۶۶		Analog power supply. Insert a bypass capacitor of 0.1 μ F or more between this						
AVDD		pin and the AGND pin.						
DGND	_	Digital ground.						
AGND	_	Analog ground.						
SG, SGC	_	Output for analog circuit reference voltage (signal ground).						
MIN	1	Inverting input of the built-in OP amplifier. The non-inverting input pin is						
LIN	•	internally connected to SG (signal ground).						
MOUT	0	Output of the built-in OP amplifier for MIN and LIN.						
LOUT		output of the bunt-in of ampliner for white and Life.						
ΔΜΩΝ	Ο	Connected to the LOUT pin in the recording mode and to the DA converter						
AIVION	0	output in the playback mode. This pin connects the built-in LPF input (FIN pin).						
FIN	I	Input of the built-in LPF.						
FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).						
ADIN	-	Input of the built-in 12-bit AD converter.						
AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects						
AUUT	0	an external speaker drive amplifier.						
DRAM/SR	66 DRAM/SR	66 DRAM/SR I	66 DRAM/SR	6 DRAM/SR				This pin selects whether memory to be connected externally is DRAM or serial register.
					RAM/SR I	Low level : Serial register		
				High level : DRAM				
		This pin selects either 1-bit $ imes$ type DRAM or 4-bit $ imes$ type DRAM.						
4B/ 1B	1	Low level : 1-bit × type						
		High level : 4-bit × type						
40 (SADV)		These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also						
, ,	0	connect to SAD pin of serial register and serial voice ROM at the time of serial						
AT (SADA)		register selection. These pins output leading addresses of read/write.						
		This pin connects to A2 of DRAM at the time of DRAM selection. It also connects						
42 (<u>TAC</u>)	0	to TAS pin of serial register and serial voice ROM at the time of serial register selection.						
AZ (1A3)	U	This pin is used to set serial addresses from the SADX and SADY pins into the						
		internal address counter of the serial register and serial voice ROM.						
		This pin connects to A3 of DRAM at the time of DRAM selection. It also connects						
A3 (SAS)	0	to the SAS pin of the serial register and the SASX and SASY pins of the serial voice						
		ROM at the time of serial register selection. Clock pin to write serial addresses.						
		This pin connects to A4 of DRAM at the time of DRAM selection. It also connects						
A4 (RWCK)	0	to the RWCK pin of the serial register and the RDCK pin of the serial voice ROM at						
	U	the time of serial register selection. Clock pin to read data from and write data into						
		the serial register.						
۸10-۸5	0	This pin connects to pins A5-A10 of DRAM at the time of DRAM selection.						
A IU-AO	U	This pin outputs addresses of read/write.						
	DVDD AVDD DGND AGND SG, SGC MIN LIN MOUT LOUT AMON FIN FOUT ADIN AOUT DRAM/SR 4B/1B A0 (SADY) A1 (SADX) A2 (TAS)	DV _{DD} — AV _{DD} — DGND — AGND — SG, SGC — MIN I LIN O AMON O FIN I FOUT O ADIN I AOUT O DRAM/SR I 48/1B I A0 (SADY) A1 (SADX) O A3 (SAS) O A4 (RWCK) O						

Symbol	Туре	Description					
WE	0	Write Enable.	This pin conn	ects to the WE	pin of the seri	al register and DRAM.	
VVE	U	This pin selects	This pin selects either read or write mode.				
DIVO	1/0	Data I/O. This	pin connects t	o the DIN and	DOUT pins of	the serial register and	
טווע	1/0	DRAM. This pin	outputs write	data and inputs	s read data.		
DROM	1	Data ROM. Th	is pin connect	s to the DOUT	pin of the seri	al voice ROM.	
RAS	0	This is a row add	dress strobe pi	n of DRAM at	the time of DR	AM selection.	
CACO		These are the co	lumn address	strobe pins of	DRAM at the t	ime of DRAM selection.	
	0	CAS7, an addres	ss output pin,	is connected t	o pin A11 of D	RAM at the time 16-Mbit	
UAS/		DRAM selection.					
CS1							
CS2		Chip Select. T	hese pins conr	nect to \overline{CS} pin (of the serial req	gister and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$,	
CS3	U	$\overline{\text{CS2}}, \overline{\text{CS3}})$ pins of	of the serial vo	ice ROM.			
CS4							
MSEL1	1	Those pine color	t the consoity	of the memory	to he connect	and autornally	
MSEL2	I	These pins selec	t the capacity	or the memory	to be connect	eu externally.	
		•			ŭ	be connected externallly.	
		MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity	
		L	L	L	L	1M × 4	
		L	L	L	Н	4M × 1	
		L	L	Н	L	1M × 8	
		L	L	Н	Н	$1M \times 4 + 4M \times 1$	
		L	Н	L	L	4M × 2	
		L	Н	L	Н	$4M \times 2$	
	l	L	Н	Н	L	$4M \times 3$	
RSEL2	l	L	Н	Н	Н	$4M \times 3$	
		Н	L	L	L	$4M \times 4$	
		НН	L	L	Н	16M × 1	
		Н	L	Н	L	$4M \times 6$	
		Н	L	Н	Н	$4M \times 6$	
		Н	Н	L	L	4M × 8	
		Н	Н	L	Н	4M × 8	
		Н	Н	Н	L	16M×2	
		Н	Н	Н	Н	16M×2	
	WE DI/O DROM RAS CASO- CAS7 CS1 CS2 CS3 CS4 MSEL1	WE 0 DI/O I/O DROM I RAS 0 CASO-CAST 0 CS1 CS2 CS3 CS4 MSEL1 I MSEL2 I	WE	WE 0 Write Enable. This pin connector this pin selects either read or with pin selects or DRAM. This pin connects the pin selection. CASO-CASO-CASO-CASO-CASO-CASO-CASO-CASO-	WE 0 Write Enable. This pin connects to the WE This pin selects either read or write mode. DI/O I/O Data I/O. This pin connects to the DIN and DRAM. This pin outputs write data and inputs DROM I Data ROM. This pin connects to the DOUT This is a row address strobe pin of DRAM at These are the column address strobe pins of CAS7, an addresss output pin, is connected to DRAM selection. CST CST Chip Select. These pins connect to CS pin of CS2, CS3) pins of the serial voice ROM. CS4 These pins select the capacity of the memory MSEL1 I MSEL2 These pins select the number of DRAMs and selected (DRAM/SR = High MSEL2 MSEL1 RSEL2 LLL LLL LLL LLL LLL LLL LLL LLL LLL	Write Enable. This pin connects to the WE pin of the sering this pin selects either read or write mode.	

Pin	Symbol	Туре	Description						
			• When serial	register is sele	cted (DRAM/S	\overline{R} = Low level)			
			MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity		
			L	L	L	L	4M × 1		
			L	L	L	Н	4M × 2		
56	RSEL1	ı	L	L	Н	L	4M × 3		
57	RSEL2	'	L	L	Н	Н	4M × 4		
37	HOLLZ	'	L	Н	L	L	8M×1		
			L	Н	L	Н	8M × 2		
			L	Н	Н	L	8M × 3		
			L	Н	Н	Н	8M × 4		
87	LOWPWR	I	power down w Low level : 15 High level : 12	This pin selects CAS-before-RAS refresh period of DRAM at the time of power down when DRAM is selected. Low level: 15 µs max. High level: 125 µs max.					
			Mode Selec						
34	MCUM			ind-alone mode					
				crocontroller ir					
62	RESET	ı		vel causes the	MSM6789A to	be initialized	and to go into the power		
			down state.	\\/\ ____\\		1401407004			
					-		goes to the power down		
60	PDWN	I	state. Unlike the RESET pin, this pin does not force the MSM6789A to be reset. When a Low level is applied to this pin during recording operation, the MSM6789A is halted, and will be maintained in the power down state while PDWN is low level.						
					•		recording will be performed		
91	XT	l	Oscillator C	onnection. V	Vhen an extern	al clock is use	d, input the clock through		
			•	•		•	d, this pin must be left		
92	XT	0	open.				, , ,		
37	TEST	ı	NACNACZOO A	Took Innut a l	our loved to the	TECT nin and a	high lovel to the TECT -:-		
61	TEST		MSM6789A	lest. Input a id	ow level to the	1EST pin and a	a high level to the TEST pin.		
9-12	TMD3-TMD0								
13-20	TDT7-TDT0	I/O	MSM6789A	Test. This pin	must be left o	pen.			
21	SYNC								
17-20	TDT3-TDT0	1/0	Connect these	pins to DQ1-D	Q4 of DRAM a	t the time of 4	-bit × type DRAM		
	[DQ4]-[DQ1]	"0	selection. Oth	erwise these p	ins must be lef	t open as they	are MSM6789A test pins.		
22	TST								
23	TCK	I	MSM6789A	Test. Input a l	ow level signa	l.			
8	TMD4								

Pin	Symbol	Туре						Desc	ription	
39	ROM	I	operation	Playback Operation. When set to low, this pin selects the record/playback operation (only for the SBC method). When set to high, it selects the ROM playback operation (for the SBC and PCM methods).						
65	REC/PLAY	I	the ROI	Recording mode or playback mode selection. This pin is invalid during the ROM playback operation. When set to low, it selects the playback mode. When set to high, it selects the recording mode.						
64	ST	I	Start F	_				evel pı	ulse is applied to	o this pin, the record/playbacl
63	SP	I	Stop F or ROM	_				vel pu	lse is applied to	this pin, the record/playback
32	PAUSE	I	Playba or ROM					-		o this pin, the record/playback
31	DEL	I	or spec through ch00: ch01 After po	Phrase Delection. When a low level pulse is applied to this pin, all phrase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5, ch00:All phrase deletion ch01 to ch3F:Specified phrase deletion After power up, be sure to input a RESET signal and then delete all phrases. After completing this procedure, start the record/playback operation.						
24-30	CAO-CA5	I	Desire	ed Pho of 63 p	rase :	Speci s can b	ficati be spe	on. cified in		the record/playback operation Remarks All phrase deletion A total of 63 phrases can be used for both record /playback and ROM playback operation.

Pin	Symbol	Туре			Descri	ption	
				-		of the following three ty n is invalid during the RC	•
				BR1	BR0	Bit rate]
35	BRO	١,		L	L	16.0 kbps	-
36	BR1	'		L	Н	12.6 kbps	-
				Н	L	10.0 kbps	
				Н	Н	Unused	
			Transition to	the Power	-down Sta	te.	
						cally goes to the power	•
		PDMD*1 I				k operation is perform	
00	DDMD*1					ically goes to the standl	-
33	PUMD					ot when the record/play se, the MSM6789A can	•
				•		ting the RESET or PDV	•
					-	ed for the built-in LPF, i	
						lying a high level to th	-
67-70	VD0-VD3	1	These pins set th	e voice dete	ct level for th	e voice triggered starti	ng and unvoiced-part
07-70	VD0-VD3	'	elimination.				
				•	•	g or the unvoiced-part e	
			Voice trigger	ed starting:		ih level to the VDS pin.	
00	\/D0					el with VD0 to VD3 pins	
38	VDS	l	Unvoiced-par	t elimination	•	r level to the VDS pin. The level to the VDS pin. The level to VD3 pins	
			Note: When neith	er the voice		arting nor the unvoiced	
			used, input a Lov			arting nor the unvoiced	part chimination is
72	MON	0	<u> </u>			cord/playback operatio	on is being performed
						state of the operation fo	
71	NAR	0	phrase. When c	ontinuous R	OM playbac	k is performed, the nex	ct phrase can
			be specified after	r the NAR pi	n goes to hi	gh positively.	

^{*1} When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input voltage	V _{IN}	Ta=25°C	-0.3 to V _{DD} +0.3	V
Storage temperature	T _{STG}	_	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*4	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	f _{OSC}	_	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

 $\mbox{DV}_{\mbox{DD}}\mbox{=}\mbox{AV}_{\mbox{DD}}\mbox{=}\mbox{4.5}$ to 5.5 V*4 DGND=AGND=0 V, Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.8×V _{DD}	_		V
Low input voltage	V _{IL}	_	_	_	$0.2 \times V_{DD}$	V
High output voltage	V _{OH}	I _{OH} =-40 μA	V _{DD} -0.3	_	_	V
Low output voltage	V _{OL}	I _{OL} =2 mA	_	_	0.45	٧
High input current *1	I _{IH1}	V _{IH} =V _{DD}	_	_	10	μΑ
High input current *2	I _{IH2}	V _{IH} =V _{DD}	_	_	20	μΑ
Low input currcent *1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current *2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Low input current *3	I _{IL3}	V _{IL} =GND	-400	_	-20	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
	I	No load			10	
Davier davin avincet	I _{DDS1}	Serial register connected	_	_	10	μΑ
Power down current	1	No load		200		
	I _{DDS2}	DRAM connected				μA

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

^{*3} Applies to the input pins with pull-up resistor (ST, SP, PAUSE, DEL) excluding the XT pin.

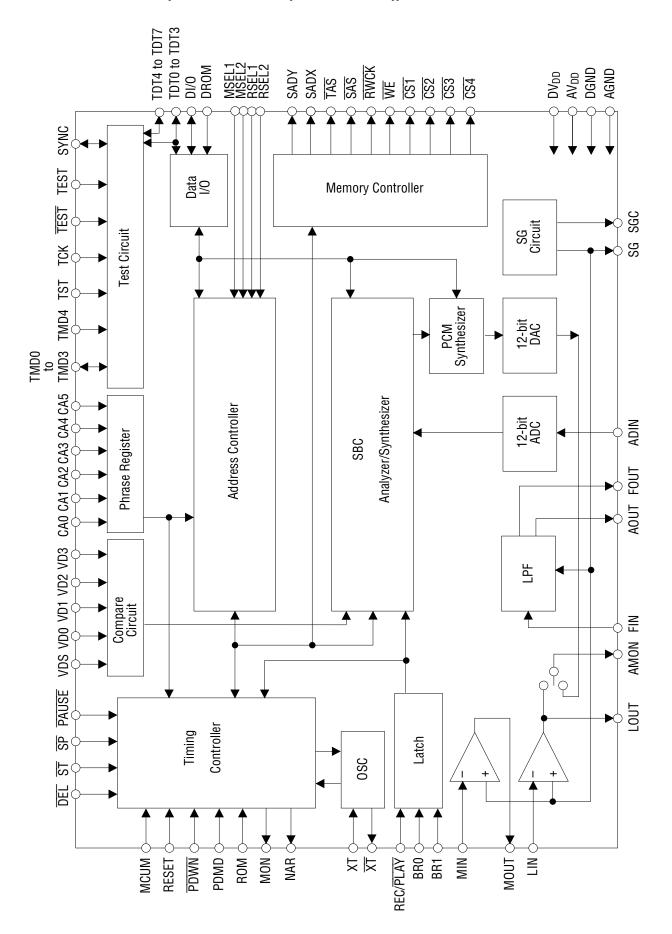
^{*4} The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

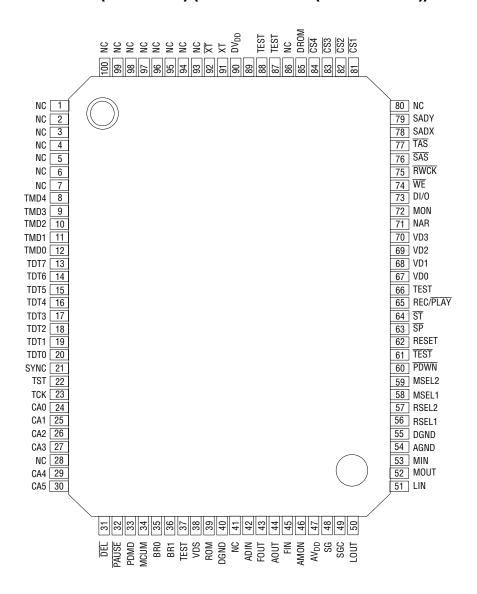
 $\ensuremath{\mathsf{DV_{DD}}}\xspace = 4.5 \text{ to } 5.5 \text{ V} \\ \ensuremath{\mathsf{DGND}}\xspace = 4.5 \text{ AGND} = 0 \text{ V} \\ \ensuremath{\mathsf{Ta=0}}\xspace \text{ to } 70\ensuremath{^\circ\mathsf{C}}\xspace$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	$ V_{DAE} $	no load		_	10	mV
FIN admissible input voltage range	V _{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_	_	ΜΩ
Op-map open loop gain	G _{OP}	f _{IN} =0 to 4kHz	40	_	_	dB
Op-amp input impedance	R _{INA}	_	1	_	_	ΜΩ
Op-amp load resistance	R _{OUTA}	_	200	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	50	_	_	kΩ
FOUT load resistance	R FOUT	_	50	_	_	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3 V Version))



100-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Туре	Description
90	DV_DD		Digital power supply. Insert a bypass capacitor of 0.1 µF or more between this
	DADD		pin and the DGND pin.
47	AV_{DD}	_	Analog power supply. Insert a bypass capacitor of 0.1 μ F or more between this pin and the AGND pin.
40, 55	DGND	_	Digital ground.
54	AGND	_	Analog ground.
48, 49	SG, SGC	_	Output for analog circuit reference voltage (signal ground).
53	MIN		Inverting input of the built-in OP amplifier. The non-inverting input pin is
51	LIN	l	internally connected to SG (signal ground).
52	MOUT	_	
50	LOUT	0	Output of the built-in OP amplifier for MIN and LIN.
46	ANAONI	0	Connected to the LOUT pin in the recording mode and to the DA converter
40	AMON	0	output in the playback mode. This pin connects the built-in LPF input (FIN pin).
45	FIN	1	Input of the built-in LPF.
43	FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
42	ADIN	I	Input of the built-in 12-bit AD converter.
44	AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects
44	AUUT	U	an external speaker drive amplifier.
79	SADY	0	They also connect to SAD pin of serial register and serial voice ROM. These pins
78	SADX	U	output leading addresses of read/write.
			This pin connects to TAS pin of serial register and serial voice ROM.
77	TAS	0	This pin is used to set serial addresses from the SADX and SADY pins into the
			internal address counter of the serial register and serial voice ROM.
76	SAS	0	This pin connects to the SAS pin of the serial register and the SASX and SASY pins
	UAU	0	of the serial voice ROM. Clock pin to write serial addresses.
75	RWCK	0	This pin connects to the RWCK pin of the serial register and the RDCK pin of the
	TIVVOIX	U	serial voice ROM. Clock pin to read data from and write data into the serial register.
74	WE	0	Write Enable. This pin connects to the $\overline{\text{WE}}$ pin of the serial register and DRAM.
	VV L		This pin selects either read or write mode.
73	DI/O	1/0	Data I/O. This pin connects to the DIN and DOUT pins of the serial register and
	<i>D170</i>	1/0	DRAM. This pin outputs write data and inputs read data.
85	DROM	I	Data ROM. This pin connects to the DOUT pin of the serial voice ROM.
81	CS1		
82	CS2	0	Chip Select. These pins connect to \overline{CS} pin of the serial register and the \overline{CS} ($\overline{CS1}$,
83	CS3		CS2, CS3) pins of the serial voice ROM.
84	CS4		

Pin	Symbol	Туре		Description						
58	MSEL1		Those nine cal	These pins select the capacity of the memory to be connected externally.						
59	MSEL2	I	rnese pins sei	ect the capacit	y of the memor	ry to be conne	ected externally.			
			These pins select the number of and serial registers to be connected externallly.							
					MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity	
56	RSEL1	1	L	L	L	L	4M × 1			
57	RSEL2	i	L	L	L	Н	4M × 2			
0,	TIOLLE	•	L	L	Н	L	4M × 3			
			L	L	Н	Н	4M × 4			
			Mode Select	tion.			-			
34	MCUM	1	Low level : Sta	nd-alone mode)					
			High level : Mid	crocontroller ir	iterface mode					
62	RESET	1	A high input le down state.	A high input level causes the MSM6789L to be initialized and to go into the power						
				When a low l	evel is innut th	MSM6780I	goes to the nower down			
			Power Down. When a low level is input, the MSM6789L goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789L to be reset.							
60	PDWN	WN I	When a Low level is applied to this pin during recording operation, the MSM6789L							
00	I DVVIV		is halted, and will be maintained in the power down state while PDWN is low level.							
			· ·		•		recording will be performed.			
			<u> </u>				ed, input the clock through			
91	XT	I					et to the ground level.			
			•				ed, this pin must be left			
92	XT	0	open.			0.001.10 000	, p			
37	TEST		1401407001	P		FFOT who and a	- bish level to the TFOT air			
61	TEST	I	MSM6789L	est. Input a id	ow level to the	i EST pin and a	a high level to the TEST pin.			
9-12	TMD3-TMD0									
13-20	TDT7-TDT0	1/0	MSM6789L	Test. This pin	must be left of	oen.				
21	SYNC									
17-20	TDT3-TDT0	1/0	These pins mu	st be left open	as they are MS	SM6789L test	pins.			
22	TST									
23	TCK	I	MSM6789L	Test. Input a l	ow level signal					
8	TMD4									

Pin	Symbol	Туре						Desc	ription																						
			Playba	ack O	perat	tion. \	Vhen s	set to lo	ow, this pin sele	ects the record/playback																					
39	ROM	I	operation	operation (only for the SBC method). When set to high, it selects the ROM playbac																											
			operation	peration (for the SBC and PCM methods).																											
				_		_	_			This pin is invalid during																					
65	REC/PLAY	I		e ROM playback operation. When set to low, it selects the playback mode.																											
				en set to high, it selects the recording mode.																											
64	ST	ı						evel pu	ilse is applied to	o this pin, the record/playbac																					
			or ROM					النجا احتيا		this wise the ware and /mlasshage																					
63	SP	I	or ROM	_				vei pui	se is applied to	this pin, the record/playback																					
								-level n	ulse is annlied t	o this pin, the record/playbac																					
32	PAUSE	I	or ROM					•		o tino pin, the record/playbac																					
																			to this pin, all phrase deletion												
		EL I	or specified phrase deletion can be performed according to the setting of pir						·																						
0.4	DEL		through CA5,																												
31	DEL		ch00:All phrase deletion																												
					ch01 to ch3F:Specified phrase deletion																										
										nen delete all phrases.																					
			After co	mplet	ing thi	s proc	edure,	start t	he record/playb	pack operation.																					
			Desire			-																									
				-			-		ndepedently for	the record/playback operatio																					
			and the	ROM	playba	ack op	eration	1.																							
			CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.	Remarks																					
			L	L	L	L	L	L	ch00	All phrase deletion																					
24-30	CA0-CA5	1	ı	I	I	I	I	1	ı	1			ı		ı	ı	1				1		ı	L	L	L	L	L	Н	ch01	
			L	L	L	L	Н	L	ch02	A total of 63 phrases can																					
			:	:	:	:	:	:	:	be used for both record /playback and ROM																					
			Н	Н	Н	Н	Н	L	ch3E	playback operation.																					
								1		p.s.y saon opolation.																					

Pin	Symbol	Туре	Description					
				-		-	ypes of bit rate (master OM playback operation.	
				BR1	BR0	Bit rate		
35	BRO			L	L	16.0 kbps		
36	BR1	'		L	Н	12.6 kbps		
				Н	L	10.0 kbps		
				Н	Н	Unused		
			Transition to	the Power	-down Sta	te.		
			Low level:	The MSM678	9L automatio	cally goes to the power	r-down state, except	
		DMD*1 I		when the red	cord/playbac	k operation is perform	ned.	
	PDMD*1 I		High level: The MSM6789L automatically goes to the standby state, instead of the					
33			power-down state, except when the record/playback operation					
			is performed. In this case, the MSM6789L can be placed in the					
				•	-	-	WN pin to a high level.	
						ed for the built-in LPF,	-	
			Those pine set			lying a high level to the		
67-70	VD0-VD3	I	elimination.	ille voice dete	ct level for th	e voice triggered start	ing and unvoiced-part	
				the voice tria	nered starting	or the unvoiced-part (elimination.	
				ered starting:	•	th level to the VDS pin.		
			detect level with VD0 to VD3 pins.					
38	VDS	I	Unvoiced-p	art elimination	:Input a Low	level to the VDS pin. T	hen set the voice	
					detect leve	I with VD0 to VD3 pins	S.	
			Note: When neither the voice triggered starting nor the unvoiced-part elimination is					
			used, input a L	ow level to VD	0 to VD3.			
72	MON	0	This pin output	ts a high level	while the re	cord/playback operation	on is being performed.	
						tate of the operation f		
71	NAR	0	1.			k is performed, the ne	xt phrase can	
			be specified aft	ter the NAR pi	n goes to hi	gh positively.		

 $^{^{*}1}$ When DRAM is selected, be sure to set the PDMD pin to a High level.

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	٧
Input voltage	V _{IN}	Ta=25°C	-0.3 to V _{DD} +0.3	٧
Storage temperature	T _{STG}	_	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	f _{OSC}	_	6.0 to 8.192	MHz

ELECTRICAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = 3.0$ to 3.6 V DGND=AGND=0 V, Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	$0.85 \times V_{DD}$	_	_	V
Low input voltage	V _{IL}	_	_	_	$0.15 \times V_{DD}$	V
High output voltage	V _{OH}	I _{OH} =-40 μA	V _{DD} -0.3	_	_	V
Low output voltage	V _{OL}	I _{OL} =2 mA		_	0.45	V
High input current *1	I _{IH1}	V _{IH} =V _{DD}	_	_	10	μΑ
High input current *2	I _{IH2}	V _{IH} =V _{DD}	_	_	20	μΑ
Low input currcent *1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current *2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Low input current *3	I _{IL3}	V _{IL} =GND	-400	_	-20	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
	1	No load			10	Δ.
Power down current	I _{DDS1}	Serial register connected	_	_	10	μΑ
FOWEI WOWII CUITEIIL	l	No load		200	_	_
	I _{DDS2}	DRAM connected	_			μΑ

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

^{*3} Applies to the input pins with pull-up resistor (ST, SP, PAUSE, DEL) excluding the XT pin.

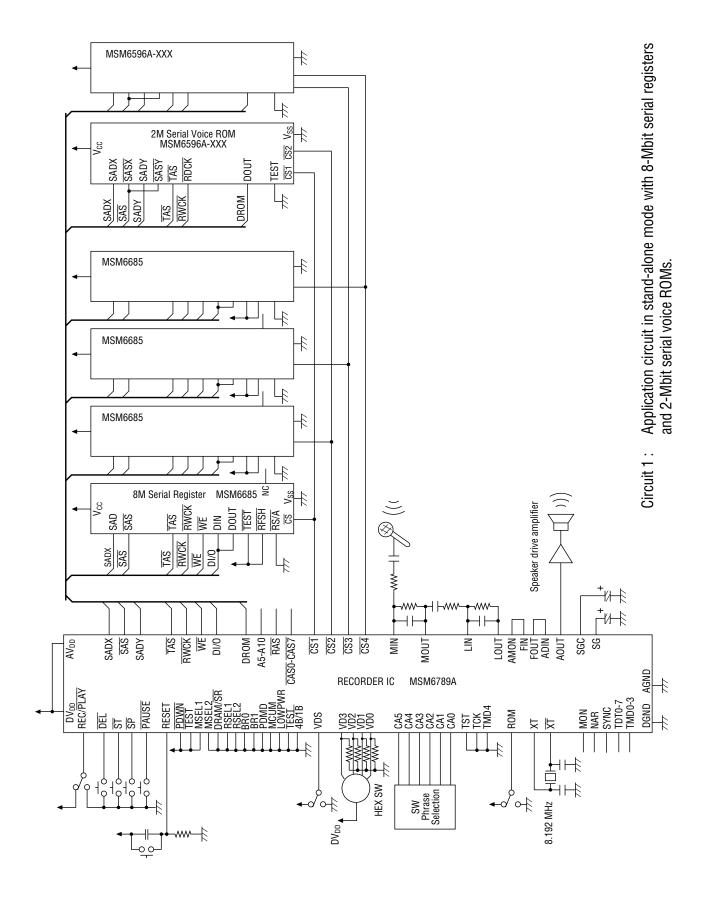
Analog Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = \ensuremath{\mathsf{AV_{DD}}}\xspace = 3.0 \ \ensuremath{\mathsf{to}} \ 3.6 \ \ensuremath{\mathsf{V}} \\ \ensuremath{\mathsf{DGND}}\xspace = \ensuremath{\mathsf{AGND}}\xspace = 0 \ \ensuremath{\mathsf{V}} \xspace \ \ensuremath{\mathsf{Ta=0}}\xspace \ \ensuremath{\mathsf{to}} \xspace \ \ensuremath{\mathsf{70^{\circ}C}}\xspace$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	$ V_{DAE} $	no load	_	_	20	mV
FIN admissible input voltage range	V _{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_	_	MΩ
Op-map open loop gain	G _{OP}	f _{IN} =0 to 4kHz	40			dB
Op-amp input impedance	R _{INA}	_	1	_	_	MΩ
Op-amp load resistance	R _{OUTA}	_	400			kΩ
AOUT load resistance	R _{AOUT}	_	100	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	100	_	_	kΩ

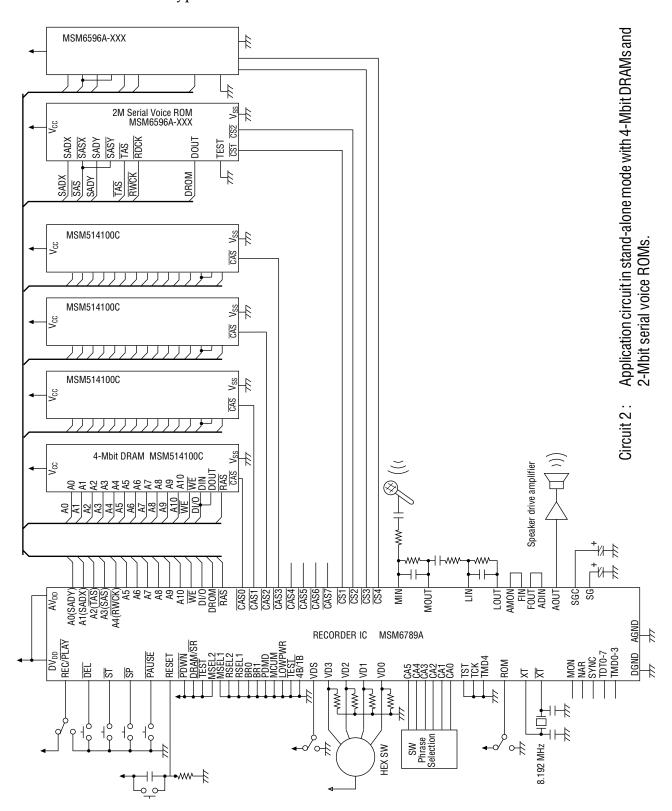
APPLICATION CIRCUITS (for MSM6789A (5 V version))

This is an application circuit example when the MSM6789A is used in stand-alone mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.



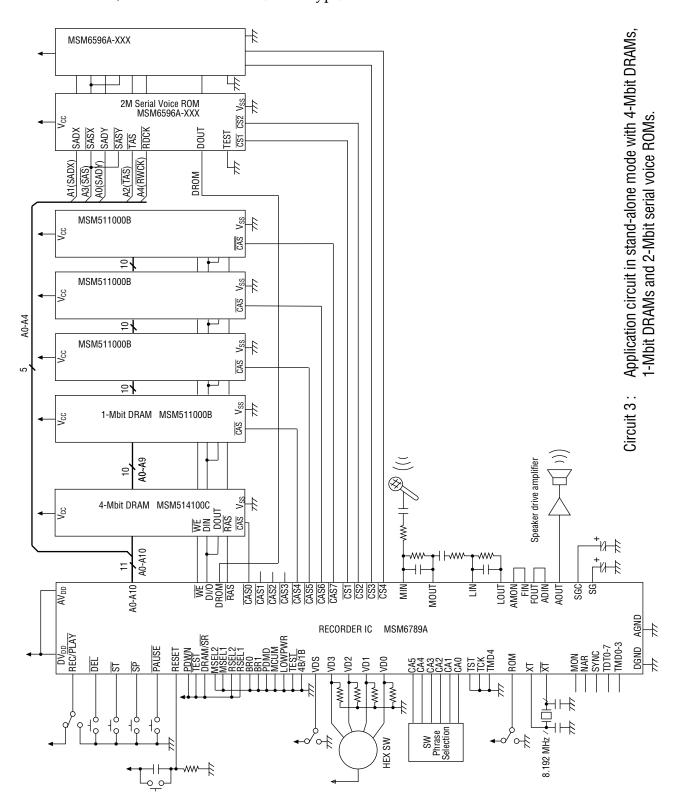
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



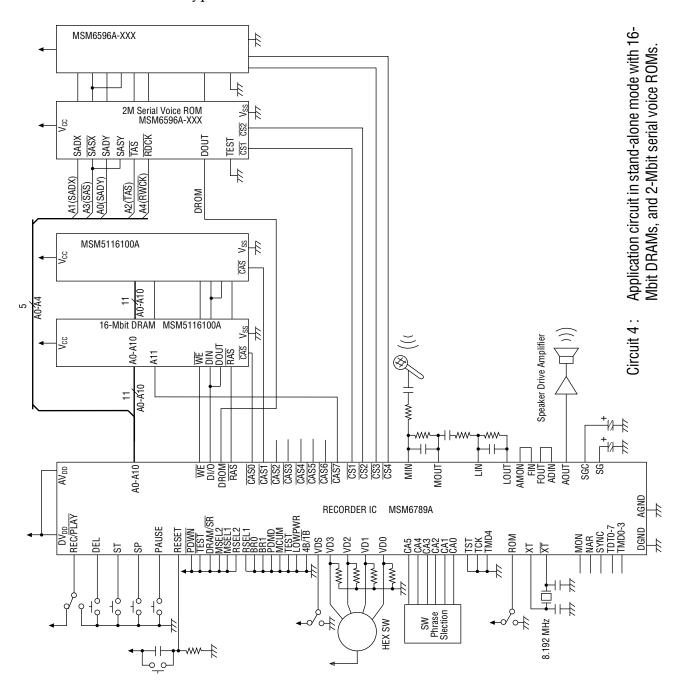
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.



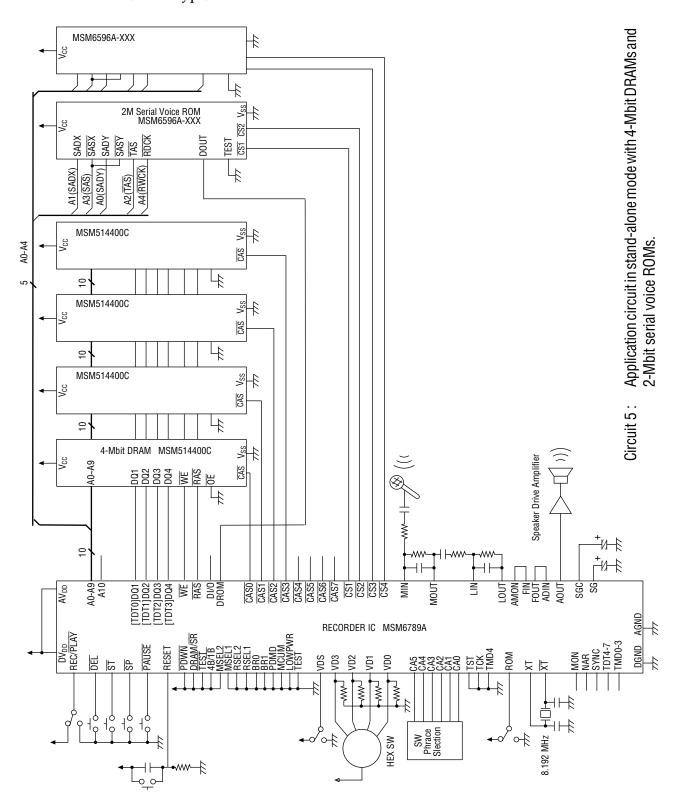
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (1-bit \times type) and two 2-Mbit serial voice ROMs.



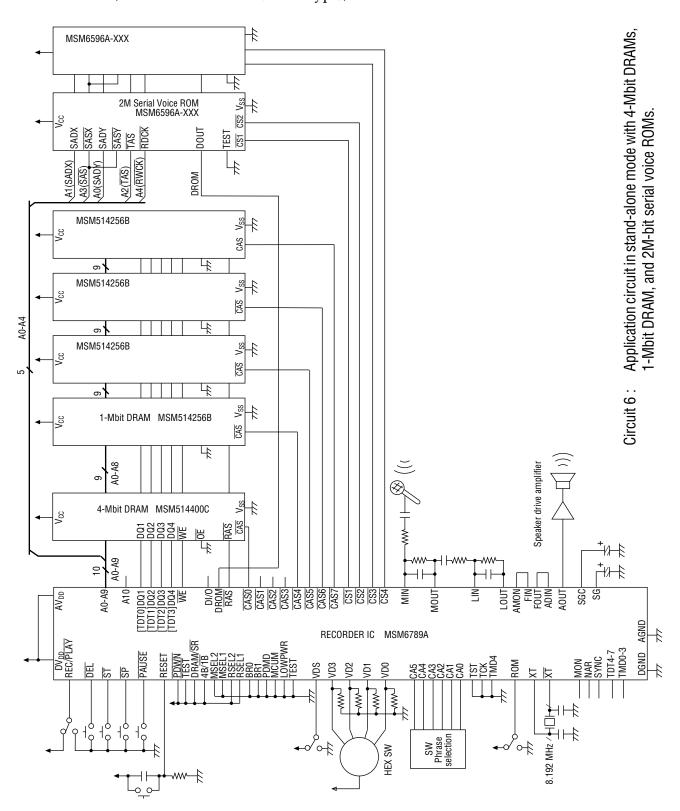
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with four 4-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



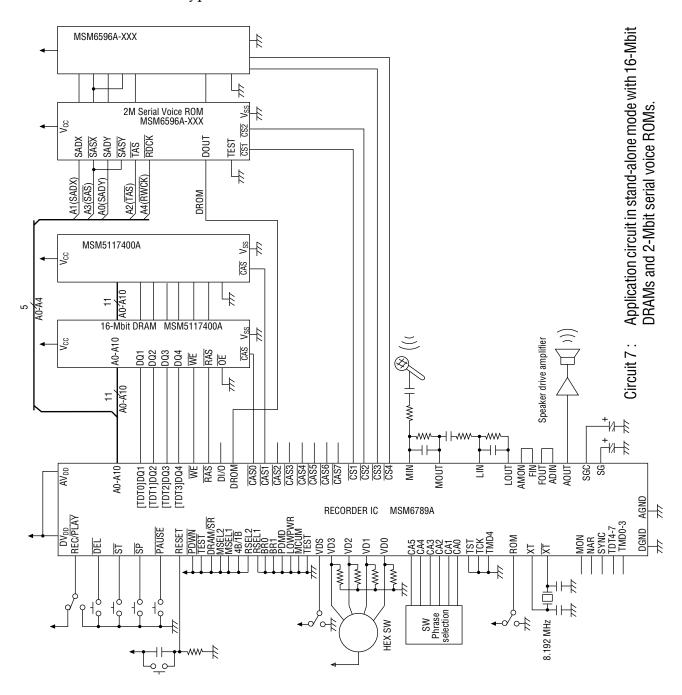
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.



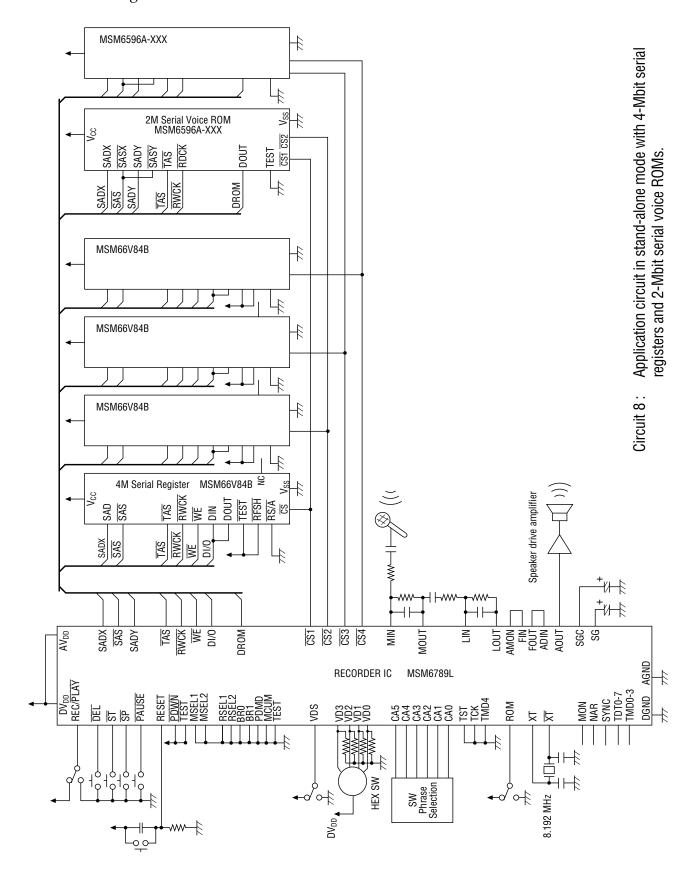
APPLICATION CIRCUITS (for MSM6789A (5 V version)) (Continued)

This is an application circuit example when the MSM6789A is used in stand-alone mode with two 16-Mbit DRAMs (4-bit \times type) and two 2-Mbit serial voice ROMs.



APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in stand-alone mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.



MICROCONTROLLER INTERFACE MODE

FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in 12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter

Attenuation characteristics –40 dB/oct

• External memories

MSM6789A (5 V version)

General-purpose DRAM, 32 Mbits maximum (for variable messages)

1-Mbit DRAM: Can be directly driven (MSM514256B, MSM511000B)

4-Mbit DRAM: Can be directly driven (MSM514400C, MSM514100C)

16-Mbit DRAM: Can be directly driven (MSM5117400A, MSM5116100A)

ARAM, 32 Mbits maximum (for variable messages)

Note: Use the first 64 Kbits with no failed bits for the ARAM.

Serial register, 32 Mbits maximum (for variable messages)

4-Mbit serial register: Can be directly driven (MSM6684B)

8-Mbit serial register : Can be directly driven (MSM6685)

MSM6789L (3.3 V version)

Serial register, 16 Mbits maximum (for variable messages)

4-Mbit serial register: Can be directly driven (MSM66V84B)

MSM6789A (5 V version) and MSM6789L (3.3 V version)

Serial voice ROM, 4 Mbits maximum (for fixed messages)

1-Mbit serial voice ROM: Can be directly driven (MSM6595A)

2-Mbit serial voice ROM: Can be directly driven (MSM6596A)

3-Mbit serial voice ROM: Can be directly driven (MSM6597A)

• Bit rate

10.0, 12.6, 16.0 kbps (at 8 kHz sampling freq.)

7.5, 9.5, 12.0 kbps (at 6 kHz sampling freq.)

• Maximum recording time (when one 8-Mbit serial register is connected)

13.8 minutes (for 10.0 kbps SBC)
11.0 minutes (for 12.6 kbps SBC)
14.6 minutes (for 9.5 kbps SBC)

8.6 minutes (for 16.0 kbps SBC)

11.5 minutes (for 12.0 kbps SBC)

• Number of phrases

63 phrases for variable messages

255 phrases for fixed messages

- Standard linear PCM playback or OKI nonlinear PCM playback can be selected.
- Voice triggered starting function (voice detect level can be set)
- Uuvoiced-part elimination function (voice detect level can be set)
- Pausing function

• Master clock frequency: 6.0 MHz to 8.192 MHz

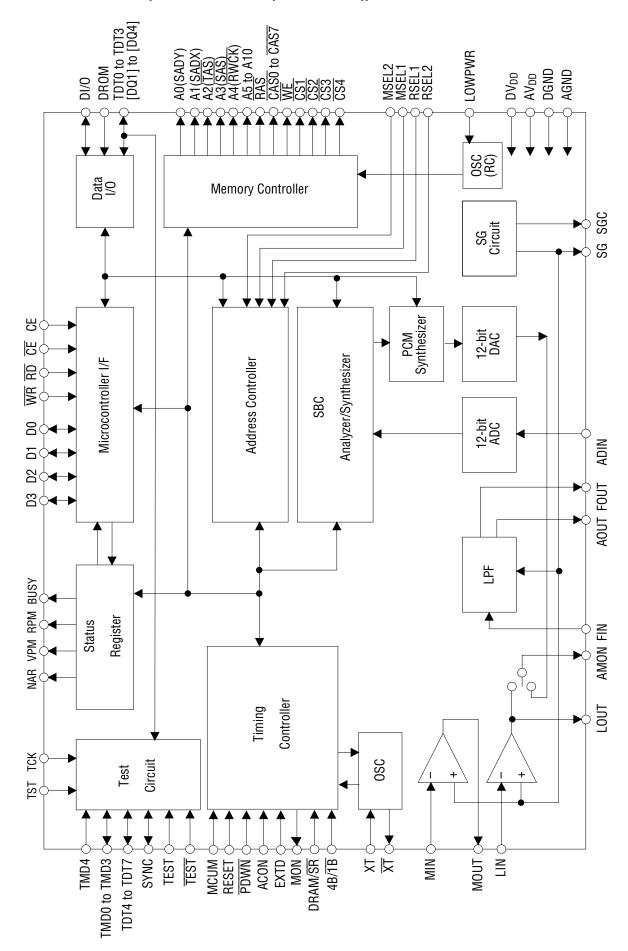
• Power supply voltage:

MSM6789A: Single 5 V power supply MSM6789L: Single 3.3 V power supply

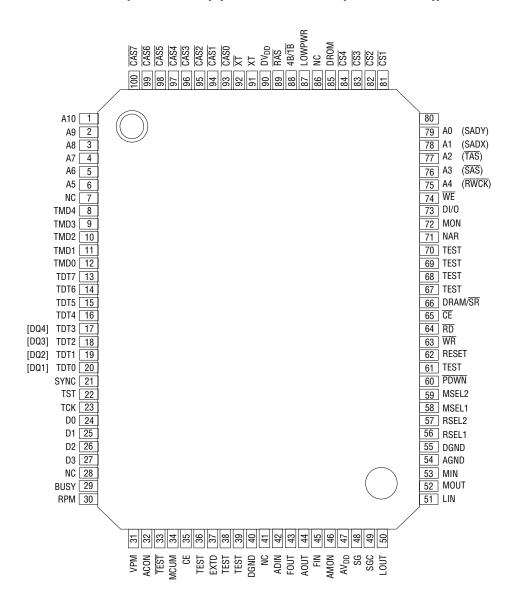
Package options:

MSM6789A: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789AGS-BK) MSM6789L: 100-pin plastic QFP (QFP100-P-1420-BK) (Product name: MSM6789LGS-BK)

BLOCK DIAGRAM (for MSM6789A (5 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789A (5 V Version))



100-Pin Plastic QFP

(): Pins for connecting serial voice ROM.[]: Pins for connecting 4-bit × type DRAM.

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789A (5 V Version))

Pin	Symbol	Туре	Description
90	DV _{DD}	_	Digital power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this pin and the DGND pin.
47	AV _{DD}		Analog power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this pin and the AGND pin.
40, 55	DGND	_	Digital ground.
54	AGND	_	Analog ground.
48, 49	SG, SGC	0	Output for analog circuit reference voltage (signal ground).
53	MIN		Inverting input of the built-in OP amplifier. The non-inverting input pin is
51	LIN	l	internally connected to SG (signal ground).
52 50	MOUT LOUT	0	Output of the built-in OP amplifier for MIN and LIN.
46	AMON	0	Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. This pin connects the built-in LPF input (FIN pin).
45	FIN	l	Input of the built-in LPF.
43	FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
42	ADIN	l	Input of the built-in 12-bit AD converter.
44	AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier.
66	DRAM/SR	I	This pin selects whether memory to be connected externally is DRAM or serial register. Low level: Serial register High level: DRAM
88	4B/1B	I	This pin selects either 1-bit \times type DRAM or 4-bit \times type DRAM. Low level : 1-bit \times type High level : 4-bit \times type
79 78	A0 (SADY) A1 (SADX)	0	These pins connect to A0 and A1 of DRAM at the time of DRAM selection. They also connect to SAD pin of serial register and serial voice ROM at the time of serial register selection. These pins output leading addresses of read/write.
77	A2 (TAS)	0	This pin connects to A2 of DRAM at the time of DRAM selection. It also connects to TAS pin of serial register and serial voice ROM at the time of serial register selection. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	A3 (SAS)	0	This pin connects to A3 of DRAM at the time of DRAM selection. It also connects to the SAS pin of the serial register and the SASX and SASY pins of the serial voice ROM at the time of serial register selection. Clock pin to write serial addresses.
75	A4 (RWCK)	0	This pin connects to A4 of DRAM at the time of DRAM selection. It also connects to the \overline{RWCK} pin of the serial register and the \overline{RDCK} pin of the serial voice ROM at the time of serial register selection. Clock pin to read data from and write data into the serial register.
1-6	A10-A5	0	These pins connect to pins A5-A10 of DRAM at the time of DRAM selection. These pins output addresses of read/write.

Pin	Symbol	Туре		Description						
74	WE		Write Enable.	This pin conn	ects to the WE	pin of the seri	al register and DRAM.			
74	WE	0	This pin selects	either read or v	write mode.					
73	DI/O	1/0	Data I/O. This	pin connects t	o the DIN and	DOUT pins of	the serial register and			
	<i>D</i> 1,7 C	.,, 0	DRAM. This pin	is used to outp	out write data a	and inputs read	d data.			
85	DROM	I		Data ROM. This pin connects to the DOUT pin of the serial voice ROM.						
89	RAS	0	This is a row add	•						
93-100	CASO- CAS7	0	CAS7, an addres	ese are the column address strobe pins of DRAM at the time of DRAM selection. AS7, an addresss output pin, is connected to pin A11 of DRAM at the time of 16-bit DRAM selection.						
81	CS1									
82	CS2		Chip Slect. Th	ese pins conne	ect CS pin of th	ne serial regist	er and the $\overline{\text{CS}}$ ($\overline{\text{CS1}}$,			
83	CS3	0	$\overline{\text{CS2}}, \overline{\text{CS3}})$ pins (of the serial vo	ice ROM.					
84	CS4									
58	MSEL1	l	These pins selec	t the canacity	of the memory	to he connect	ad avtarnally			
59	MSEL2	I	These pins selec	t the capacity		to be connect	eu externally.			
				externallly. • When DRAM MSEL2		$\frac{ RAM/\overline{SR} = Hig}{ RSEL2}$	-	Memory capacity		
			L	L	L	L	1M × 4			
			L	L	L	Н	4M × 1			
			L	L	Н	L	1M × 8			
			L	L	Н	Н	$1M \times 4 + 4M \times 1$			
			L	Н	L	L	4M × 2			
56	RSEL1		L	Н	L	Н	4M × 2			
57	RSEL2		L	Н	Н	L	4M × 3			
O1	HOLLE	'	L	Н	Н	Н	4M × 3			
			Н	L	L	L	4M × 4			
			Н	L	L	Н	16M × 1			
			Н	L	Н	L	4M × 6			
			Н	L	Н	Н	4M × 6			
			H	Н	L	L	4M × 8			
			H	Н	L	Н	4M × 8			
			H	Н	Н	L	16M × 2			
			H	Н	Н	Н	16M × 2			
				11	11	11	TOWI A Z			

Pin	Symbol	Туре			Descrip	tion				
			• When serial	register is sele	cted (DRAM/SI	\overline{R} = Low level)				
			MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity			
			L	L	L	L	4M × 1			
			L	L	L	Н	4M × 2			
56	RSEL1		L	L	Н	L	4M × 3			
57	RSEL2		L	L	Н	Н	4M × 4			
01	TIOLLE		L	Н	L	L	8M × 1			
			L	Н	L	Н	8M×2			
			L	Н	Н	L	8M × 3			
			L	Н	Н	Н	8M × 4			
87	LOWPWR	I	This pin selects power down wh Low level : 15 µ High level : 125	en DRAM is se s max. µs max.	•	iod of DRAM a	at the time of			
34	MCUM	I	Low level : Stan							
			-	High level : Microcontroller interface mode						
62	RESET	ı		el causes the N	ISM6789A to	be initialized a	nd to go into the power			
			down state.	140		401407004				
60	PDWN	I	state. Unlike the l When an Low le is halted, and wil	Power Down. When a low level is input the MSM6789A goes to the power down state. Unlike the RESET pin, this pin does not force the MSM6789A to be reset. When an Low level is applied to this pin during recording operation, the MSM6789A is halted, and will be maintained in the power down state while PDWN is low level. After this pin is restored to a high level, postprocessing for recording will be						
24	D0									
25	D1	1/0	Bidirectional dat	ta bus to trans	fer commands	and data to a	nd from an external			
26	D2	1/0	microcontroller.							
27	D3									
63	WR	I	Write Pulse Into be input via D	-	g a low pulse t	o WR pin caus	ses a command or data			
64	RD	I		•	g a low pulse t	o RD pin caus	es status bits or data to			
65 35	CE CE	I	be output via D0 to D3 pins. Chip Enable Input. When the $\overline{\text{CE}}$ pin is set to low level and the CE pin is set to a high level, the write pulse ($\overline{\text{WR}}$) or read pulse ($\overline{\text{RD}}$) can be accepted. When the $\overline{\text{CE}}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{\text{WR}}$) and read pulse ($\overline{\text{RD}}$) cannot be accepted so that data cannot be communicated via D0 to D3 pins.							

Pin	Symbol	Туре	Description
29	BUSY	0	Busy. This pin outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0 to D3 pins. The state of this pin is the
			same as the contents of the BUSY bit of the status register.
30	RPM	0	RPM. This pin outputs a high level during recording or playback operation. The state of this pin is the same as the contents of the RPM bit of the status register.
31	VPM	0	VPM. This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	0	NAR. This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	Pop Noise Suppression Select. This pin selects whether the pop noise suppression circuit is used. Low level: the pop noise suppression circuit is not used. High level: the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	EXTD. In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	Oscillator Connect. When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	XT	0	Oscillator Connect. When an external clock is uesd, this pin must be left open.
72	MON	0	MON. This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70 33	TEST TEST	I	MSM6789A Test. Input a low level to the TEST pin and a high level to the TEST pin.
9-12	TMD3-TMD0		
13-20	TDT7-TDT0	1/0	MSM6789A Test. This pin must be left open.
21	SYNC		
17-20	TDT3-TDT0 [DQ4]-[DQ1]	1/0	Connect these pins to DQ1 to DQ4 of DRAM at the time of 4-bit \times type DRAM selection. Otherwise these pins must be left open as they are MSM6789A test pins.
22	TST		
23	TCK	I	MSM6789A Test. Input a low level.
8	TMD4		

ABSOLUTE MAXIMUM RATINGS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	V _{IN}	Ta=25°C	−0.3 ~ V _{DD} +0.3	V
Storage temperature	T _{STG}	_	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789A (5 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.5 to +5.5*3	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	fosc	_	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789A (5 V Version))

DC Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = 4.5 \text{ to } 5.5 \ensuremath{\:\mathsf{V^{*3}}}\xspace$ DGND=AGND=0 V $\ensuremath{\:\mathsf{Ta=0}}\xspace$ to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.8×V _{DD}	_	_	V
Low input voltage	V _{IL}	_	_	_	$0.2 \times V_{DD}$	V
High output voltage	V _{OH}	I _{OH} =-40 μA	V _{DD} -0.3	_	_	V
Low output voltage	V _{OL}	I _{OL} =2 mA		_	0.45	V
High input current ^{*1}	I _{IH1}	$V_{IH}=V_{DD}$	_		10	μΑ
High input current*2	I _{IH2}	$V_{IH}=V_{DD}$		_	20	μΑ
Low input current*1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current*2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load		20	35	mA
Power down current	I _{DDS1}	No load		_	10	
		Serial register connected	_			μΑ
	I _{DDS2}	No load		200	_	μА
		DRAM connected				

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

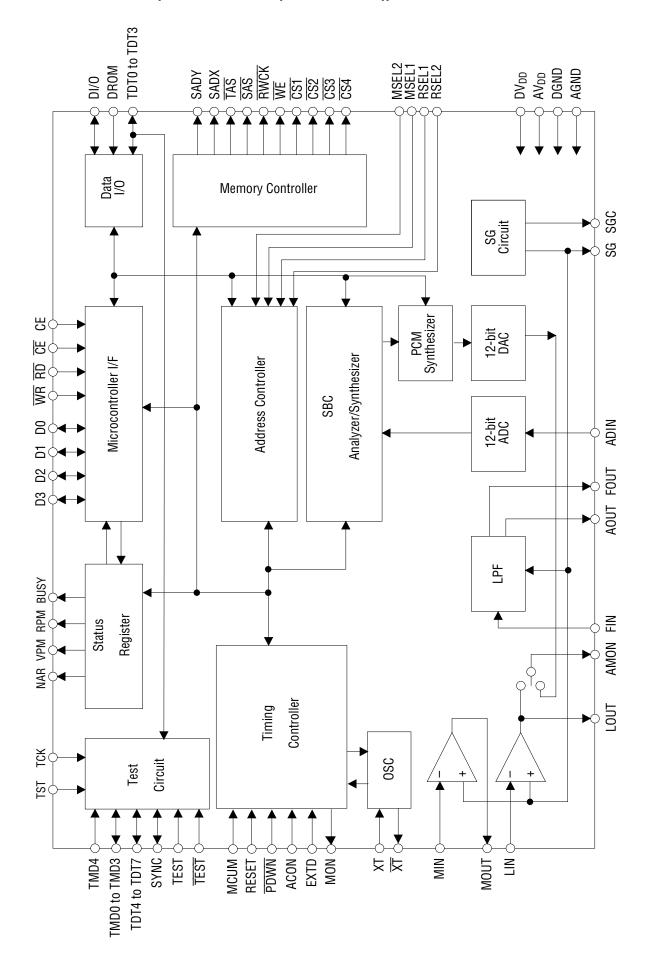
^{*3} The record/playback operation must be performed at the power supply voltage of 4.5 to 5.5 V. The MSM6789A operates at 3.5 to 5.5 V when the serial register is backed up.

Analog Characteristics

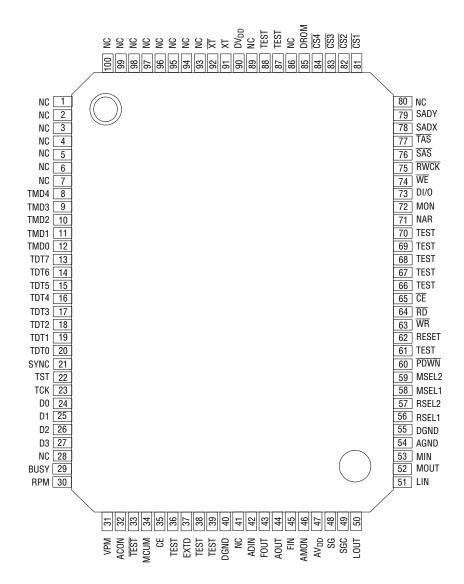
DV_{DD}=AV_{DD}=4.5 to 5.5 V DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	$ V_{DAE} $	No load			10	mV
FIN admissible input voltage range	V _{FIN}	_	1	_	V _{DD} -1	V
FIN input impedance	R _{FIN}	_	1	_	_	MΩ
OP-amp open loop gain	G _{OP}	f _{IN} =0 to 4 kHz	40	_		dB
OP-amp input impedance	R _{INA}	_	1	_	_	MΩ
OP-amp load resistance	R _{OUTA}	_	200	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	50	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	50	_	_	kΩ

BLOCK DIAGRAM (for MSM6789L (3.3 V Version))



PIN CONFIGURATION (TOP VIEW) (for MSM6789L (3.3V Version))



100-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version))

Pin	Symbol	Туре	Description
90	DV_DD	_	Digital power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this pin and the DGND pin.
47	AV _{DD}	_	Analog power supply. Insert a bypass capacitor of $0.1\mu F$ or more between this pin and the AGND pin.
40, 55	DGND		Digital ground.
54	AGND	_	Analog ground.
48, 49	SG, SGC	0	Output for analog circuit reference voltage (signal ground).
53	MIN		Inverting input of the built-in OP amplifier. The non-inverting input pin is
51	LIN		internally connected to SG (signal ground).
52 50	MOUT LOUT	0	Output of the built-in OP amplifier for MIN and LIN.
46	AMON	0	Connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. This pin connects the built-in LPF input (FIN pin).
45	FIN	ı	Input of the built-in LPF.
43	FOUT	0	Output of the built-in LPF. This pin connects the AD converter input (ADIN pin).
42	ADIN	I	Input of the built-in 12-bit AD converter.
44	AOUT	0	Output of the built-in LPF. This pin outputs playback waveforms and connects an external speaker drive amplifier.
79	SADY		These pins connect to SAD pin of serial register and serial voice ROM. These pins
78	SADX	0	output leading addresses of read/write.
77	TAS	0	This pin connects to TAS pin of serial register and serial voice ROM. This pin is used to set serial addresses from the SADX and SADY pins into the internal address counter of the serial register and serial voice ROM.
76	SAS	0	This pin connects to the \overline{SAS} pin of the serial register and the \overline{SASX} and \overline{SASY} pins of the serial voice ROM. Clock pin to write serial addresses.
75	RWCK	0	This pin connects to the \overline{RWCK} pin of the serial register and the \overline{RDCK} pin of the serial voice ROM. Clock pin to read data from and write data into the serial register.
74	WE	0	Write Enable. This pin connects to the \overline{WE} pin of the serial register and DRAM. This pin selects either read or write mode.
73	DI/O	1/0	Data I/O. This pin connects to the DIN and DOUT pins of the serial register and DRAM. This pin is used to output write data and inputs read data.
85	DROM	I	Data ROM. This pin connects to the DOUT pin of the serial voice ROM.
81	CS1		
82	CS2		Chip Slect. These pins connect \overline{CS} pin of the serial register and the \overline{CS} ($\overline{CS1}$,
83	0		CS2, CS3) pins of the serial voice ROM.
84	CS4		
58	MSEL1	I	These pine colors the conseity of the memory to be connected systematic.
59	MSEL2	I	These pins select the capacity of the memory to be connected externally.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

Pin	Symbol	Туре			Descri	ption	
			These pins se externallly.	lect the numb	er of serial reg	isters to be co	onnected
56	RSEL1		MSEL2	MSEL1	RSEL2	RSEL1	Memory capacity
57	RSEL2	i	L	L	L	L	4M ×1
•	1.0222		L	L	L	Н	4M × 2
			L	L	Н	L	4M × 3
			L	L	Н	Н	4M × 4
34	MCUM	I	Mode Selecti Low level : Stan High level : Mic	d-alone mode			
62	RESET	I	A high input lev down state.	el causes the	MSM6789L to	o be initialized	and to go into the power
60	PDWN	I	state. Unlike the When an Low le is halted, and wi	RESET pin, this vel is applied t Il be maintaine	s pin does not to this pin dur d in the power	force the MSN ing recording down state w	loes to the power down 16789L to be reset. operation, the MSM6789L hile PDWN is low level. for recording will be
24	D0						
25	D1	1.00	Bidirectional da	ta bus to trans	sfer command	ls and data to	and from an external
26	D2	1/0	microcontroller	•			
27	D3						
63	WR	ı	Write Pulse Into be input via [-		to WR pin ca	uses a command or data
64	RD	ı	Read Pulse In be output via Do	-	ng a low pulse	to RD pin ca	uses status bits or data to
65 35	CE CE	I	high level, the w	vrite pulse (W n is set to a hi pulse (RD) ca	R) or read pul	se (RD) can be pin is set to	el and the CE pin is set to a be accepted. a low level, the write pulse ata cannot be communicated
29	BUSY	0	Busy. This pin	outputs a hig , do not apply	any data to D	0 to D3 pins.	being executed. When this The state of this pin is the ter.
30	RPM	0			J	•	playback operation. The bit of the status register.

PIN DESCRIPTIONS (for MSM6789L (3.3 V Version)) (Continued)

Pin	Symbol	Туре	Description
31	VPM	0	VPM. This pin outputs a high level during standby for voice incoming after the start of recording by voice triggered starting or unvoiced-part elimination. Also outputs a high level when the record/playback is stopped temporarily by inputting the PAUSE command. The state of this pin is the same as the contents of the VPM bit of the status register.
71	NAR	0	NAR. This NAR pin indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after verifying that the NAR pin is at high level and input the START command.
32	ACON	I	Pop Noise Suppression Select. This pin selects whether the pop noise suppression circuit is used. Low level: the pop noise suppression circuit is not used. High level: the pop noise suppression circuit is used. The DC level is shifted by the LEV command.
37	EXTD	I	EXTD. In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
91	XT	I	Oscillator Connect. When an external clock is used, input the clock through this pin. At the power-down state, this pin must be set to the ground level.
92	XT	0	Oscillator Connect. When an external clock is uesd, this pin must be left open.
72	MON	0	MON. This pin outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
36, 37-39, 61, 67-70 33	TEST TEST	I	MSM6789L Test. Input a low level to the TEST pin and a high level to the TEST pin.
9-12	TMD3-TMD0		
13-20	TDT7-TDT0	1/0	MSM6789L Test. This pin must be left open.
21	SYNC		
17-20	TDT3-TDT0	I/O	These pins must be left open as they are MSM6789L test pins.
22	TST		
23	TCK	I	MSM6789L Test. Input a low level.
8	TMD4		

ABSOLUTE MAXIMUM RATINGS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	V _{IN}	Ta=25°C	−0.3 ~ V _{DD} +0.3	V
Storage temperature	T _{STG}	_	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (for MSM6789L (3.3 V Version))

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	DGND=AGND=0 V	+3.0 to +3.6	V
Operating temperature	T _{op}	_	0 to +70	°C
Master clock frequencuy	f _{OSC}	_	6.0 to 8.192	MHz

ELECTRIAL CHARACTERISTICS (for MSM6789L (3.3 V Version))

DC Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = 4.0 \ensuremath{\mathsf{VDD}}\xspace = 3.0 \ensuremath{\mathsf{to}}\xspace 3.6 \ensuremath{\mathsf{V}}\xspace$ DGND=AGND=0 V Ta=0 to 70°C

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High input voltage	V _{IH}	_	0.85×V _{DD}	_	_	V
Low input voltage	V _{IL}	_	_	_	0.15×V _{DD}	V
High output voltage	V _{OH}	Ι _{0H} =-40 μΑ	V _{DD} -0.3	_	_	V
Low output voltage	V _{OL}	I _{OL} =2 mA	_	_	0.45	V
High input current*1	I _{IH1}	V _{IH} =V _{DD}	_	_	10	μΑ
High input current*2	I _{IH2}	V _{IH} =V _{DD}	_	_	20	μΑ
Low input current*1	I _{IL1}	V _{IL} =GND	-10	_	_	μΑ
Low input current*2	I _{IL2}	V _{IL} =GND	-20	_	_	μΑ
Operating current consumption	I _{DD}	f _{OSC} =8 MHz, no load	_	20	35	mA
	1	No load			10	μА
Power down current	I _{DDS1}	Serial register connected	_	_		
	1	No load		200		
	I _{DDS2}	DRAM connected		200		μΑ

^{*1} Applies to all inputs excluding the XT pin.

^{*2} Applies to the XT pin.

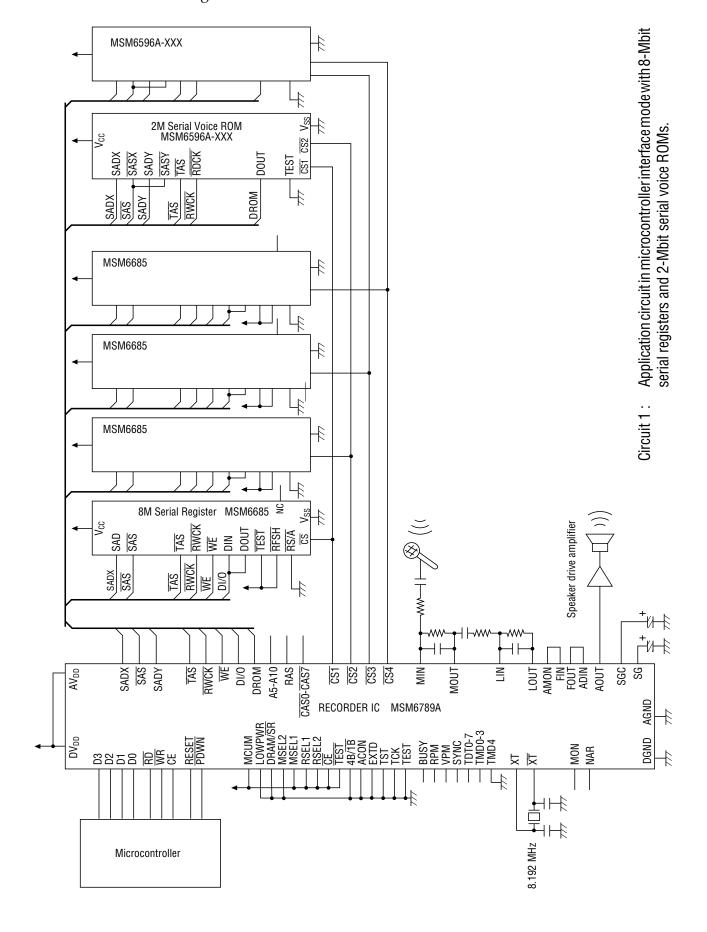
Analog Characteristics

 $\ensuremath{\mathsf{DV_{DD}}}\xspace = \ensuremath{\mathsf{AV_{DD}}}\xspace = 3.0 \ \ensuremath{\mathsf{to}} \ 3.6 \ \ensuremath{\mathsf{V}} \\ \ensuremath{\mathsf{DGND}}\xspace = \ensuremath{\mathsf{AGND}}\xspace = 0 \ \ensuremath{\mathsf{V}} \xspace \ \ensuremath{\mathsf{Ta=0}}\xspace \ \ensuremath{\mathsf{to}} \xspace \ \ensuremath{\mathsf{70^{\circ}C}}\xspace$

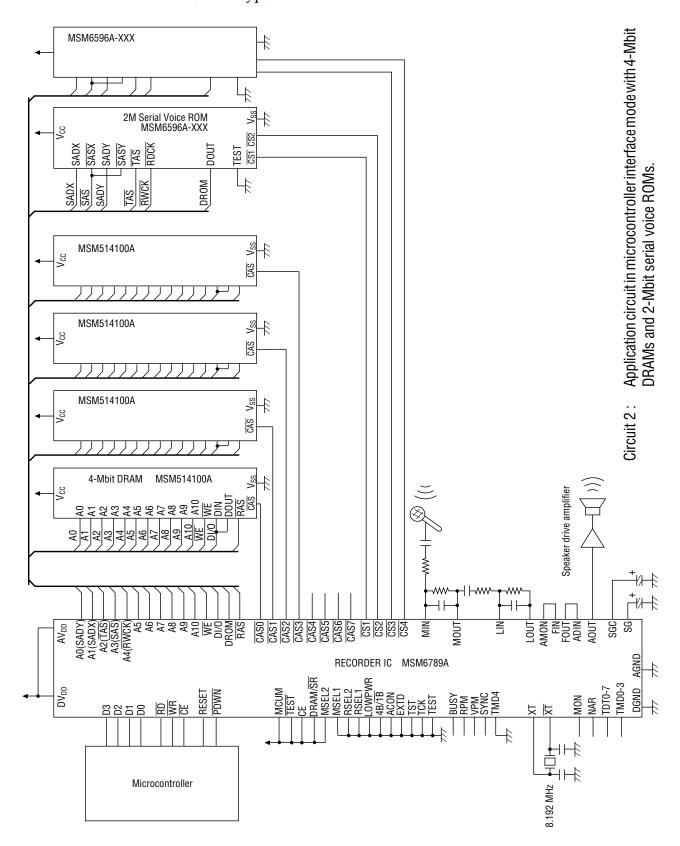
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
DA output relative error	$ V_{DAE} $	No load		_	20	mV
FIN admissible input voltage range	V_{FIN}	_	1		V _{DD} -1	V
FIN input impedance	R_{FIN}	_	1	_	_	MΩ
OP-amp open loop gain	G _{OP}	f _{IN} =0 to 4 kHz	40	_		dB
OP-amp input impedance	R _{INA}	_	1	_	_	MΩ
OP-amp load resistance	R _{OUTA}	_	400	_	_	kΩ
AOUT load resistance	R _{AOUT}	_	100	_	_	kΩ
FOUT load resistance	R _{FOUT}	_	100	_	_	kΩ

APPLICATION CIRCUITS (for MSM6789A (5 V Version))

This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 8-Mbit serial registers and two 2-Mbit serial voice ROMs.

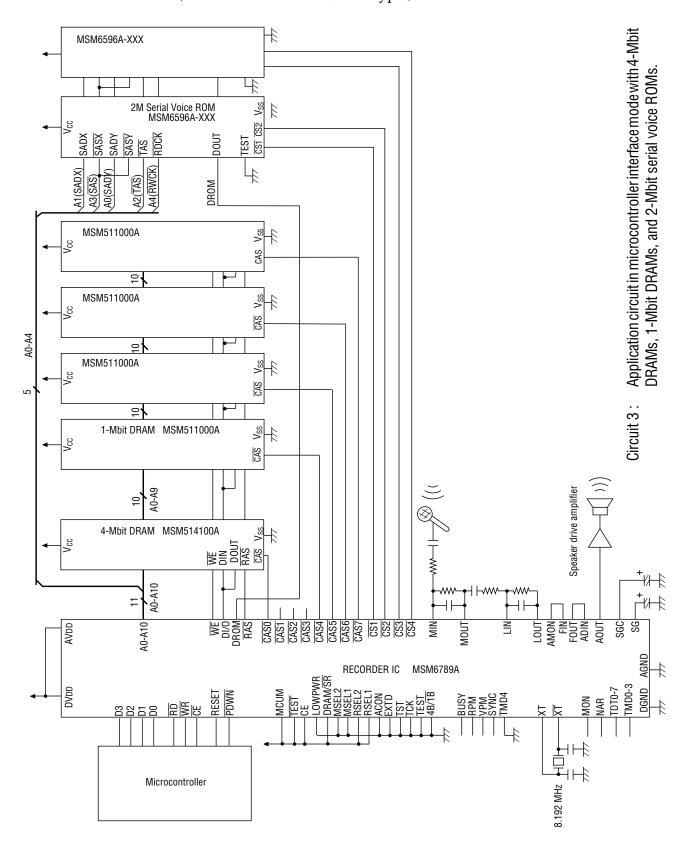


This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (1-bit \times type) and two 2-Mbit serial voice ROMs.

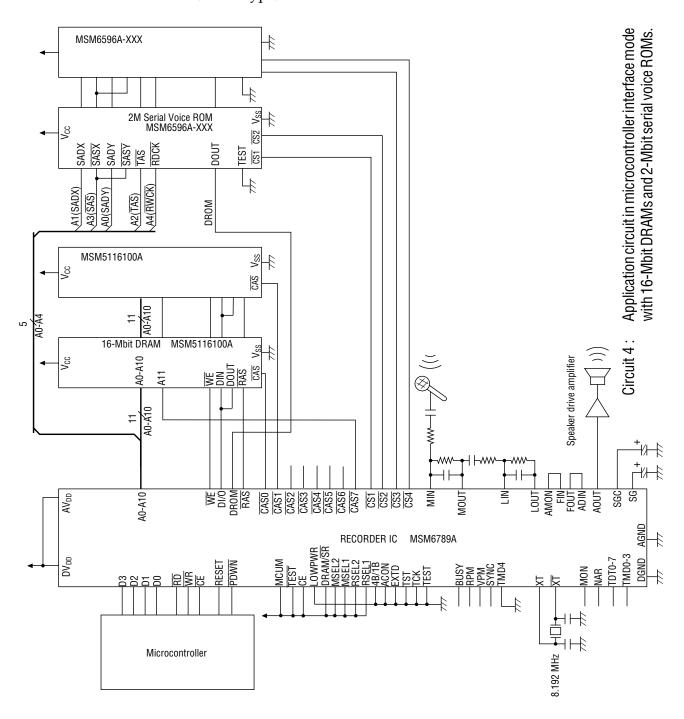


APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (1-bit \times type), and two 2-Mbit serial voice ROMs.

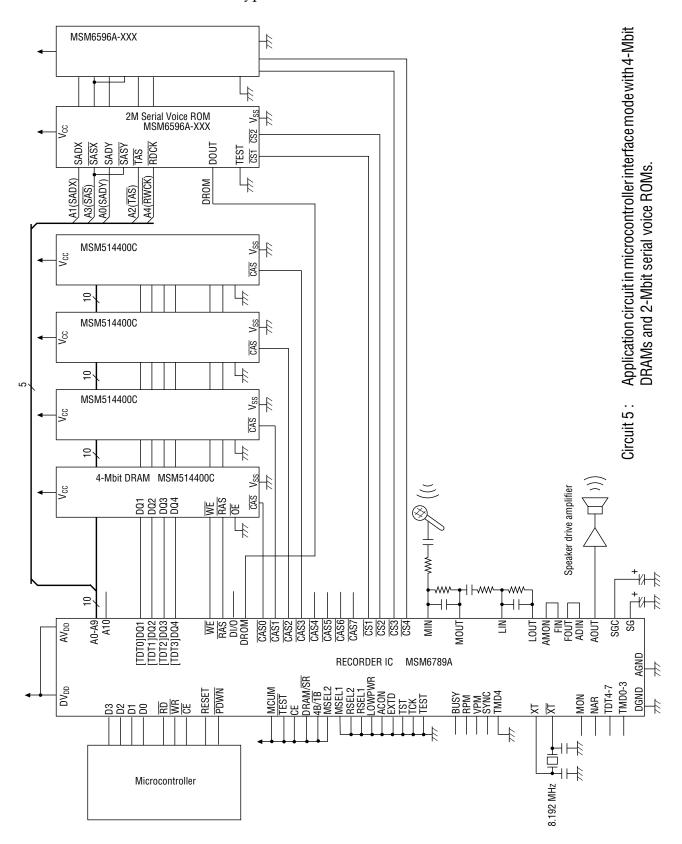


This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (1-bit × type) and two 2-Mbit serial voice ROMs.

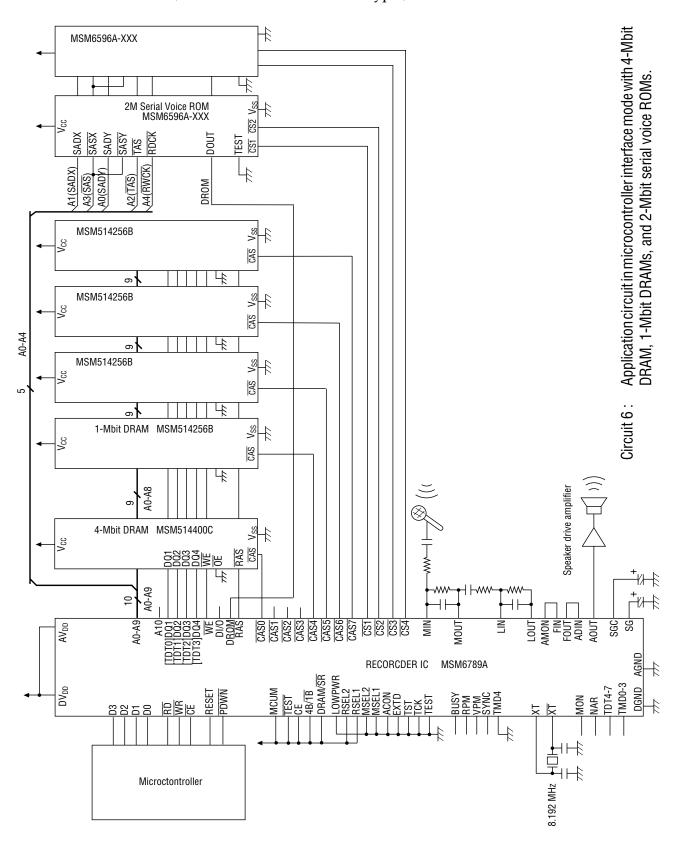


APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

This is an application circuit example when the MSM6789A is used in microcontroller interface mode with four 4-Mbit DRAMs (4-bit \times type) and two 2-Mbit serial voice ROMs.

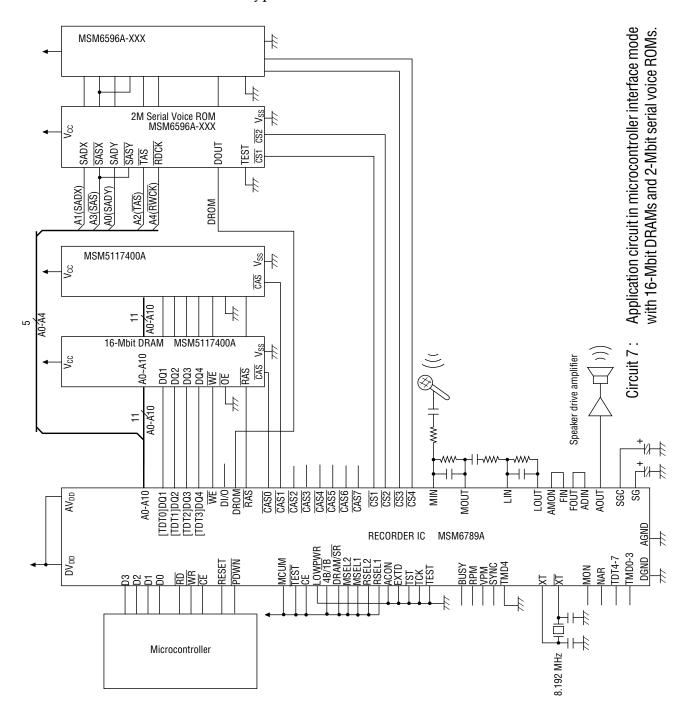


This is an application circuit example when the MSM6789A is used in microcontroller interface mode with one 4-Mbit DRAM, four 1-Mbit DRAMs (4-bit × type), and two 2-Mbit serial voice ROMs.

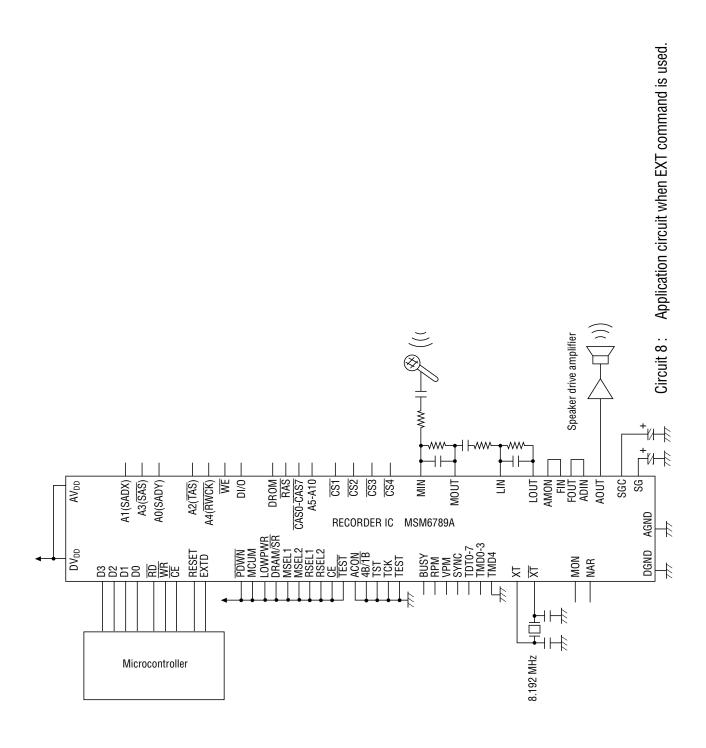


APPLICATION CIRCUITS (for MSM6789A (5 V Version)) (Continued)

This is an application circuit example when the MSM6789A is used in microcontroller interface mode with two 16-Mbit DRAMs (4-bit × type) and two 2-Mbit serial voice ROMs.



This is an application circuit example when the EXT command is used for recording/playback.



APPLICATION CIRCUITS (for MSM6789L (3.3 V Version))

This is an application circuit example when the MSM6789L is used in microcontroller interface mode with four 4-Mbit serial registers and two 2-Mbit serial voice ROMs.

