OKI Semiconductor

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MSM6794

DOT MATRIX LCD DRIVER WITH 128-CHANNEL RAM

GENERAL DESCRIPTION

The MSM6794 is a dot matrix graphic liquid crystal display LSI device to display bit maps. It drives an LCD panel for dot matrix graphic display under the control of a 4- or 8-bit microcomputer.

All necessary functions for driving a bit map type LCD are built in on one chip. Therefore,by using the MSM6794, a bit map type dot matrix graphic liquid crystal display system can be implemented with a small number of chips.

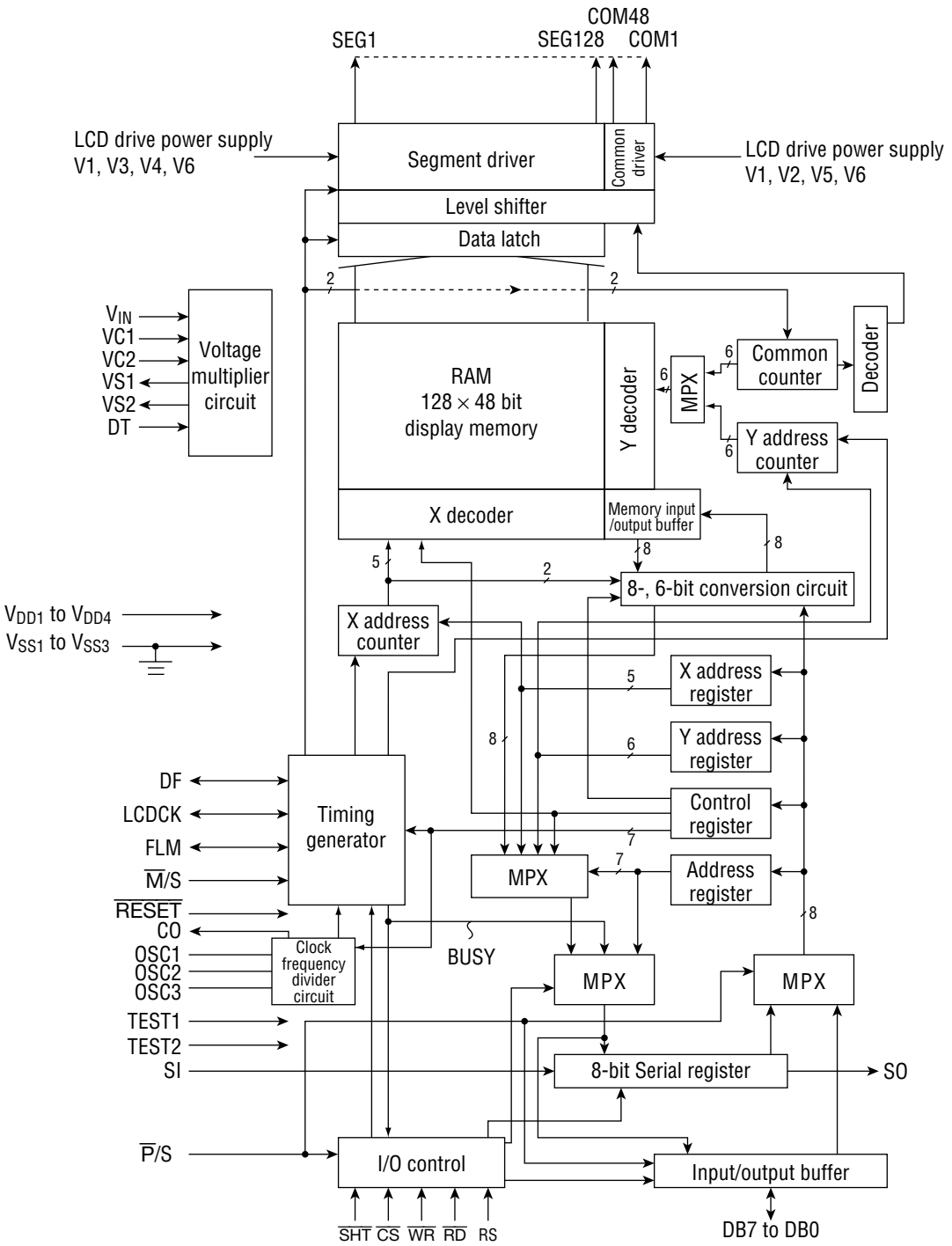
Since 1-bit data of the display RAM corresponds to the light-on/off of 1-dot of the LCD panel (bit map system), a flexible display, including kanji display, is possible. One chip comprises a graphic display system of a maximum of 128×48 dots. This display can be expanded by using multiple chips.

The MSM6794 uses CMOS process. Since it is an internal RAM type, the MSM 6794 features low power consumption, and is suited to display for battery-driven portable equipment.

FEATURES

- Segment outputs : Maximum of 128
- Common outputs : Maximum of 48
- Display duty : 1/33, 1/41, 1/44, 1/48
- Bit map type internal RAM : 6,144 bits (128×48 bits)
- Display data I/F : 8-bit parallel/serial switchable
- Standby function by program
- LCD drive bias resistor (externally connected)
- Built-in voltage multiplier circuit
- LOGIC voltage : 2.7 to 5.5V
- LCD driving voltage : V_{BI} 5 to 12V (positive voltage)
- Low current consumption : Maximum of 10µA (in standby mode)
- Number of pads : 224

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable Pins
Supply voltage	V_{DD}	Ta=25°C, V_{DD1-4}–V_{SS1-3}	–0.3 to +7	V	V_{DD1-4}, V_{SS1-3}
Bias voltage	V_{BI}	Ta=25°C,V1–V6	–0.3 to +14	V	V1, V6
Voltage multiplication reference voltage	V_{IN}	V_{IN}–V_{SS1-3} *2	–0.3 to +7	V	V_{IN}, V_{SS1-3}
		V_{IN}–V_{SS1-3} *3	–0.3 to +4.6		
Input voltage	V_I	Ta=25°C	–0.3 to V_{DD}+0.3	V	All Inputs
Power dissipation	P_D	—	*1	mW	—
Storage temperature	T_{STG}	—	–55 to +150	°C	—

Ta : ambient temperature

*1 Power dissipation depends on the heat radiation in a device attach condition. Set junction temperature to 150°C or lower.

*2 Ta = 25°C; when doubler is used.

*3 Ta = 25°C; when tripler is used.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable Pins
Supply voltage	V_{DD}	V_{DD1-4}–V_{SS1-3}	2.7 to 5.5	V	V_{DD1-4}, V_{SS1-3}
Bias voltage	V_{BI}	V1–V6 1	5 to 12	V	V1, V6
Voltage multiplicatipon reference voltage	V_{IN}	V_{IN}–V_{SS1-3}	1 to V_{DD}	V	V_{IN}, V_{SS1-3}
		See Note 1 on p.6	1 to 4		
Operating frequency	f_{op}	2	270 to 500	kHz	OSC1
Operating temperature	T_{op}	—	–25 to +85	°C	—

1 For bias potential, V1 has the highest potential and V6 has the lowest potential. Use V6 at the same potential as V_{SS1} to V_{SS3}.

2 RC oscillation and external input clock frequency (when frequency dividing ratio is 1). For divided frequency operation, clock frequency after dividing must be within this range.

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD}=2.7 to 4.5V, V_{BI}=5 to 12V, Ta=–25 to +85°C)

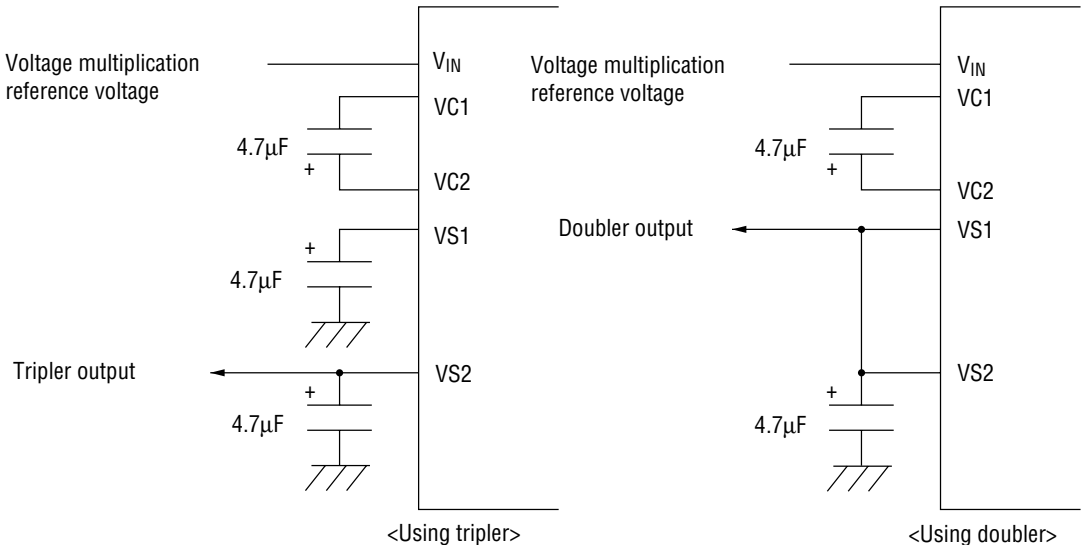
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit.	Applicable Pin
"H" input voltage 1	V_{IH1}	—	0.8V_{DD}	—	V_{DD}	V	OSC1
"H" input voltage 2	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	DB0-7, LCDCK, FLM, DF
"H" input voltage 3	V_{IH3}	—	0.8V_{DD}	—	V_{DD}	V	Other input pins
"L" input voltage 1	V_{IL1}	—	0	—	0.2V_{DD}	V	OSC1
"L" input voltage 2	V_{IL2}	—	0	—	0.2V_{DD}	V	DB0-7, LCDCK, FLM, DF
"L" input voltage 3	V_{IL3}	—	0	—	0.2V_{DD}	Unit.	Other input pins
"H" input current 1	I_{IH1}	V_I=V_{DD}	—	—	5	µA	Input pins excluding DB0-7, LCDCK, FLM and DF
"H" input current 2	I_{IH2}	V_I=V_{DD}	–5	—	5	µA	DB0-7, LCDCK, FLM, DF
"L" input current I	I_{IL1}	V_I=0V	–5	—	—	µA	Input pins excluding DB0-7, LCDCK, FLM and DF
"L" input current 2	I_{IL2}	V_I=0V	–5	—	5	µA	DB0-7, LCDCK, FLM, DF
OFF leakage current	I_{off}	V_I=V_{DD} or 0V	–5	—	5	µA	SO
"H" output voltage 1	V_{OH1}	I_O=–1.0mA	0.9V_{DD}	—	—	V	CO, LCDCK, FLM, DF, SO
"H" output voltage 2	V_{OH2}	I_O=–1.0mA	0.9V_{DD}	—	—	V	DB0 to DB7
"L" output voltage 1	V_{OL1}	I_O=1.0mA	—	—	0.1V_{DD}	V	CO, LCDCK, FLM, DF, SO
"L" output voltage 2	V_{OL2}	I_O=1.0mA	—	—	0.1V_{DD}	V	DB0 to DB7
Multiplied voltage 1 Doubler output	V_{DB}	I_O=–500µA f_{osc}=350kHz	V_{IN}×2 –0.5	—	—	V	VS2
Multiplied voltage 2 Tripler output	V_{TR}	I_O=–500µA f_{osc}=350kHz	V_{IN}×3 –1.0	—	—	V	VS2
COM output resistance	R_C	I_O=±50µA	—	—	10	kΩ	COM1 to COM48
SEG output resistance	R_S	I_O=±20µA	—	—	20	kΩ	SEG1 to SEG128
Supply Current 1	I_{DD1}	During display External clock f_{osc} = 350kHz	—	—	450	µA	V_{DD}
Supply Current 2	I_{DD2}	During display Internal oscillation f_{osc} = 350kHz	—	360	700	µA	V_{DD}
Supply Current 3	I_{DDS}	During standby	—	—	10	µA	V_{DD}
Oscillation frequency	f_{OSC}	R_f=18kΩ C_f=56pF See Note 3 on p.6	292	350	437	kHz	OSC1, OSC2, OSC3

DC Characteristics (2)

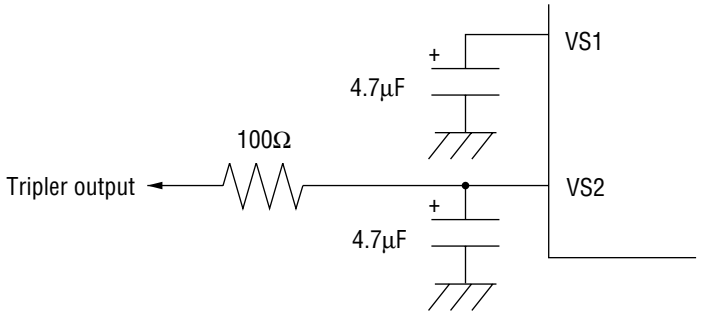
(V_{DD}=4.5 to 5.5V, V_{BI}=5 to 12V, Ta=–25 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
"H" input voltage 1	V_{IH1}	—	0.8V_{DD}	—	V_{DD}	V	OSC1
"H" input voltage 2	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	DB0-7, LCDCK, FLM, DF
"H" input voltage 3	V_{IH3}	—	0.8V_{DD}	—	V_{DD}	V	Other input pins
"L" input voltage 1	V_{IL1}	—	0	—	0.2V_{DD}	V	OSC1
"L" input voltage 2	V_{IL2}	—	0	—	0.2V_{DD}	V	DB0-7, LCDCK, FLM, DF
"L" input voltage 3	V_{IL3}	—	0	—	0.2V_{DD}	V	Other input pins
"H" input current 1	I_{IH1}	V_I=V_{DD}	—	—	5	µA	Input pins excluding DB0-7, LCDCK, FLM and DF
"H" input current 2	I_{IH2}	V_I=V_{DD}	–5	—	5	µA	DB0-7, LCDCK, FLM, DF
"L" input current I	I_{IL1}	V_I=0V	–5	—	—	µA	Input pins excluding DB0-7, LCDCK, FLM and DF
"L" input current 2	I_{IL2}	V_I=0V	–5	—	5	µA	DB0-7, LCDCK, FLM, DF
OFF leakage current	I_{off}	V_I=V_{DD}/0V	–5	—	5	µA	SO
"H" output voltage 1	V_{OH1}	I_O=–1.5mA	0.9V_{DD}	—	—	V	CO, LCDCK, FLM, DF, SO
"H" output voltage 2	V_{OH2}	I_O=–1.5mA	0.9V_{DD}	—	—	V	DB0 to DB7
"L" output voltage 1	V_{OL1}	I_O=1.5mA	—	—	0.1V_{DD}	V	CO, LCDCK, FLM, DF, SO
"L" output voltage 2	V_{OL2}	I_O=1.5mA	—	—	0.1V_{DD}	V	DB0 to DB7
Multiplied voltage 1 Doubler output	V_{DB}	I_O=–500µA f_{osc}=350kHz	V_{IN}×2 –0.5	—	—	V	VS2
Multiplied voltage 2 Tripler output	V_{TR}	I_O=–500µA f_{osc}=350kHz	V_{IN}×3 –1.0	—	—	V	VS2
COM output resistance	R_C	I_O=±50µA	—	—	10	kΩ	COM1 to COM48
SEG output resistance	R_S	I_O=±20µA	—	—	20	kΩ	SEG1 to SEG128
Supply Current 1	I_{DD1}	During display External clock f_{osc} = 350kHz	—	—	450	µA	V_{DD}
Supply Current 2	I_{DD2}	During display Internal oscillation f_{osc}=350kHz	—	360	700	µA	V_{DD}
Supply Current 3	I_{DDS}	During standby	—	—	10	µA	V_{DD}
Oscillation frequency	f_{OSC}	R_f=22kΩ C_f=56pF See Note 3 on p.6	292	350	437	kHz	OSC1, OSC2, OSC3

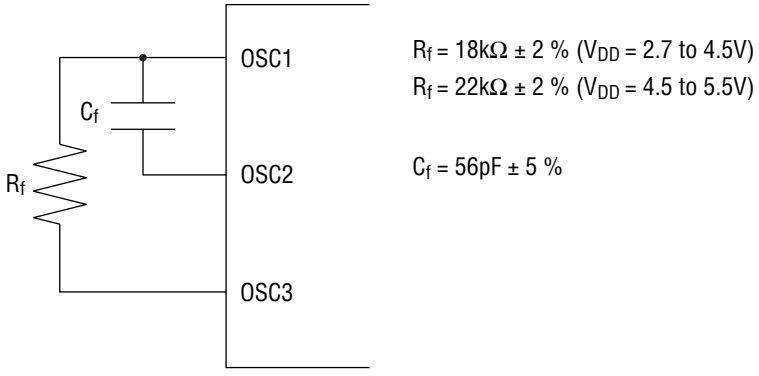
Notes: 1. Voltage multiplication reference voltage is = V_{DD} maximum when the multiplied voltage is 12V or less.
The voltage multiplication reference voltage is 4V maximum when the multiplied voltage is 12V or more (tripler output).
Condition: f_{osc} = 350kHz
Voltage multiplier circuit configuration: connect as in the following diagram.



2. If the multiplied voltage output and bias power supply are directly connected, the voltage multiplier circuit operation may malfunction due to bias power supply noise. A countermeasure for noise is necessary, such as inserting a series resistor to prevent noise from entering multiplied voltage output (VS1, VS2).



3. RC oscillation circuit configuration: connect as in the following diagram.



AC Characteristics

Parallel interface (1)

(V_{DD}=2.7 to 4.5V, V_{BI}=5 to 12V, Ta=–25 to +85°C)

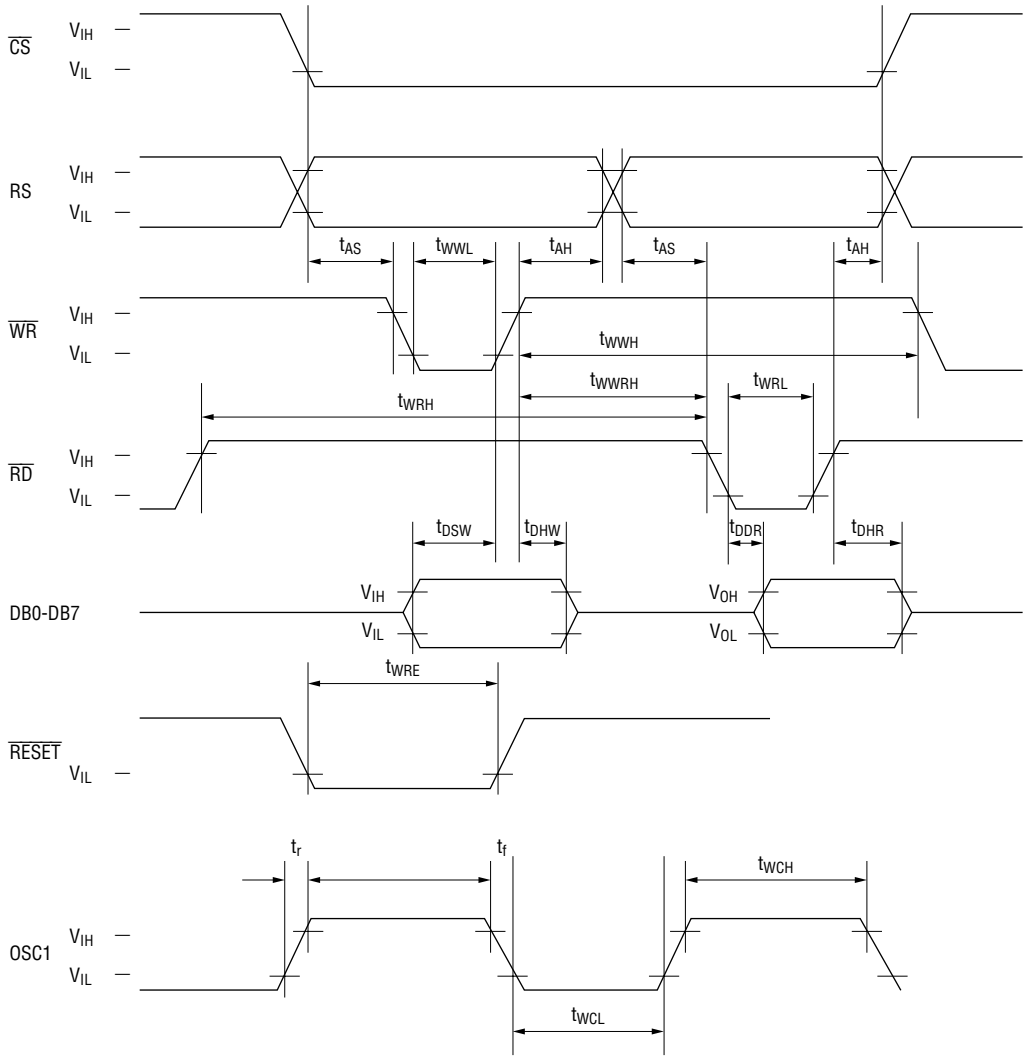
Parameter	Symbol	Condition	Min	Max	Unit
$\overline{RD}$ "H" level width	t_{WRH}	—	200	—	ns
$\overline{RD}$ "L" level width	t_{WRL}	—	200	—	ns
$\overline{WR}$ "H" level width	t_{WWH}	—	200	—	ns
$\overline{WR}$ "L" level width	t_{WWL}	—	200	—	ns
$\overline{WR}$-$\overline{RD}$ "H" level width	t_{WWRH}	—	200	—	ns
$\overline{CS}$, RS setup time	t_{AS}	—	50	—	ns
$\overline{CS}$, RS hold time	t_{AH}	—	10	—	ns
Write data setup time	t_{DSW}	—	50	—	ns
Write data hold time	t_{DHW}	—	20	—	ns
Read data output delay time	t_{DDR}	C_L=50pF	—	170	ns
Read data hold time	t_{DHR}	—	20	—	ns
External clock "H" level width	t_{WCH}	—	200	—	ns
External clock "L" level width	t_{WCL}	—	200	—	ns
$\overline{RESET}$ pulse width	t_{WRE}	—	2.0	—	µs
External clock rise time, fall time	t_r, t_f	—	—	100	ns

Parallel interface (2)

(V_{DD}=4.5 to 5.5V, V_{BI}=5 to 12V, Ta=–25 to +85°C)

Parameter	Symbol	Condition	Min	Max	Unit
$\overline{RD}$ "H" level width	t_{WRH}	—	150	—	ns
$\overline{RD}$ "L" level width	t_{WRL}	—	150	—	ns
$\overline{WR}$ "H" level width	t_{WWH}	—	150	—	ns
$\overline{WR}$ "L" level width	t_{WWL}	—	150	—	ns
$\overline{WR}$-$\overline{RD}$ "H" level width	t_{WWRH}	—	150	—	ns
$\overline{CS}$, RS setup time	t_{AS}	—	50	—	ns
$\overline{CS}$, RS hold time	t_{AH}	—	10	—	ns
Write data setup time	t_{DSW}	—	50	—	ns
Write data hold time	t_{DHW}	—	20	—	ns
Read data output delay time	t_{DDR}	C_L=50pF	—	130	ns
Read data hold time	t_{DHR}	—	20	—	ns
External clock "H" level width	t_{WCH}	—	150	—	ns
External clock "L" level width	t_{WCL}	—	150	—	ns
$\overline{RESET}$ pulse width	t_{WRE}	—	2.0	—	µs
External clock rise time, fall time	t_r, t_f	—	—	20	ns

Parallel Interface Timing Diagram



$V_{IH} = 0.8V_{DD}$, $V_{IL} = 0.2V_{DD}$

$V_{OH} = 0.9V_{DD}$, $V_{OL} = 0.1V_{DD}$

Serial interface (1)

(V_{DD}=2.7 to 4.5V, V_{BI}=5 to 12V, Ta=–25 to +85°C)

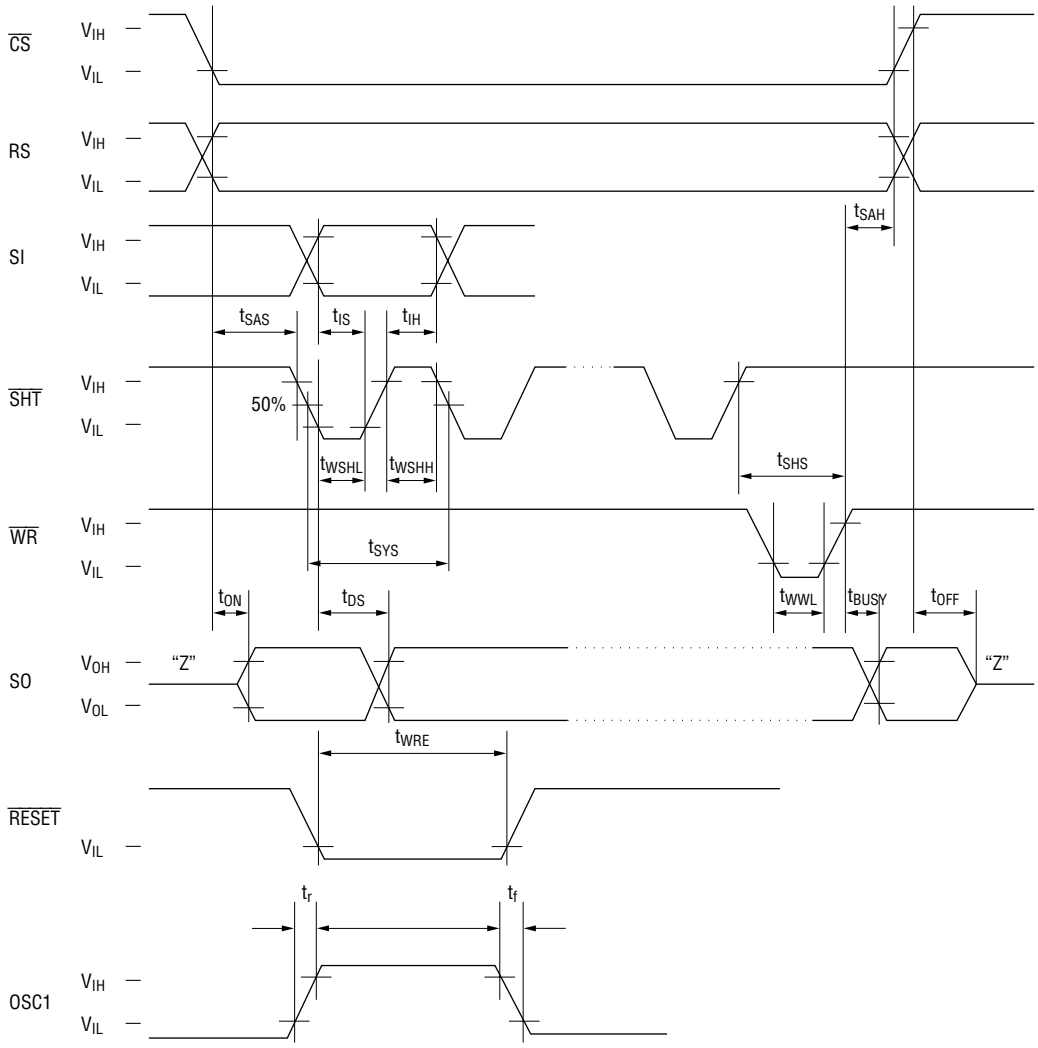
Parameter	Symbol	Condition	Min	Max	Unit
$\overline{CS}$, RS setup time	t_{SAS}	—	60	—	ns
$\overline{CS}$, RS hold time	t_{SAH}	—	15	—	ns
S1 setup time	t_{IS}	—	100	—	ns
S1 hold time	t_{IH}	—	15	—	ns
$\overline{SHT}$ "H" pulse width	t_{WSHH}	—	100	—	ns
$\overline{SHT}$ "L" pulse width	t_{WSHL}	—	100	—	ns
$\overline{SHT}$ clock cycle time	t_{SYS}	—	400	—	ns
SO ON delay time	t_{ON}	C_L=50pF	—	200	ns
SO output delay time	t_{DS}	C_L=50pF	0	200	ns
SO OFF delay time	t_{OFF}	—	—	50	ns
BUSY delay time	t_{BUSY}	C_L=50pF	—	200	ns
$\overline{WR}$ setup time	t_{SHS}	—	100	—	ns
$\overline{WR}$ "L" pulse width	t_{WWL}	—	120	—	ns
$\overline{RESET}$ pulse width	t_{WRE}	—	2.0	—	µs
External clock rise time, fall time	t_r, t_f	—	—	100	ns

Serial interface (2)

(V_{DD}=4.5 to 5.5V, V_{BI}=5 to 12V, Ta=–25 to +85°C)

Parameter	Symbol	Condition	Min	Max	Unit
$\overline{CS}$, RS setup time	t_{SAS}	—	50	—	ns
$\overline{CS}$, RS hold time	t_{SAH}	—	10	—	ns
S1 setup time	t_{IS}	—	50	—	ns
S1 hold time	t_{IH}	—	10	—	ns
$\overline{SHT}$ "H" pulse width	t_{WSHH}	—	80	—	ns
$\overline{SHT}$ "L" pulse width	t_{WSHL}	—	80	—	ns
$\overline{SHT}$ clock cycle time	t_{SYS}	—	200	—	ns
SO ON delay time	t_{ON}	C_L=50pF	—	100	ns
SO output delay time	t_{DS}	C_L=50pF	0	100	ns
SO OFF delay time	t_{OFF}	—	—	20	ns
BUSY delay time	t_{BUSY}	C_L=50pF	—	100	ns
$\overline{WR}$ setup time	t_{SHS}	—	50	—	ns
$\overline{WR}$ "L" pulse width	t_{WWL}	—	80	—	ns
$\overline{RESET}$ pulse width	t_{WRE}	—	2.0	—	µs
External clock rise time, fall time	t_r, t_f	—	—	20	ns

Serial Interface Timing Diagram

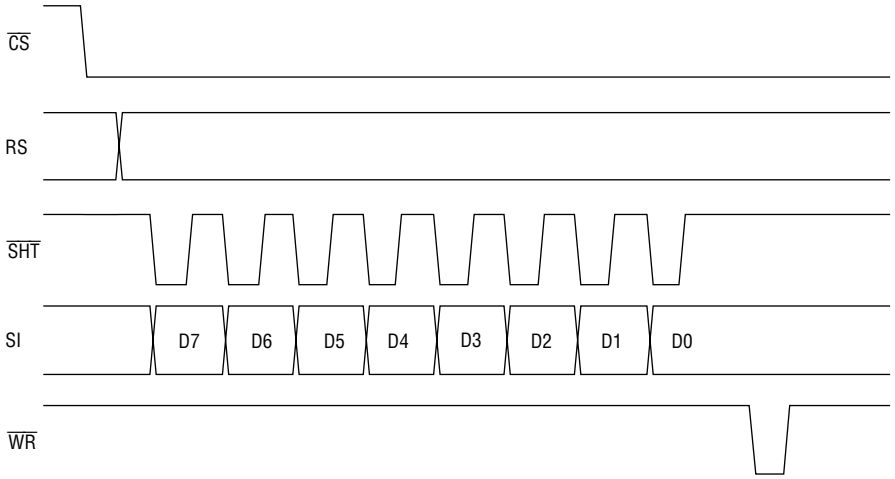


$V_{IH} = 0.8V_{DD}$, $V_{IL} = 0.2V_{DD}$

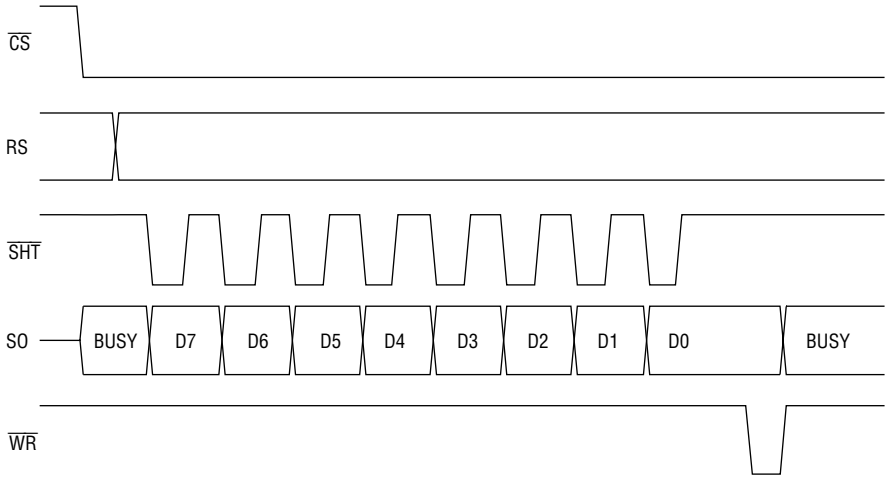
$V_{OH} = 0.9V_{DD}$, $V_{OL} = 0.1V_{DD}$

Serial Interface Input/Output Timing

Input timing



Output timing



For SO output, 8 bits after input of the $\overline{WR}$ pulse are valid.

FUNCTIONAL DESCRIPTION

Pin Functional Description

- $\overline{CS}$ (Chip Select)
  Chip select input pin. "L" is for Select, "H" is for Unselect. Internal registers can be accessed only when this pin is at "L".
  When this pin is "H", the SO pin becomes high impedance.

- $\overline{WR}$ (Write Enable)
  This is a write signal input pin when a parallel interface is used. Data is written to a register at the rising edge of a signal pulse.
  This becomes a latch signal input pin when a serial interface is used.
  This pin is normally "H".

- $\overline{RD}$ (Read Enable)
  This is a read signal input pin when a parallel interface is used. Data can be read while the pulse is "L". This pin is normally "H".
  Set this pin to "H" or "L" when a serial interface is used.

- RS (Register Select)
  Input pin to select register. Setting this pin to "L" selects the address register. Setting to "H" selects a register set by the address register.
  If this pin is changed from "H" to "L" while a serial interface is used, the SERW bit (D4 bit) of the address register is automatically reset to "0".

- DB0 to DB7 (Data Buses 0 to 7)
  Data input/output pins for parallel interface. These pins are normally in high impedance status. When $\overline{RD}$ = "L", each register data is output.
  Leave this pin open when a serial interface is used.

- SI (Serial Data Input)
  Data input pin for serial interface. Each register data and display data are read at the rising edge of $\overline{SHT}$, and written to the register at the falling edge of $\overline{WR}$. 8-bit data just before the rise of $\overline{WR}$ is valid data.
  Set this pin to "H" or "L" when a parallel interface is used.

- SO (Serial Data Output)
  Data output pin for serial interface. Each register data is output synchronizing with the rise of $\overline{SHT}$. For busy/non-busy data, busy ("H") is output after the rise of $\overline{WR}$, and automatically becomes non-busy ("L") after a specified time.
  This pin is always in high impedance status when a parallel interface is used.

- $\overline{SHT}$ (Shift Clock)
  Clock input pin for serial interface data input/output. Data is input synchronizing with the rise of the clock, and data is output synchronizing with the fall of the clock.
  This pin is normally in "H".
  Set this pin to "H" or "L" when a parallel interface is used.

- $\overline{P}$/S (Parallel/Serial Select)
  Input pin for selecting parallel interface or serial interface. Setting this pin to "L" selects parallel interface. Setting to "H" selects serial interface. Do not change the setting value after power is turned on.

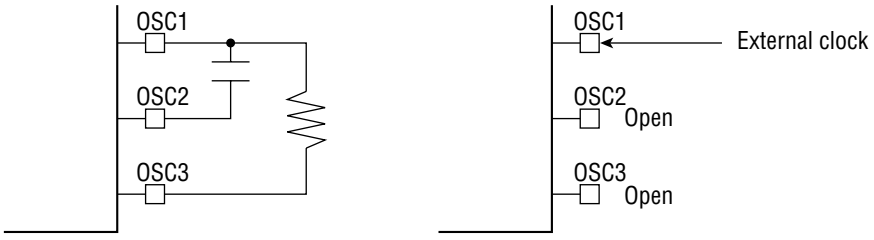
•LCDCK (LCD Clock)
Input/output pin for display data latch clock. This pin is an output pin if master is specified and is an input pin if slave is specified. To use two or more MSM6794 devices, connect LCDCK of the master with LCDCK of the slave.

•FLM (First Line Marker)
Input/output pin for the first line marker. This pin is an output pin if master is specified, and is an input pin if slave is specified. To use two or more MSM6794 devices, connect FLM of the master with FLM of the slave.

•DF (Display Frequency)
Input/output pin for LCD alternating frame signals. This pin is an output pin if master is specified, and an input pin if slave is specified. To use two or more MSM6794 devices, connect DF of the master with DF of the slave.

•OSC1 (Oscillation 1)
Input pin for RC oscillation. Connecting the specified capacitor and resistor to this pin and the OSC2 and OSC3 pins creates an RC oscillation circuit. To generate an original oscillation clock externally, input the original oscillation clock to this pin.

•OSC2, OSC3 (Oscillation 2, Oscillation 3)
Output pins for RC oscillation. Connecting the specified capacitor and resistor to these pins and the OSC1 pin creates an RC oscillation circuit. To generate an original oscillation clock externally, leave these pins open.



Oscillation circuit diagram

$\overline{M}$/S (Master/Slave)
Input pin for switching between master and slave. Setting this pin to "L" sets this IC to the IC at the master side. Setting this pin to "H" sets this IC to the IC at the slave side. Do not change the setting value after power is turned on.

CO (Clock Output)
Output pin for original oscillation clock. The clock in the same phase as OSC1 is output. To use two or more MSM6794 devices, connect CO of the master with OSC1 of the slave.

$\overline{\text{RESET}}$ (Reset)
Pin for reset signal input. Setting this pin to "L" sets initial status. For the status of each register and display after reset input, see "Status of Pins and Registers after Reset Input".

TEST1, TEST2 (Test Signal 1, Test Signal 2)
Test signal input pins. These pins are used by Oki to test. Set these pins to "L" permanently.

SEG1 to SEG128 (Segment 1 to Segment 128)
Segment signal output pins for driving LCD. Leave unused segment pins open.

COM1 to COM48 (Common 1 to Common 48)
Common signal output pins for driving LCD. Use COM1 to COM33 and leave COM34 to COM48 open for 1/33 duty. Use COM1 to COM41 and leave COM42 to COM48 open for 1/41 duty. Use COM1 to COM44 and leave COM45 to COM48 open for 1/44 duty.

V_{DD1} to V_{DD4}
Pins to connect the logic power supply. Connect these pins to positive pins of the power supply.

V_{SS1} to V_{SS3}
Pins to connect GND power supply.

V1,V3, V4, V6
LCD power supply pins for the segment driver. Connect V6 to GND.

V1, V2, V5, V6
LCD power supply pins for the common driver. Connect V6 to GND.

DT (Doubler/Tripler Select)
Input pin to select voltage multiplier circuit. Setting this pin to "L" selects tripler, and setting this pin to "H" selects doubler. Do not change the selection after power is turned on.

VS1
Doubler voltage output pin. Voltage twice as high as voltage that is input from V_{IN} is output from this pin. Connect a 4.7µF capacitor between this pin and the V_{SS1} to V_{SS3} pins to stabilize power supply. When doubler is used, connect this pin with VS2.
Set this pin to GND level if the voltage multiplier circuit is not used.

VS2
Multiplied voltage output pin. Multiplied voltage set by the DT pin is output from this pin. If tripler is used, connect a 4.7µF capacitor between this pin and the V_{SS1} to V_{SS3} pins to stabilize power supply. If doubler is used, connect this pin with VS1.
Set this pin to GND level if the voltage multiplier circuit is not used.

VC1, VC2
Capacitor connection pins for voltage multiplication. Connect a 4.7µF capacitor between the VC1 and VC2 pins. When an electrolytic capacitor is used, connect the VC2 pin to the positive side.
Set these pins to GND level if the voltage multiplier circuit is not used.

V_{IN}
Voltage multiplication reference voltage input pin. Voltage two or three times higher than voltage that is input to this pin is output from the VS2 pin.
Set this pin to GND level if the voltage multiplier circuit is not used.

Registers

CS	RS	Register number		Register	Register	Data bit							
		1	0	symbol	name	7	6	5	4	3	2	1	0
1	—	—	—	—	Invalid	—	—	—	—	—	—	—	—
0	0	—	—	AR	Address register	BUSY	STBY	DISP	SERW	HZ	—	Register number	
0	1	0	0	DRAM	Display data register	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	YAD	X address register	—	—	—	XAD				
0	1	1	0	XAD	Y address register	—	—	YAD					
0	1	1	1	FCR	Control register	INC	WLS	—	FFS			DUTY	

Register Description

Address register (AR)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	STBY	DISP	SERW	HZ	—	Register number	

(1) D7 BUSY (Busy flag)

1: busy
0: ready

This bit indicates that this IC is in internal processing. Reading/Writing display memory sets this bit to "1". This bit becomes busy for a period of a maximum of 8 clocks by reading/writing display memory. Registers other than this register cannot be read or written while this bit is "1".

Setting the $\overline{\text{RESET}}$ pin to "L" also sets this bit to "1". This bit becomes "1" while the $\overline{\text{RESET}}$ pin is "L", and becomes "0" when the $\overline{\text{RESET}}$ pin becomes "H". In the case of a serial interface, the SO pin becomes high impedance if the $\overline{\text{RESET}}$ pin becomes "L". Therefore this bit cannot be read during a reset period.

This bit is read only. Writing to this bit is invalid.

(2) D6 STBY (Standby)

1: standby
0: normal

This bit sets this IC to standby mode. This IC enters standby mode by writing "1" to this bit, and returns from standby mode to normal mode by writing "0" to this bit.

This bit is set to normal status by setting the $\overline{\text{RESET}}$ pin to "L".

Setting this bit to standby mode in a busy state may cause a malfunction.

For details of standby mode, see "Pin status during Standby Operation and Register Status after Cancellation".

(3) D5 DISP (Display on/off)

1: display on
0: display off

This bit sets ON/OFF of the liquid crystal display connected to this IC. Writing "1" to this bit turns the liquid crystal display ON, and writing "0" turns it OFF. This bit is used to prevent a random display until the initialization of the display memory after power-on.

This bit is set to display off status by setting the $\overline{\text{RESET}}$ pin to "L".

(4) D4 SERW (Serial Data Read/Write)

1: writing registers other than address register is invalid
0: writing all registers is valid

This bit limits writing to registers when a serial interface is used. Writing "1" to this bit disables writing to registers other than the address register, and writing "0" enables writing to all registers.

This bit is a command to make registers read-only when a serial interface is used. When serial data is read from the SO pin, this pin disables writing to registers other than the address register, even if data is input to the SI pin.

This bit is valid only when a serial interface is used. When a parallel interface is used, writing to this bit is invalid, and "0" is always read from this bit.

This bit is set to write enable of all registers by setting the $\overline{\text{RESET}}$ pin to "L". This bit is automatically reset to "0" each time the RS pin is set from "H" to "L".

(5) D3 HZ (high impedance) (SO pin output control)

1: high impedance

0: output enable

This bit sets the status of the SO pin when a serial interface is used. Writing "1" to this bit sets the SO pin to a high impedance state, and writing "0" to this bit sets the SO pin to an output enable state.

This bit is valid only when a serial interface is used. When a parallel interface is used, writing to this bit is invalid, and "0" is always read from this bit.

This bit is set to a high impedance state by setting the $\overline{\text{RESET}}$ pin to "L".

(6) D2 (Invalid Bit)

Writing to this bit is invalid, and "0" is always read from this bit.

(7) D1, D0 (Register Number)

These bits select a register other than the address register. The relationship between each bit and each register is shown in the table below.

Code	D1	D0	Register Name
0	0	0	Display data register
1	0	1	X address register
2	1	0	Y address register
3	1	1	Control register

These bits are reset to (D1, D0) = (0, 0) (display data register select status) by setting the $\overline{\text{RESET}}$ pin to "L".

Display data register (DRAM)

D7	D6	D5	D4	D3	D2	D1	D0
8-bit DATA							
—		6-bit DATA					

This register is used to write or read display data to and from the liquid crystal display RAM. The contents of this register are written or read to and from the address set by the X address register and Y address register.
The bit length of display data is selected by the WLS bit (D6 bit) of the control register. If 6-bit data is selected, writing to the D7 and D6 bit is invalid, and "0" is always read from these bits. D7 (D5 for 6-bit DATA) is MSB, and D0 is LSB.
The content of this register does not change, even if the $\overline{\text{RESET}}$ pin is set to "L".

X address register (XAR)

D7	D6	D5	D4	D3	D2	D1	D0
—			XAD				

This register is used to set the X address of the liquid crystal display RAM.
If 8-bit data is selected by the WLS bit (D6 bit) of the control register, the addresses are 0 to15 (00H to 0FH). If 6-bit data is selected, the addresses are 0 to 21 (00H to 15H). If other addresses are set, operation is unpredictable.
Writing to the D7 to D5 bits is invalid, and "0" is always read from these bits.
This register is reset to "0" by setting the $\overline{\text{RESET}}$ pin to "L".

Y address register (YAR)

D7	D6	D5	D4	D3	D2	D1	D0
—		YAD					

This register is used to set the Y address of the liquid crystal display RAM.
If 1/48 duty is selected by DUTY bits (D1, D0 bits) of the control register, the address set value is 0 to 47 (00H to 2FH). If 1/44 duty is selected, the address set value is 0 to 43 (00H to 2BH). If 1/41 duty is selected, the address set value is 0 to 40 (00H to 28H), and if 1/33 duty is selected, the address set value is 0 to 32 (00H to 20H). If other values are set, operation is unpredictable.
Writing to D7 and D6 bits is invalid, and "0" is always read from these bits.
This register is reset to "0" by setting the $\overline{\text{RESET}}$ pin to "L".

Control register (FCR)

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	—	FFS			DUTY	

(1) D7 INC (Address Increment Direction)

1: X direction

0: Y direction

This bit sets the address increment direction of the display RAM. The address of the display RAM is automatically incremented by 1 by writing data to the display data register. Writing "1" to this bit sets the X address increment, and writing "0" to this bit sets the Y address increment.

For details of address increment, see "X, Y Address Counter Auto Increment".

The value of this register does not change, even if the $\overline{\text{RESET}}$ pin is set to "L".

(2) D6 WLS (Word Length Select)

1: 6 bits

0: 8 bits

This bit selects the read/write word length to the display RAM. Writing "1" to this bit sets read/write data to the display RAM in 6 bit units, and writing "0" to this bit sets read/write data to the display RAM in 8 bit units. Select the word length according to the character font to be used.

The value of this register does not change, even if the $\overline{\text{RESET}}$ pin is set to "L".

(3) D5 (Invalid Bit)

Writing to this bit is invalid. "0" is always read from this bit.

(4) D4 to D2 FFS (Frame Frequency Select)

This bit selects the internal clock frequency dividing ratio to the original oscillation frequency. Correspondence between each bit and each frequency dividing ratio is shown in the table below.

Code	D4	D3	D2	Frequency Dividing Ratio
0	0	0	0	1
1	0	0	1	1/2
2	0	1	0	1/3
3	0	1	1	1/4
4	1	0	0	1/6
5	1	0	1	1/8
6	1	1	0	TEST
7	1	1	1	TEST

When the original oscillation frequency is 350kHz and the frequency dividing ratio is 1, the frame frequency is about 80Hz. When the display data register is written/read, the busy time is a maximum of 8 original oscillation clocks. If the original oscillation frequency is increased to shorten the busy time, the frame frequency increases in proportion to the original oscillation frequency. In this case the frequency dividing ratio must be changed so that the frame frequency falls in the range of 60 to 100Hz. For details on the relation between original oscillation frequency and frame frequency, see "Original Oscillation Frequency and Frame Frequency".
(D4, D3, D2) = (1, 1, 0) and (1, 1, 1) are combinations which Oki uses for testing.
If these combinations are used by the user, the operation of this IC is unpredictable.
The value of this register does not change even if the $\overline{\text{RESET}}$ pin is set to "L".
Once frame frequency is set after power is turned on, the value cannot be changed. To change the frame frequency, set it again according to the power-on flowchart. See "Power-on Flowchart".

(5) D1, D0 DUTY (Display Duty Select)
These bits select the display duty. Correspondence between each bit and display duty is shown in the table below.

Code	D1	D0	DUTY
0	0	0	1/48
1	0	1	1/44
2	1	0	1/41
3	1	1	1/33

The value of this register does not change, even if the $\overline{\text{RESET}}$ pin is set to "L".
Once display duty is set after power is turned on, the value cannot be changed. To change display duty, set it again according to the power-on flowchart. See "Power-on Flowchart".

Status of Pins and Registers After Reset Input

The following tables show pin and register status after reset input.

Pin	Status
OSC2, 3	Clock output or oscillation status
CO	Clock output
SO	High impedance
DF	"H" (master), high impedance (slave)
FLM	"L" (master), high impedance (slave)
LCDCK	"L" (master), high impedance (slave)

Register	Status
Address register	HZ = "1", other bits are reset to "0".
Display data register	Display data is held
X address register	Reset to "0"
Y address register	Reset to "0".
Control register	No change from status before inputting reset

Pin Status during Standby Operation and Register Status after Cancellation

The following tables show pin status during standby operation and register status after cancellation.

Pin	Status
OSC2	"L"
OSC3	"H"
CO	"L"
SO	High impedance
DF	"H" (master), high impedance (slave)
FLM	"L" (master), high impedance (slave)
LCDCK	"L" (master), high impedance (slave)

Register	Status
Address register	STBY = "0", other bits maintain data before standby
Display data register	Maintains data before standby
X address register	Reset to "0"
Y address register	Reset to "0"
Control register	Maintains data before standby

X , Y Address Counter Auto Increment

RAM for the liquid crystal display of the MSM6794 has an X address counter and Y address counter, and both have an auto increment function.
Writing/reading display data increments either X or Y address counter. The INC bit (D7 bit) of the control register selects X or Y address to be incremented.

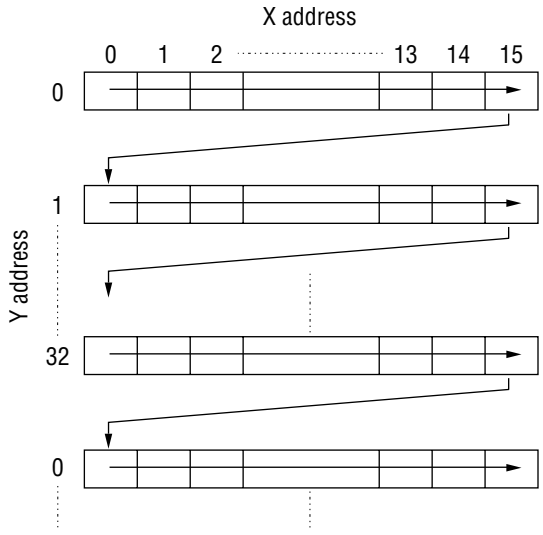
(When X address is selected:)

Address count cycle of X address counter changes depending on word length: 8- or 6-bit.
If the word length is 8-bit, X address is counted in a 0 to 15 range.
If the word length is 6-bit, X address is counted in a 0 to 21 range.
When the maximum value of an X address count value (15 for an 8-bit word length, and 21 for a 6-bit word length) returns to "0", the Y address count value is also automatically incremented.

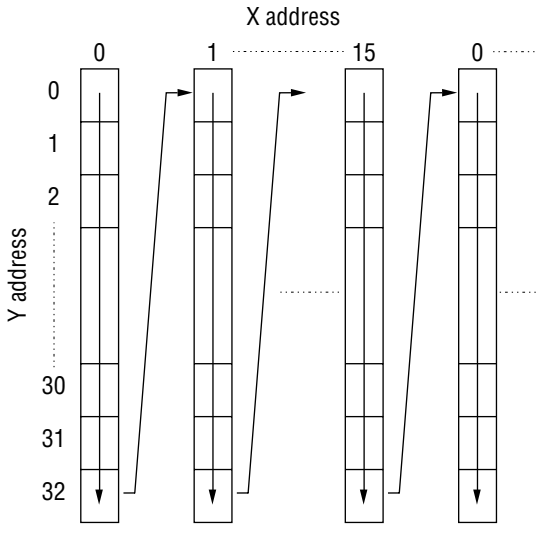
(When Y address is selected:)

The address count of Y address counter changes depending on the display duty: 1/33, 1/41, 1/44 or 1/48.
If the display duty is 1/33, Y address is counted in a 0 to 32 range.
If the display duty is 1/41, Y address is counted in a 0 to 40 range.
If the display duty is 1/44, Y address is counted in a 0 to 43 range.
If the display duty is 1/48, Y address is counted in a 0 to 47 range.
When the maximum value of a Y address count value (32 for display duty 1/33, 40 for display duty 1/41, 43 for display duty 1/44, and 47 for display duty 1/48) returns to "0", the X address count value is also automatically incremented.
(Note) If an address other than the count cycle is set at X or Y address counter, count operation becomes abnormal.

1. Example of X address increment (8-bit word length, 1/33 duty)



2. Example of Y address increment (8-bit word length, 1/33 duty)



Display Screen and Memory Address

The MSM6794 includes a bit map type display RAM (48 × 128 bit). Display data is written to display memory with MSB as (Xn, Yn) address, and LSB as (Xn+7, Yn) address, as shown in Figure 1.
Writing "1" to display memory turns the light on, and writing "0" turns the light off.
The address assignment of memory address changes depending on the selection of word length: 8 bits or 6 bits. The memory address is 0 to 15 for 8 bits per word, and 0 to 21 for 6 bits per word. When X address is 21 with 6 bits per word, the display memory is 2 bits. 2 bits (D5, D4) from MSB of data display are written to memory, with the remaining 4 bits (D3 to D0) becoming invalid.

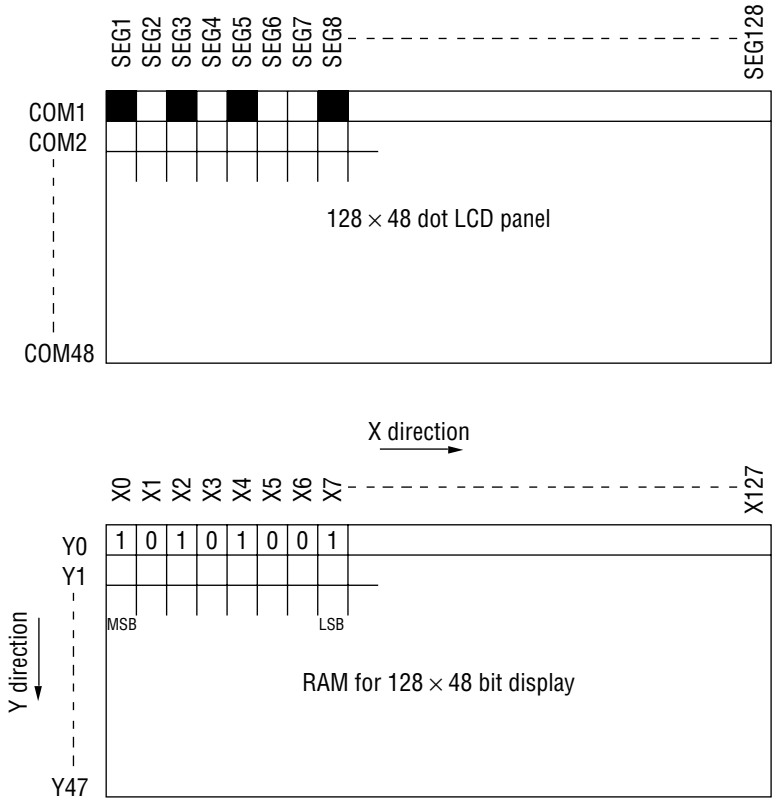


Figure 1. Correspondence between display screen and memory

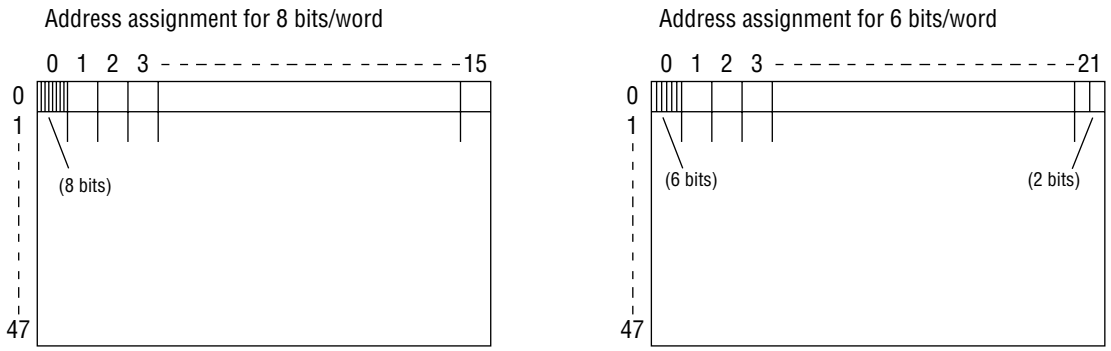
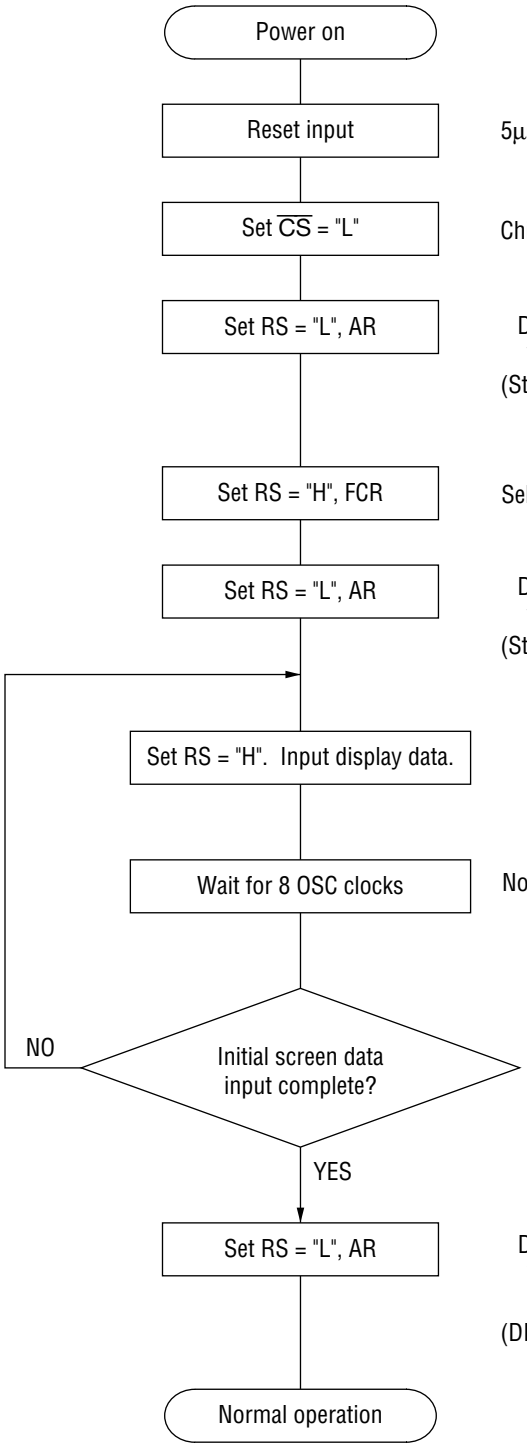


Figure 2. Display memory address

Power-on Flowchart (Serial Interface)



5µs, external or power-on reset

Chip enable

D7	D6	D5	D4	D3	D2	D1	D0
*	1	0	0	0	*	1	1

(Standby setting, FCR select, SO output enable)

Select duty according to specification. Set FFS, WLS, INC.

D7	D6	D5	D4	D3	D2	D1	D0
*	0	0	0	0	*	0	0

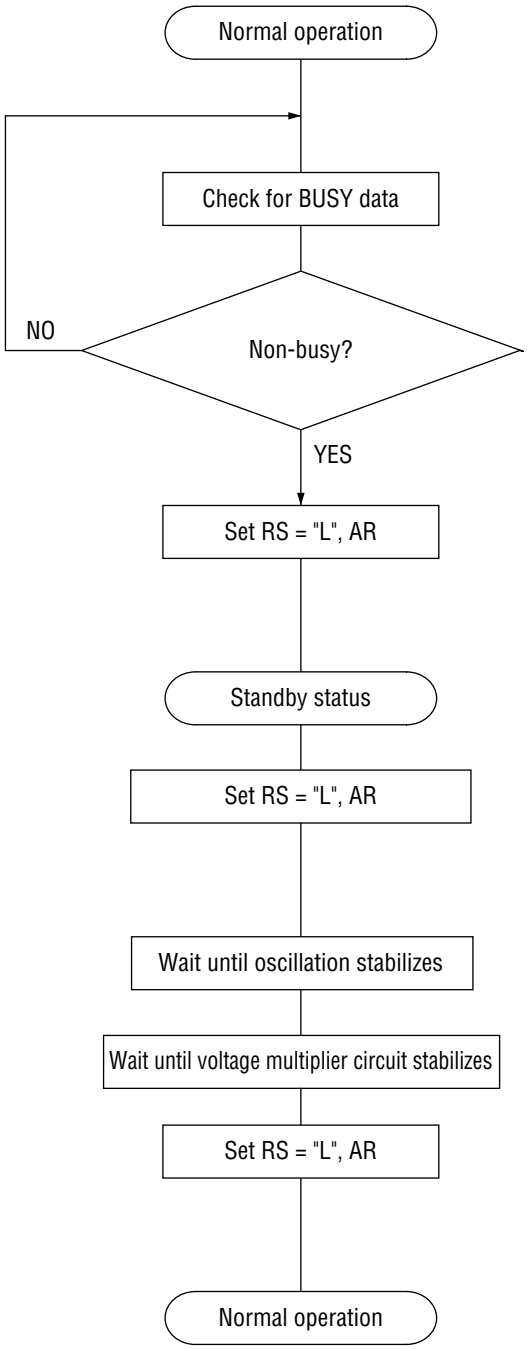
(Standby release, DRAM select)

Note: This wait is a wait during busy period. To detect busy by SO, wait until the busy output is set from "H" to "L".

D7	D6	D5	D4	D3	D2	D1	D0
*	0	1	0	0	*	X	X
						Arbitrary	

(DISP ON)

STBY Setting and Cancellation Flowchart



Original Oscillation Frequency and Frame Frequency

Frame frequency calculation

For 1/33, 1/44, 1/48 DUTY:
(Original oscillation clock cycle) × (1/frequency dividing ratio) × 4224 = frame cycle
.....Formula 1
For 1/41 DUTY:
(Original oscillation clock cycle) × (1/frequency dividing ratio) × 4264 = frame cycle
.....Formula 2

Frame frequency can be calculated by the above formulas.

Example 1) For original oscillation 350 [kHz], frequency dividing ratio 1/1, and 1/33 duty specification:
By formula 1, frame cycle $Tf = 1/(350\times10^3) \times 1 \times 4224 = 12.1$ [ms]
Therefore, frame frequency = 82.9 [Hz]

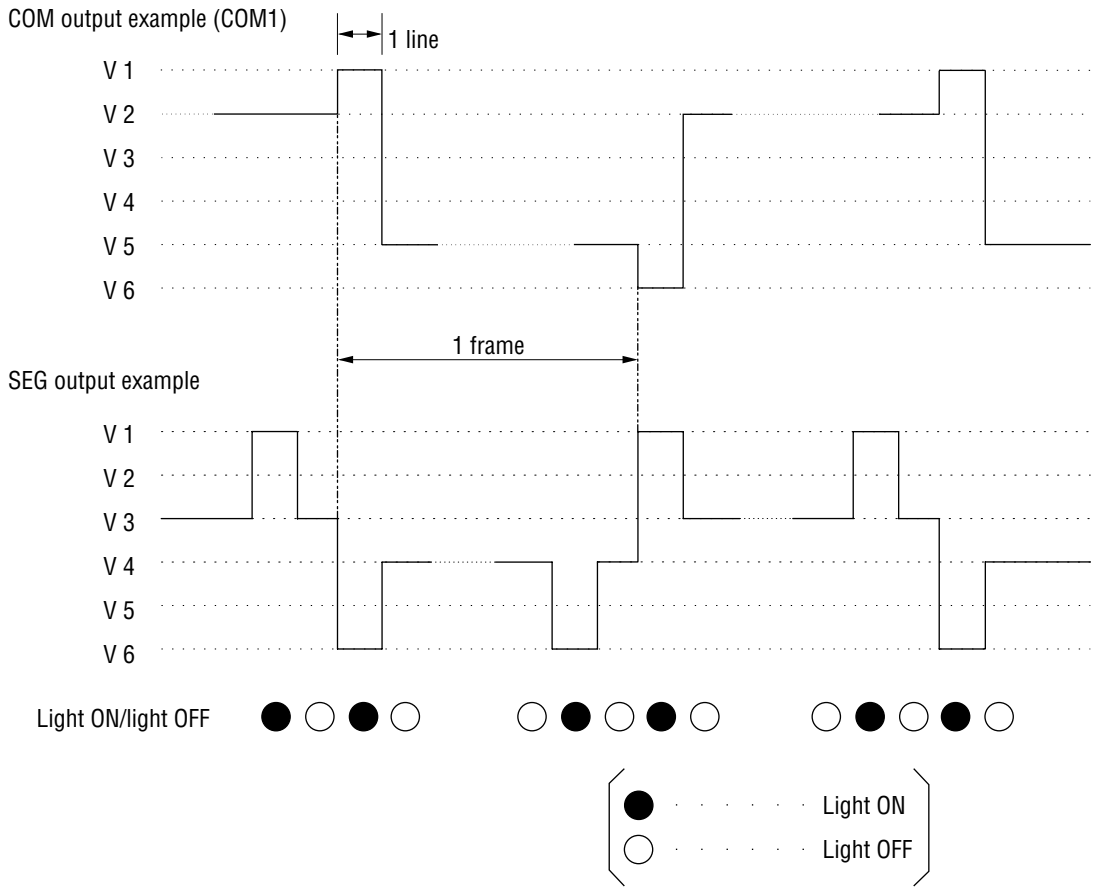
Example 2) For original oscillation 1 [MHz], frequency dividing ratio 1/3, 1/41 duty specification:
By formula 2, frame cycle $Tf = 1/(1\times10^6) \times 3 \times 4264 = 12.8$ [ms]
Therefore, frame frequency = 78.2 [Hz]

Original oscillation frequency and BUSY time

When RAM data is written or read, data processing time (BUSY time) occurs. BUSY time is a maximum of [(original oscillation clock cycle) × 8]. As the original oscillation frequency increases, BUSY time becomes shorter (not influenced by the frequency dividing ratio).

By increasing the original oscillation frequency, BUSY time can be made shorter in proportion. In this case frame frequency also increases. So, set the frequency dividing ratio so that frame frequency reaches a frequency close to the frame frequency to be used.

LCD Drive Power Supply

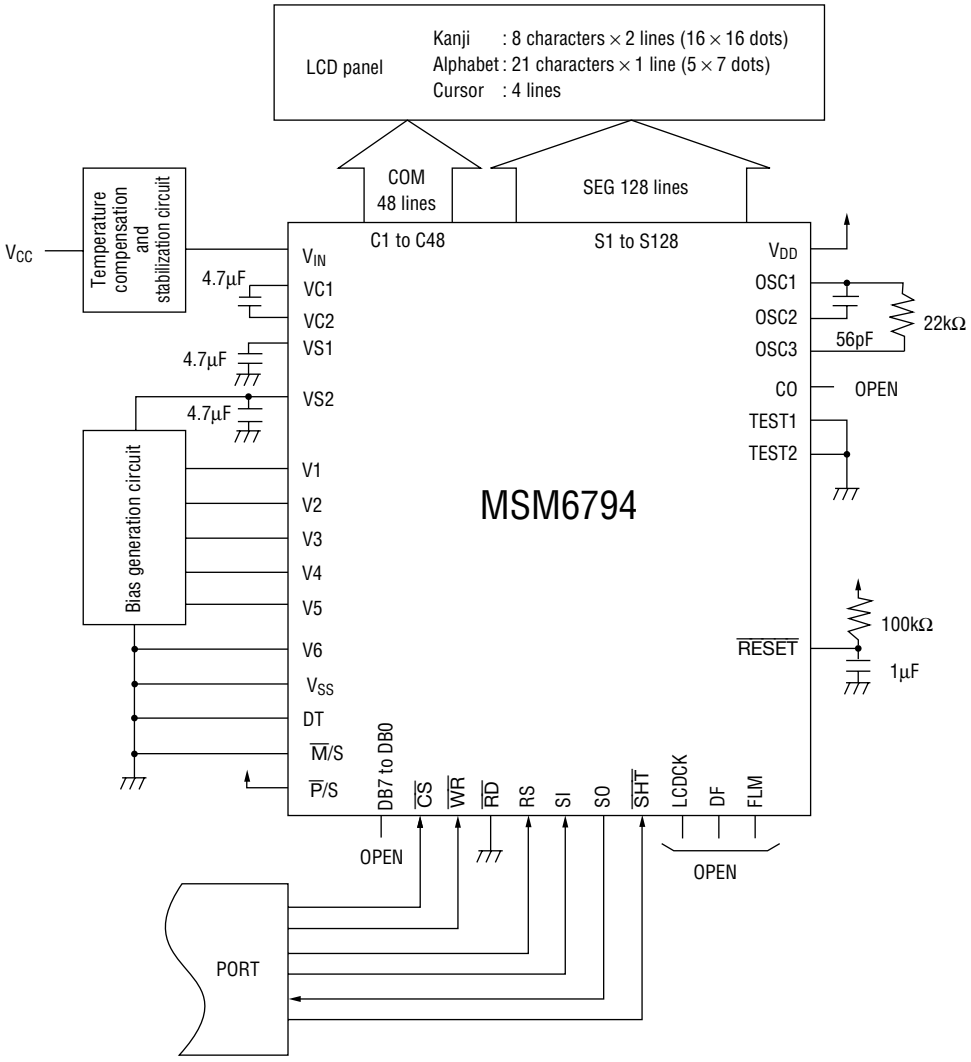


COM DRV input power supply : V1, V2, V5, V6
SEG DRV input power supply : V1, V3, V4, V6

APPLICATION CIRCUITS

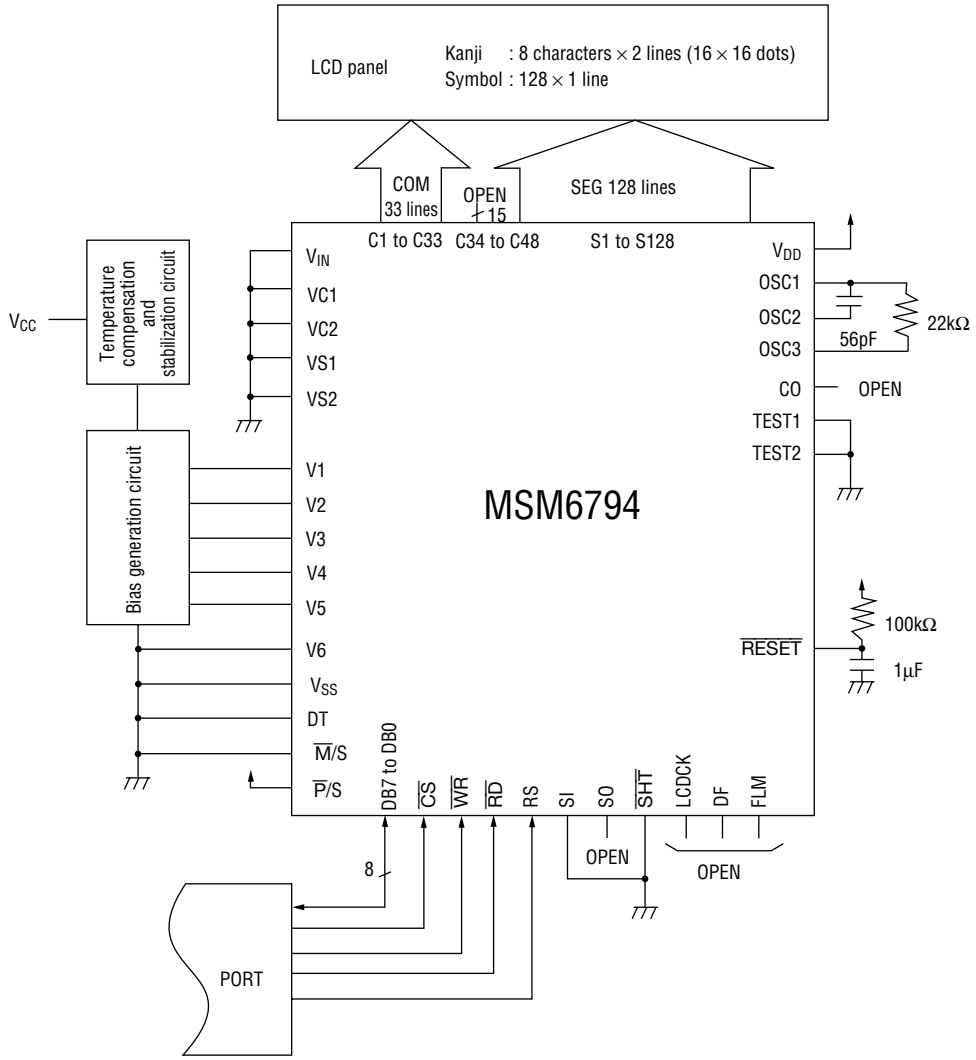
Application example (1)

(1/48 duty, serial interface, voltage multiplier circuit (tripler) used, single chip)



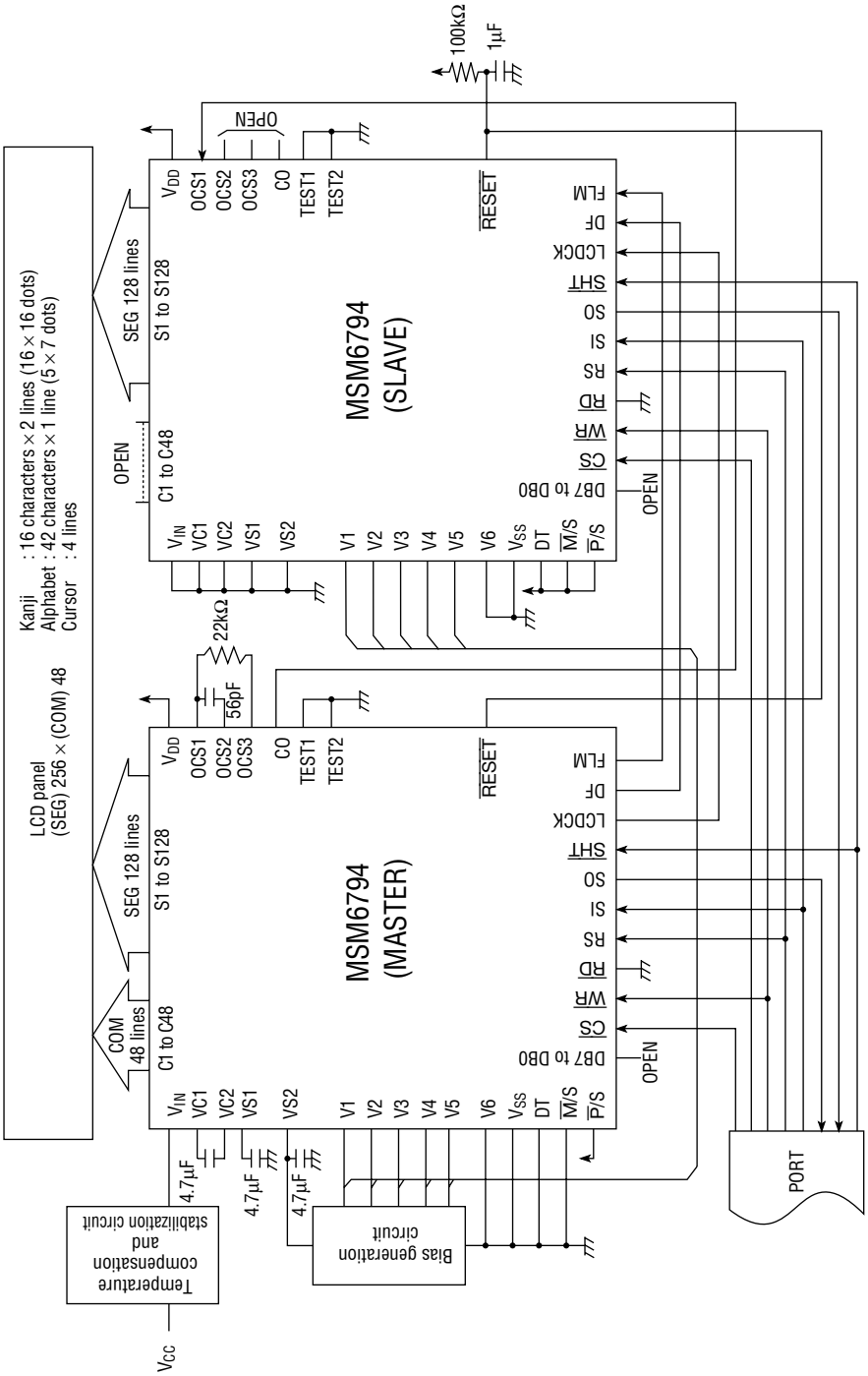
Application example (2)

(1/33 duty, parallel interface, voltage multiplier circuit unused, single chip)



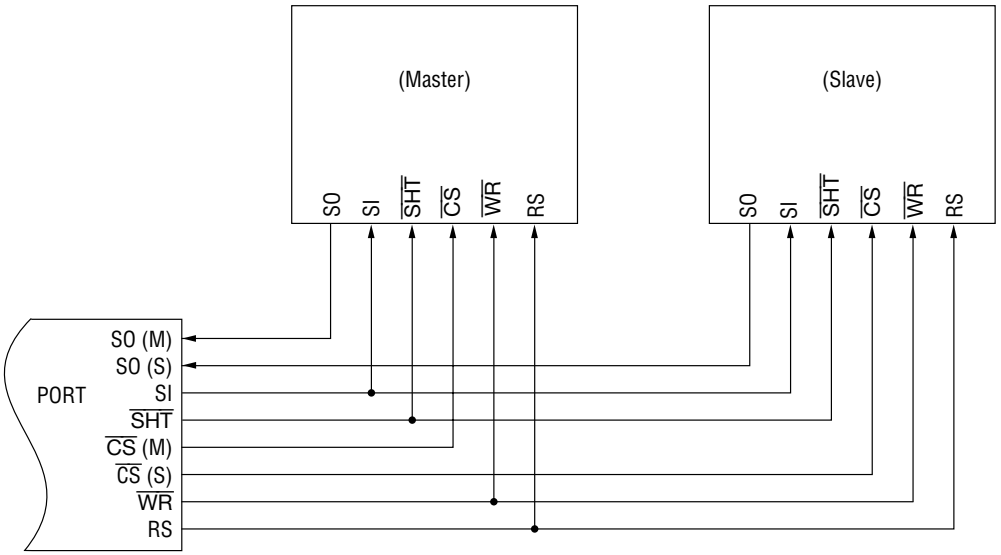
Application example (3)

(1/48 duty, serial interface, 2 chips used, cascade connection)



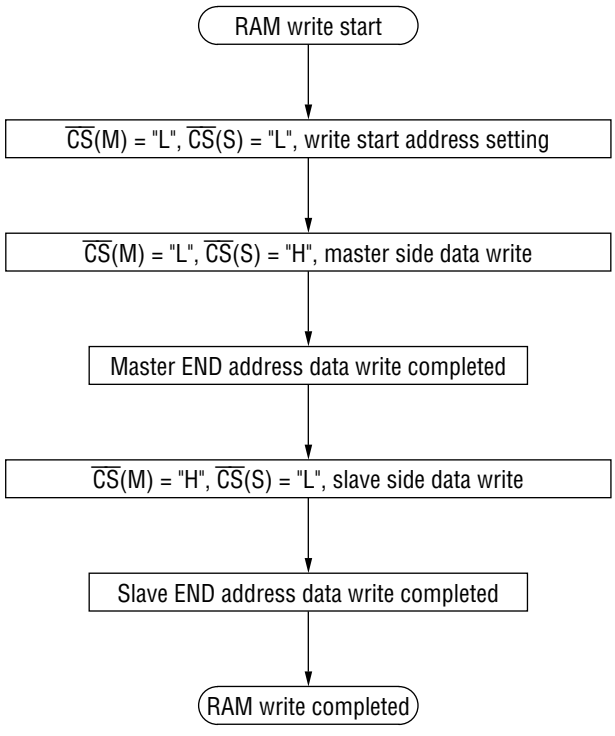
Interface Connection Example

For serial interface (only control signals are described)



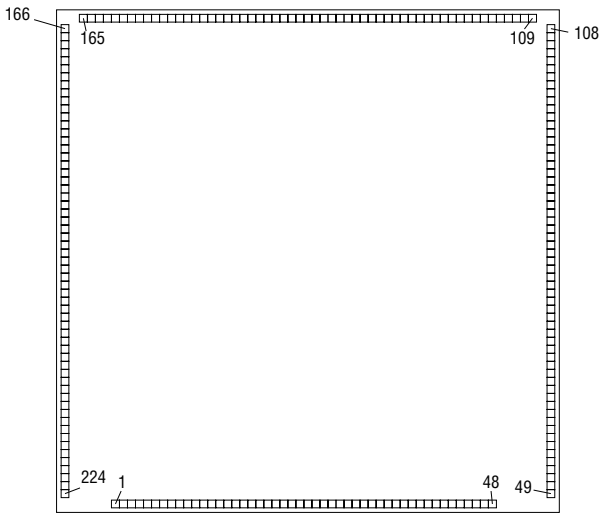
Master and slave control operation

Connect as in the above diagram. The master side and slave side can be selected by setting $\overline{CS}$ to "L" respectively.
Rise or fall the $\overline{CS}$ signal level after confirming NON-BUSY.
Example of continuous writing of RAM data (all master addresses → all slave addresses):



PAD CONFIGURATION (TOP VIEW)

Pad Layout



Pad Coordinates

Pad No.	Pad Name	X(μm)	Y(μm)	Pad No.	Pad Name	X(μm)	Y(μm)	Pad No.	Pad Name	X(μm)	Y(μm)
1	V6	–3377	–3784	26	DB3	271	–3784	51	C46	4058	–3306
2	V4	–3257	–3784	27	DB2	440	–3784	52	C45	4058	–3186
3	V3	–3137	–3784	28	DB1	609	–3784	53	C44	4058	–3066
4	V1	–3017	–3784	29	DB0	778	–3784	54	C43	4058	–2946
5	V_{DD1}	–2897	–3784	30	TEST1	697	–3784	55	C42	4058	–2826
6	V_{DD2}	–2777	–3784	31	TEST2	1098	–3784	56	C41	4058	–2706
7	OSC1	–2647	–3784	32	$\overline{M}$/S	1218	–3784	57	C40	4058	–2586
8	OSC2	–2453	–3784	33	FLM	1399	–3784	58	C39	4058	–2466
9	OSC3	–2284	–3784	34	DF	1568	–3784	59	C38	4058	–2346
10	CO	–2215	–3784	35	LCDCK	1737	–3784	60	C37	4058	–2226
11	V_{SS1}	–1962	–3784	36	DT	1937	–3784	61	C36	4058	–2106
12	V_{SS2}	–1842	–3784	37	V_{DD3}	2057	–3784	62	C35	4058	–1986
13	$\overline{RESET}$	–1712	–3784	38	V_{SS3}	2177	–3784	63	C34	4058	–1866
14	SO	–1519	–3784	39	VS1	2297	–3784	64	C33	4058	–1746
15	SI	–1317	–3784	40	VS2	2417	–3784	65	C32	4058	–1626
16	$\overline{SHT}$	–1186	–3784	41	VC2	2537	–3784	66	C31	4058	–1506
17	$\overline{PS}$	–1066	–3784	42	V_{IN}	2657	–3784	67	C30	4058	–1386
18	$\overline{CS}$	–946	–3784	43	VC1	2777	–3784	68	C29	4058	–1266
19	$\overline{WR}$	–826	–3784	44	V_{DD4}	2897	–3784	69	C28	4058	–1146
20	$\overline{RD}$	–706	–3784	45	V1	3017	–3784	70	C27	4058	–1026
21	RS	–586	–3784	46	V2	3137	–3784	71	C26	4058	–906
22	DB7	–404	–3784	47	V5	3257	–3784	72	C25	4058	–786
23	DB6	–235	–3784	48	V6	3377	–3784	73	C24	4058	–666
24	DB5	–67	–3784	49	C48	4058	–3546	74	C23	4058	–546
25	DB4	–103	–3784	50	C47	4058	–3426	75	C22	4058	–426

Pad No.	Pad Name	X(μm)	Y(μm)	Pad No.	Pad Name	X(μm)	Y(μm)	Pad No.	Pad Name	X(μm)	Y(μm)
76	C21	4058	–306	101	S124	4058	2694	126	S99	1292	3824
77	C20	4058	–186	102	S123	4058	2814	127	S98	1172	3824
78	C19	4058	–66	103	S122	4058	2934	128	S97	1052	3824
79	C18	4058	54	104	S121	4058	3054	129	S96	932	3824
80	C17	4058	174	105	S120	4058	3174	130	S95	812	3824
81	C16	4058	294	106	S119	4058	3294	131	S94	692	3824
82	C15	4058	414	107	S118	4058	3414	132	S93	572	3824
83	C14	4058	534	108	S117	4058	3534	133	S92	452	3824
84	C13	4058	654	109	S116	3332	3824	134	S91	332	3824
85	C12	4058	774	110	S115	3212	3824	135	S99	212	3824
86	C11	4058	894	111	S114	3092	3824	136	S89	93	3824
87	C10	4058	1014	112	S113	2972	3824	137	S88	–28	3824
88	C9	4058	1134	113	S112	2852	3824	138	S87	–147	3824
89	C8	4058	1254	114	S111	2732	3824	139	S86	–267	3824
90	C7	4058	1374	115	S110	2612	3824	140	S85	–387	3824
91	C6	4058	1494	116	S109	2492	3824	141	S84	–507	3824
92	C5	4058	1614	117	S108	2372	3824	142	S83	–627	3824
93	C4	4058	1734	118	S107	2252	3824	143	S82	–747	3824
94	C3	4058	1854	119	S106	2132	3824	144	S81	–867	3824
95	C2	4058	1974	120	S105	2012	3824	145	S80	–987	3824
96	C1	4058	2094	121	S104	1892	3824	146	S79	–1107	3824
97	S128	4058	2214	122	S103	1772	3824	147	S78	–1277	3824
98	S127	4058	2334	123	S102	1652	3824	148	S77	–1347	3824
99	S126	4058	2454	124	S101	1532	3824	149	S76	–1467	3824
100	S125	4058	2574	125	S100	1412	3824	150	S75	–1587	3824

Pad No.	Pad Name	X(μm)	Y(μm)	Pad No.	Pad Name	X(μm)	Y(μm)	Pad No.	Pad Name	X(μm)	Y(μm)
151	S74	–1707	3824	176	S49	–4058	2334	201	S24	–4058	–666
152	S73	–1827	3824	177	S48	–4058	2214	202	S23	–4058	–786
153	S72	–1947	3824	178	S47	–4058	2094	203	S22	–4058	–906
154	S71	–2067	3824	179	S46	–4058	1974	204	S21	–4058	–1026
155	S70	–2187	3824	180	S45	–4058	1854	205	S20	–4058	–1146
156	S69	–2307	3824	181	S44	–4058	1734	206	S19	–4058	–1266
157	S68	–2427	3824	182	S43	–4058	1614	207	S18	–4058	–1386
158	S67	–2547	3824	183	S42	–4058	1494	208	S17	–4058	–1506
159	S66	–2667	3824	184	S41	–4058	1374	209	S16	–4058	–1626
160	S65	–2787	3824	185	S40	–4058	1254	210	S15	–4058	–1746
161	S64	–2907	3824	186	S39	–4058	1134	211	S14	–4058	–1866
162	S63	–3207	3824	187	S38	–4058	1014	212	S13	–4058	–1986
163	S62	–3147	3824	188	S37	–4058	894	213	S12	–4058	–2106
164	S61	–3267	3824	189	S36	–4058	774	214	S11	–4058	–2226
165	S60	–3387	3824	190	S35	–4058	654	215	S10	–4058	–2346
166	S59	–4058	3534	191	S34	–4058	534	216	S9	–4058	–2466
167	S58	–4058	3414	192	S33	–4058	414	217	S8	–4058	–2586
168	S57	–4058	3294	193	S32	–4058	294	218	S7	–4058	–2706
169	S56	–4058	3174	194	S31	–4058	174	219	S6	–4058	–2826
170	S55	–4058	3054	195	S30	–4058	54	220	S5	–4058	–2946
171	S54	–4058	2934	196	S29	–4058	–66	221	S4	–4058	–3066
172	S53	–4058	2814	197	S28	–4058	–186	222	S3	–4058	–3186
173	S52	–4058	2694	198	S27	–4058	–306	223	S2	–4058	–3306
174	S51	–4058	2574	199	S26	–4058	–426	224	S1	–4058	–3426
175	S50	–4058	2454	200	S25	–4058	–546				