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OKI Semiconductor

MSM7718-01

Echo Canceler with ADPCM CODEC

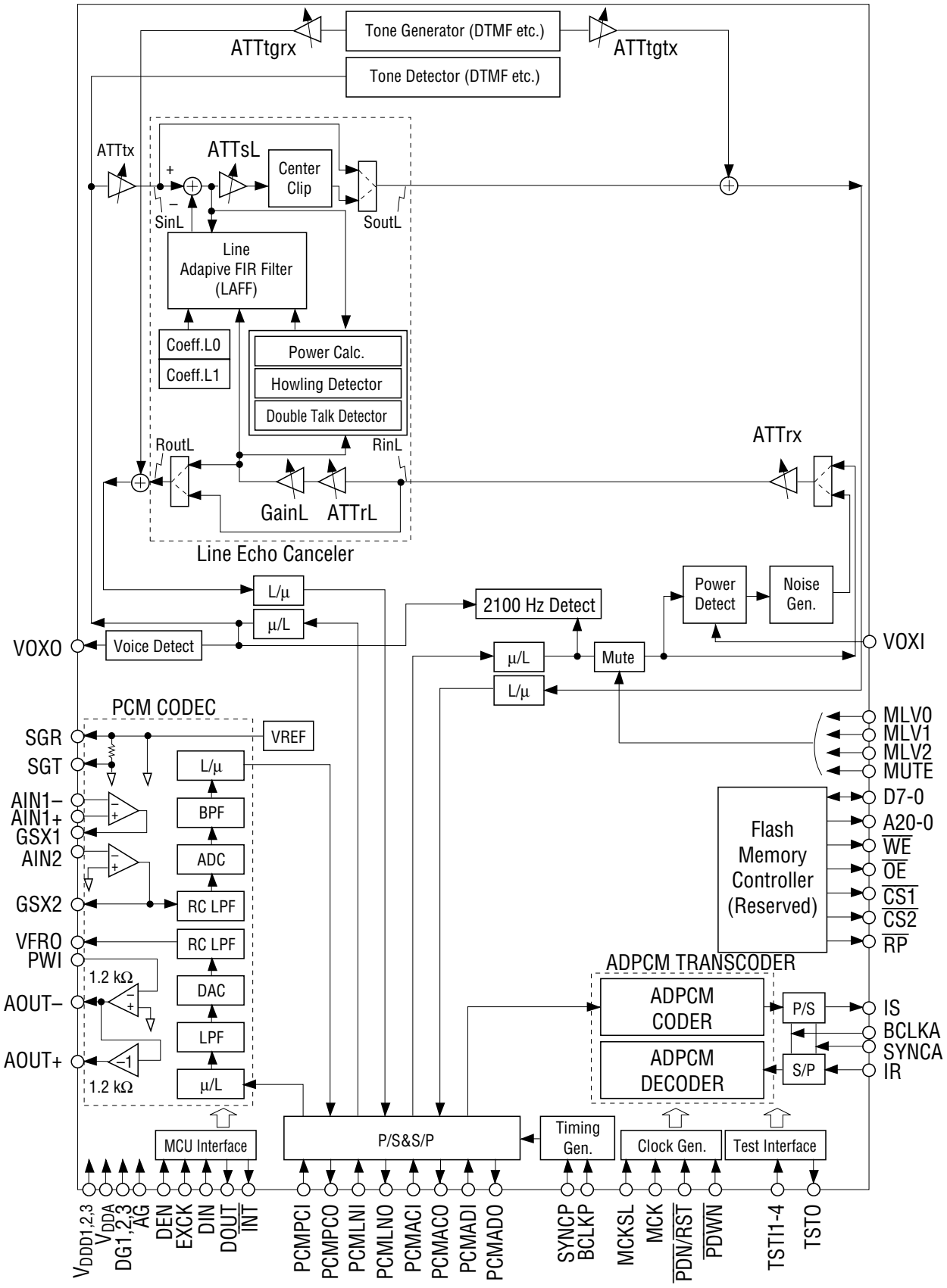
GENERAL DESCRIPTION

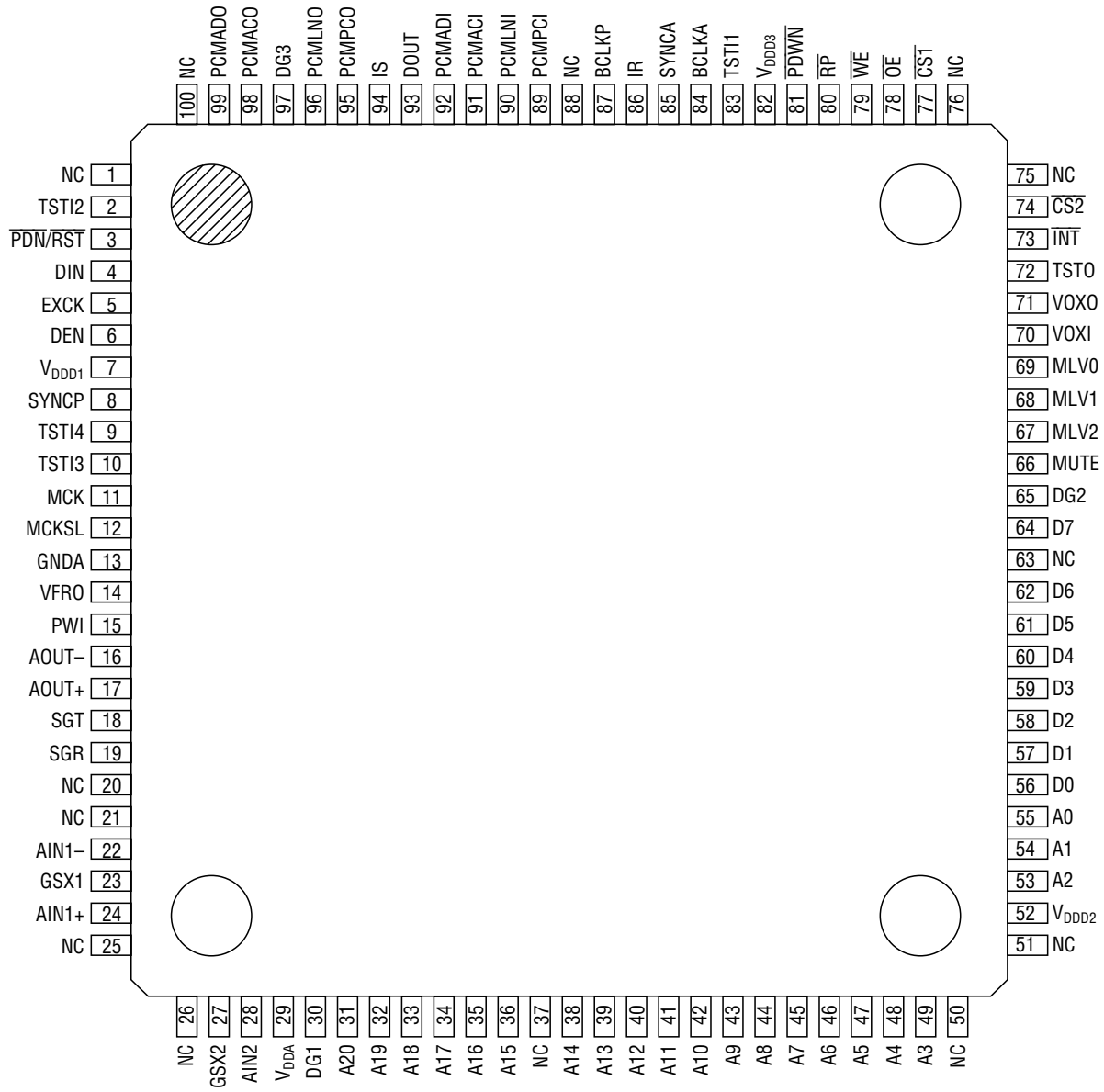
The MSM7718, developed for PHS (Personal Handyphone System) applications, is a CMOS LSI device and contains a line echo canceler and a single channel full-duplex ADPCM transcoder that performs interconversion between voice-band analog signal and 32 kbps ADPCM data. This device includes DTMF tone and several types of tone generation, transmit/receive data mute and gain control, and VOX function and is best suited for master telephones in PHS applications.

FEATURES

- Single 3 V power supply V_{DD} : 2.7 V to 3.6 V
- ADPCM : ITU-T Recommendations G.726 (32 kbps)
- Full-Duplex single channel operation
- Transmit/receive synchronous mode
- PCM interface coding format : μ-law
- Built-in line echo canceler
  - Echo attenuation : 30 dB (typ.)
  - Cancelable echo delay time :
    - Normal speech mode : 23 ms (max.)
    - Line echo canceler expansion mode : 54 ms (max.)
- Serial PCM/ADPCM transmission data rate : 64 kbps to 2048 kbps
- Low power consumption
  - Operating mode : Typically 66 mW (V_{DD} = 3.0 V)
  - Power-down mode : Typically 0.3 mW (V_{DD} = 3.0 V)
- Two analog input gain adjustable amplifier stages
- Analog output stage : Push-pull drive, (direct drive of 350 Ω + 120 nF)
- Master clock frequency : 9.600/19.200 MHz
- Transmit/receive mute, transmit/receive programmable gain control
- Built-in DTMF tone generator and various ringing tones generator
- DTMF tone and call progress tone detection
- Serial MCU interface control
- Built-in VOX control
  - Transmit side : Voice/silence detect
  - Receive side : Background noise generation at the absence of voice signal
- Built-in 2100 Hz tone detection (bidirectional)
- Package:
  100-pin plastic TQFP (TQFP100-1414-0.50-K) (Product name : MSM7718-01TS-K)

BLOCK DIAGRAM





NC: No-connect pin

100-Pin Plastic TQFP

PIN FUNCTIONAL DESCRIPTION

AIN1+, AIN1–, AIN2, GSX1, GSX2

Transmit analog inputs and the outputs for transmit gain adjustment.
AIN1– (AIN2) connects to inverting input of the internal transmit amplifier. AIN1+ connects to non-inverting input of the internal transmit amplifier. GSX1 (GSX2) connects to the internal transmit amplifier output. Refer to Fig.1 for gain adjustment.

VFRO, AOUT+, AOUT–, PWI

Receive analog outputs and the output for receive gain adjustment.
VFRO is the receive filter output. AOUT+ and AOUT– are differential analog signal outputs which can directly drive Z_L (= 350 Ω + 120 nF) or a 1.2 kΩ load. Refer to Fig.1 for gain adjustment. However, these outputs are in high impedance state during power-down.

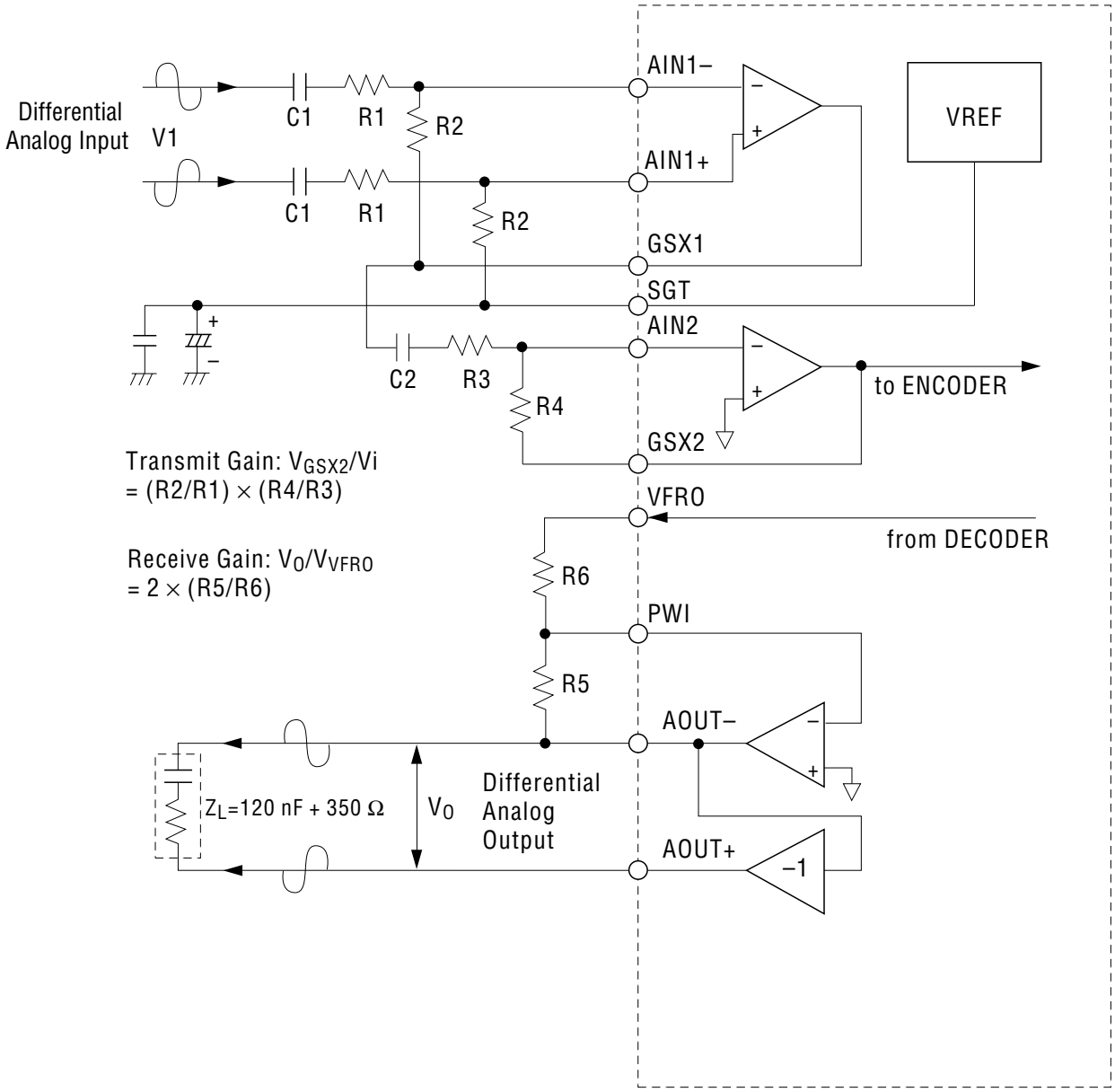


Figure 1 Analog Interface

SGT, SGR

Outputs of the analog signal ground voltage.
SGT outputs the analog signal ground voltage of the transmit system, and SGR outputs the analog signal ground voltage for the receive system. The output voltage is approximately 1.4 V. Connect bypass capacitors of 10 µF and 0.1 µF (ceramic type) between these pins and the AG pin. However to reduce the response time of the receiver power-on, it is recommended to apply bypass capacitors of 1 µF and 0.1 µF. During power-down, the output changes to 0 V.

AG

Analog ground.

DG1, 2, 3

Digital ground.

V_{DDA}

+3 V power supply for analog circuits.

$V_{DDD1, 2, 3}$

+3 V power supply for digital circuits.

$\overline{PDN}/\overline{RST}$

Power-down reset control input.
A logic "0" makes the LSI device enter a power-down state. At the same time, all control register data is reset to the initial state. Set this pin to a logic "1" during normal operating mode. Since the $\overline{PDN}/\overline{RST}$ pin is ORed with CR0-B5 of the control register, set CR0-B5 to digital "0" when using this pin.

$\overline{PDWN}$

Power-down control input.
When set to a logic "0", the device changes to the power-down state, but each bit of control register and internal variables of control register are retained. During normal operation, set this pin to logic "1". Since the $\overline{PDWN}$ pin is ORed with CR0-B6 of the control register, set CR0-B6 to logic "0" when using this pin.

MCK

Master clock input.
The frequency must be 9.6 MHz or 19.2 MHz. The master clock signal is allowed to be asynchronous with SYNCP, SYNCA, BCLKP, and BCLKA.

MCKSL

Master clock selection input.
Set MCKSL to logic "0" when the master clock frequency is 9.6 MHz, and to logic "1" when it is 19.2 MHz.

PCMPCO

PCM data output of the PCM CODEC.
PCM is output from MSB, synchronizing with the rising edge of BCLKP and SYNCP. This pin is in a high impedance state except during 8-bit PCM output. (It is also in a high impedance state during power-down mode.) A pull-up resistor must be connected to this pin because its output is configured as an open drain.

PCMPCI

PCM data input of the PCM CODEC.
PCM is shifted in at the falling edge of the BCLKP signal. The start of the PCM data (MSB) is identified at the rising edge of SYNCP.

PCMADO

PCM data output of the ADPCM transcoder.
PCM is the output data after ADPCM decoder processing and is serially output from MSB in synchronization with the rising edge of BCLKP and SYNCP. However, this signal timing can be controlled at PCM multiplexing by the control register CR1-B5.
(The time slot 1 or 2 can be selected. Refer to Figs. 2-4.)
This pin is in a high impedance state except during 8-bit PCM output. (It is also in an high impedance state during power-down mode.) A pull-up resistor must be connected to this pin because its output is configured as an open drain.

PCMADI

PCM data input of the ADPCM transcoder.
PCM is shifted in at a falling edge of the BCLKP signal and input from MSB. The start of the PCM data (MSB) is identified at the rising edge of SYNCP. However, this signal timing can be controlled at PCM multiplexing by the control register CR1-B5.
(The time slot 1 or 2 can be selected. Refer to Figs. 2-4.)

PCMLNO

PCM receive data output of the line echo canceler.
PCM is output from MSB in a sequential order, synchronizing with the rising edge of BCLKP and SYNCP. However, this signal timing can be controlled at PCM multiplexing by the control register CR2-B3 to B5.
(The time slot of 1 to 7 can be selected. Refer to Figs. 2-4.)
This pin is in a high impedance state except during 8-bit PCM output. (It is also in a high impedance state during power-down mode.) A pull-up resistor must be connected to this pin because its output is configured as an open drain.

PCMLNI

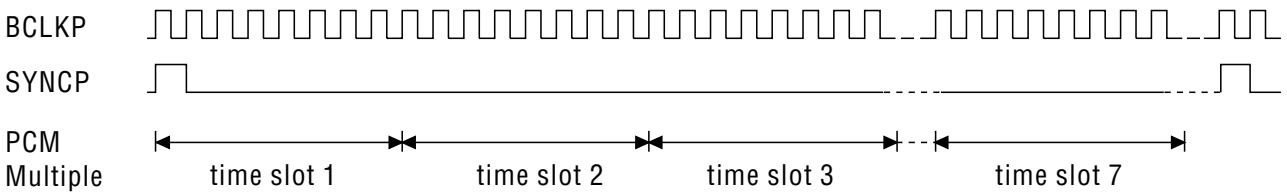
PCM transmit data input of the line echo canceler.
PCM is shifted in at a falling edge of the BCLKP signal and input from MSB. The start of the PCM data (MSB) is identified at the rising edge of SYNCP. However, this signal timing can be controlled at PCM mutiplexing by the control register CR2-B3 to B5.
(One of the time slots 1 to 7 can be selected. Refer to Figs. 2-4.)

PCMACO

PCM transmit data output of the line echo canceler.
PCM is output from MSB in a sequential order, synchronizing with the rising edge of BCLKP and SYNCP. However, this signal timing can be controlled at PCM multiplexing by the control register CR2-B0 to B2. (The time slot 1 to 7 can be selected. Refer to Figs. 2 - 4.)
This pin is in a high impedance state except during 8-bit PCM output.
(It is also in a high impedance sate during power down mode.) A pull-up resistor must be connected to this pin because its output is configured as an open drain.

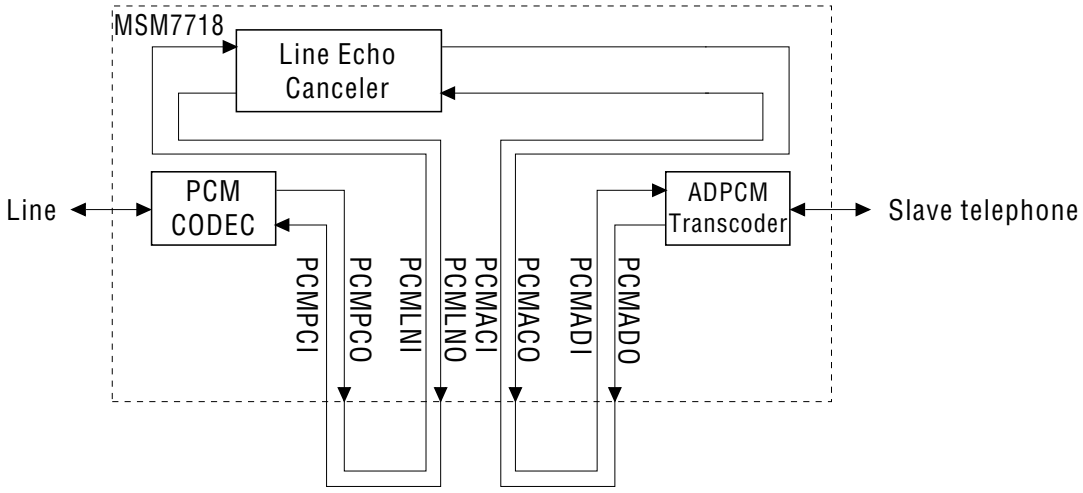
PCMACI

PCM receive data input of the line echo canceler.
PCM is shifted in at a falling edge of BCLKP and input from MSB.
The start of the PCM data (MSB) is identified at the rising edge of SYNCP. However, this signal timing can be controlled at PCM multiplexing by the control register CR2-B0 to B2. (One of the time slots 1 to 7 can be selected. Refer to Figs. 2-4.)



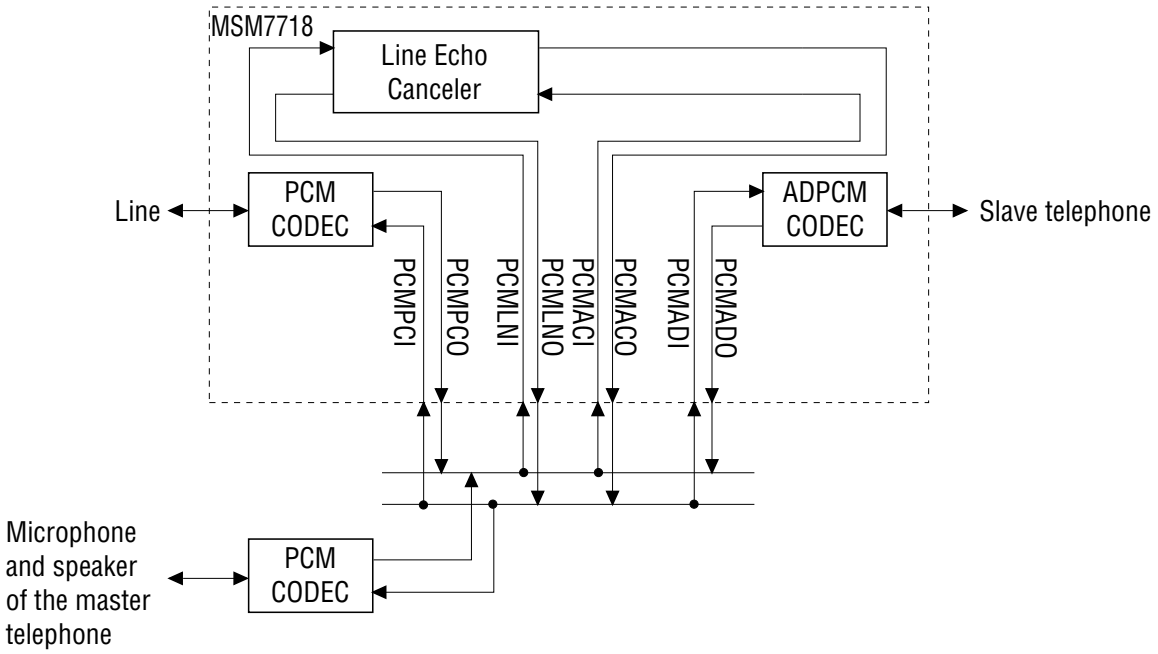
Note : The PCM signals (PCMPCI and PCMPCO) of the PCM CODEC are always assigned to time slot 1.
The PCM signals (PCMADI and PCMADO) of the ADPCM transcoder can be assigned to time slot 1 or 2.
The PCM signals (PCMLNI, PCMLNO, PCMACI, PCMACO) of the line echo canceler can be assigned to one of the time slots 1 to 7. (Multiple timing is controlled by CR1 and CR2.)

Figure 2 PCM Multiple Timing



Note : In this connection, PCMLNI, PCMLNO, PCMACI, and PCMACO should all be assigned to time slot 1 for their output timing (the output timing for the PCM CODEC is always assigned to time slot 1).
Turn on the line echo canceler and establish a route between the slave telephone and the line.

Figure 3 PCM Signal Connection Example 1



Notes : The PCM signals of the ADPCM transcoder are assigned to time slot 2. (The PCM signals of the PCM CODEC are always assigned to time slot 1.) The PCM signals of an external PCM CODEC are assigned to time slot 3.

Route between the line and the slave telephone

PCMLNI and PCMLNO are assigned to time slot 1 and PCMACI and PCMACO are assigned to time slot 2.

Turn on the line echo canceler, and establish the route between the line and the slave telephone.

Route between the master telephone's microphone/speaker (handsfree) and the slave telephone

PCMLNI and PCMLNO are assigned to time slot 3 and PCMACI and PCMACO are assigned to time slot 2.

Turn on the line echo canceler, and establish the route between the microphone/speaker of the master telephone and the slave telephone.

Route between the line and the master telephone's microphone/speaker (handsfree)

PCMLNI and PCMLNO are assigned to time slot 1 and PCMACI and PCMACO are assigned to time slot 3.

Put the line echo canceler into “through mode”, and establish the route between the line and the microphone/speaker of the master telephone.

Various routing can be implemented providing extension of external PCM CODECs.

Figure 4 PCM Signal Connection Example 2

BCLKP

Shift clock input for the PCM data (PCMPCO, PCMPCI, PCMADO, PCMADI, PCMLNO, PCMLNI, PCMACO, PCMACI). The frequency is set in the range of 64 kHz to 2048 kHz.
This signal must be synchronized with the SYNCP signal. (Refer to Fig. 2.)

SYNCP

8 kHz synchronous signal input for transmit and receive PCM data.
This signal must be synchronized with the BCLKP signal. (Refer to Fig. 2.)

IS

Transmit ADPCM data output.
This data is the output data after ADPCM encoding, and is serially output from MSB in synchronization with the rising edge of BCLKA and SYNCA. This pin is an open drain output which remains in a high impedance state during power-down, and requires a pull-up resistor.

IR

Receive ADPCM data input.
ADPCM is shifted in on the rising edge of BCLKA in synchronization with SYNCA and input orderly from MSB.

BCLKA

Shift clock input for the ADPCM data (IS, IR).
The frequency is from 64 kHz to 2048 kHz.
This signal must be synchronized with the SYNCA signal.

SYNCA

8 kHz synchronous signal input for transmit and receive ADPCM data.
Synchronize this data with BCLKA signal. SYNCA is used for indicating the MSB of the serial ADPCM data stream.

DEN, EXCK, DIN, DOUT, $\overline{\text{INT}}$

Serial control ports for MCU interface.
Reading and writing data is performed by an external MCU through these pins. 17-byte control registers are provided in this device.
DEN is the "Enable" control signal input, EXCK is the data shift clock input, DIN is the address and data input, and DOUT is the data output.
Input/output timing is shown in Fig. 5.
$\overline{\text{INT}}$ goes to logic "0" when any change has been found in the tone detection results in the tone detection mode (change in the control register bits CR7-B3, B2), and goes to logic "1" when the data of control register CR7 is read out.

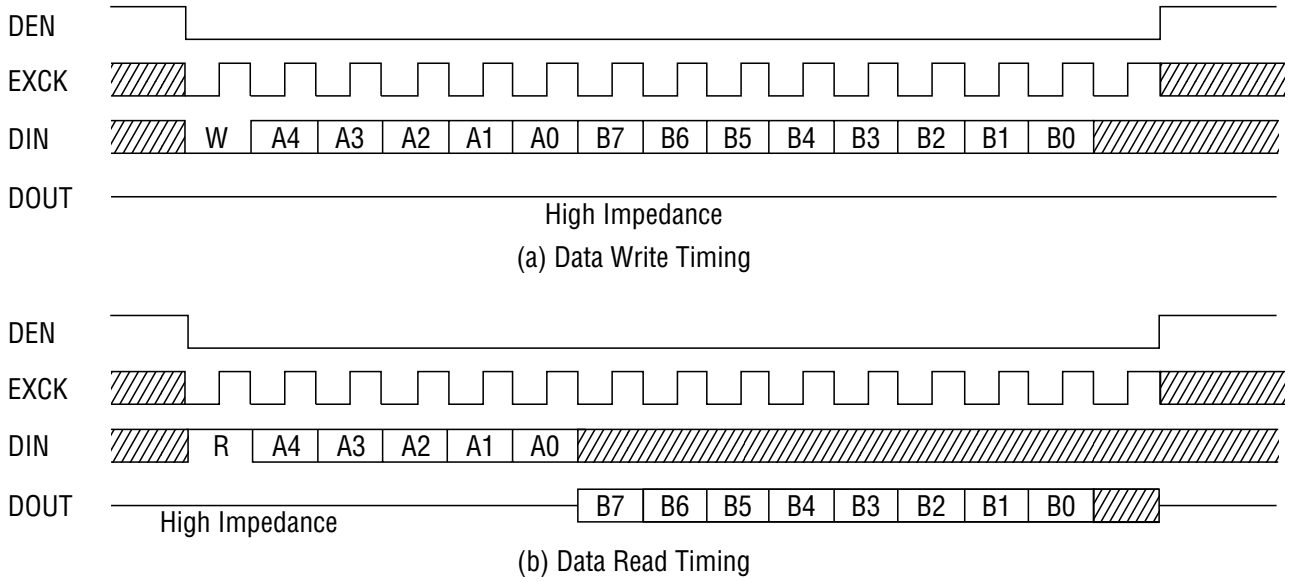


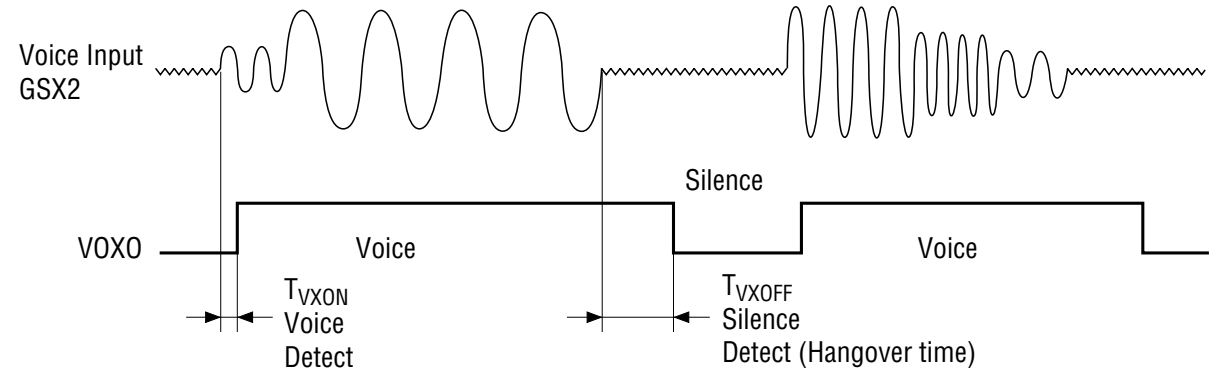
Figure 5 MCU Interface Input/Output Timing

VOXO

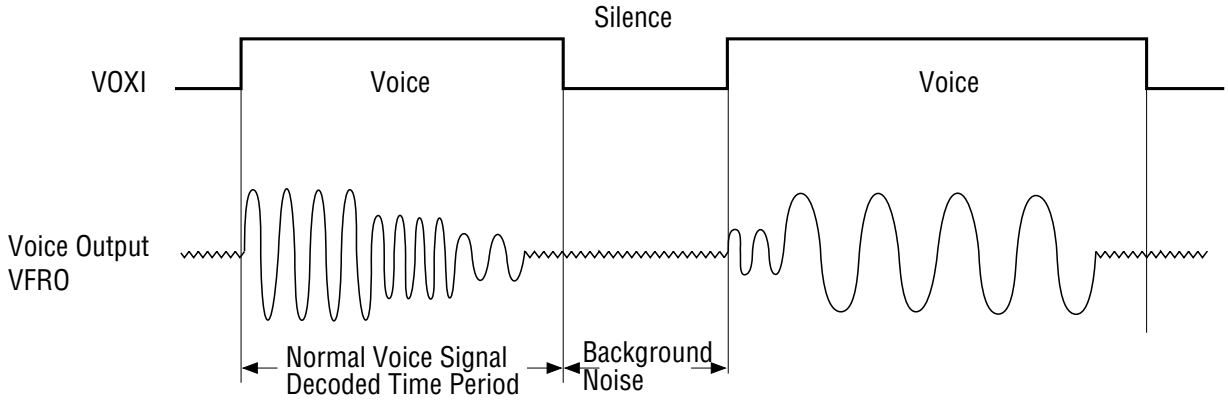
Signal output for transmit VOX function.
The VOX function recognizes the presence or absence of the transmit voice signal by detecting the level of the transmit signal to the line echo canceler . "1" and "0" levels set to this pin correspond to the presence and the absence of voice, respectively. This result appears also at the register data CR7-B7. The signal energy detect threshold is set by the control register data CR6-B6, B5.
The timiging diagram of the VOX function is shown in Fig 6.
The transmit signal to the line echo canceler refers to the signal input to the PCMLNI pin.

VOXI

Signal input for receive VOX function.
The "1" level at VOXI indicates the presence of a voice signal, the decoder block processes normal receive signal, and the voice signal on the PCMACI pin goes through. The "0" level indicates the absence of a voice signal and the background noise generated in this device is output to the line echo canceler.
The background noise amplitude is set by the control register CR6.
Because this signal is ORed with the register data CR6-B3, set the control register data CR6-B3 to logic "0".



(a) Transmit VOX Function Timing Diagram (for Analog Input)



(b) Receive VOX Function (CR6-B3: logic "0") Timing Diagram (for Analog Input)

Note: The VOX function is valid when CR6-B7 is set to logic "1".

Figure 6 VOX Function

MUTE

This pin is used to enable the receive side voice path mute level.
To set the mute level, set this pin to "1".

MLV0, MLV1, MLV2

These pins are used to set the receive side voice path mute level.
For the control method, refer to the control register description (CR1). Since these pins are ORed with CR1-B2, B1, and B0 internally, set the bits of the register to "0" before using this pin.

D7 to D0 (reserved for external memory I/F)

Output of write data, and input-output of read data.

A20 to A0 (reserved for external memory I/F)

External memory address output.

$\overline{WE}$ (reserved for external memory I/F)

Output for write control .

$\overline{OE}$ (reserved for external memory I/F)

Output for read control.

$\overline{CS1}$, $\overline{CS2}$ (reserved for external memory I/F)

Chip select output.

$\overline{RP}$ (reserved for external memory I/F)

Reset/power-down control output for external memory.

TSTI1, TSTI2, TSTI3, TSTI4

Input for test.
Normally fix these pins to logic "0".

TSTI4

Input for mode select.
Fix this pin to logic "0" for normal speech mode.
Fix this pin to logic "1" for line echo canceler expansion mode. Refer to the explanation of CR0 for the operation mode.

TSTO

Output for test.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5	V
Analog Input Voltage	V_{AIN}	—	– 0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.7	—	3.6	V
Operating Temperature	Ta	—	–25	+25	+70	°C
Input High Voltage	V_{IH}	All digital inputs	0.45 × V_{DD}	—	—	V
Input Low Voltage	V_{IL}	All digital inputs	0	—	0.16 × V_{DD}	V
Digital Input Rise Time	t_{Ir}	All digital inputs	—	—	50	ns
Digital Input Fall Time	t_{If}	All digital inputs	—	—	50	ns
Master Clock Frequency	f_{MCK}	MCK	–100ppm	19.2/9.6	+100ppm	MHz
Master Clock Duty Ratio	D_C	MCK	40	50	60	%
Bit Clock Frequency	f_{BCK}	BCLKP, BCLKA	64	—	2048	kHz
Synchronous Pulse Frequency	f_{SYNC}	SYNCP, SYNCA	–1000ppm	8.0	+1000ppm	kHz
Clock Duty Cycle	D_{CK}	BCLKP, BCLKA, EXCK	40	50	60	%
Transmit Sync Pulse Setting Time	t_{XS}	BCLKP to SYNCP, BCLKA to SYNCA	100	—	—	ns
	t_{SX}	SYNCP to BCLKP, SYNCA to BCLKA	100	—	—	ns
	t_{XO}	SYNCP to BCLKP, SYNCA to BCLKA	—	—	100	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLKP to SYNCP, BCLKA to SYNCA	100	—	—	ns
	t_{SR}	SYNCP to BCLKP, SYNCA to BCLKA	100	—	—	ns
	t_{RO}	SYNCP to BCLKP, SYNCA to BCLKA	—	—	100	ns
Receive Sync Pulse Setting Time	t_{WS}	SYNCP, SYNCA	1 BCLK	—	100	µs
PCM, ADPCM Setup Time	t_{DS}	—	100	—	—	ns
PCM, ADPCM Hold Time	t_{DH}	—	100	—	—	ns

Note: If SYNCP and SYNCA are generated from different clocks, do not change the relative timing of the rising edge of SYNCP and that of SYNCA (that is, which rising edge is earlier) after the reset state has been released.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}= 2.7 to 3.6 V, Ta= –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current 1	I_{DD1}	Operating mode, no signal (only the master clock is input)	—	22	40	mA
Power Supply Current 2	I_{DD2}	Power down mode (only the master clock is input)	—	0.2	1	mA
Input Leakage current	I_{IH}	V_I=V_{DD}	—	—	2	µA
	I_{IL}	V_I= 0 V	—	—	0.5	µA
High Level Digital Output Voltage	V_{OH1}	I_{OH}= 0.4 mA	0.5×V_{DD}	—	V_{DD}	V
	V_{OH2}	I_{OH}= 1 µA	0.8×V_{DD}	—	V_{DD}	V
Low Level Digital Output Voltage	V_{OL}	1LSTTL, pull-up resistance : 500 Ω	0	0.2	0.4	V
Digital Output Leakage Current	I_O	IS	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD}= 2.7 to 3.6 V, Ta= –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input Resistance	R_{IN}	AIN+, AIN–, AIN2, PWI	10	—	—	MΩ
Output Load Resistance	R_{L1}	GSX1, GSX2, VFRO	20	—	—	kΩ
	R_{L2}	AOUT+	1.2	—	—	kΩ
	R_{L3}	AOUT–	1.2	—	—	kΩ
Output Load Capacitance	C_{L1}	GSX1, GSX2, VFRO	—	—	100	pF
	C_{L2}	AOUT+	—	—	100	pF
	C_{L3}	AOUT–	—	—	100	pF
Output Voltage Level (*1)	V_{O1}	GSX1, GSX2, VFRO (R_L=20kΩ)	—	—	1.3	V_{PP}
	V_{O2}	AOUT+ (R_L=1.2 kΩ)	—	—	1.3	V_{PP}
	V_{O3}	AOUT– (R_L=1.2 kΩ)	—	—	1.3	V_{PP}
Offset Voltage	V_{OFGX}	VFRO	–100	—	+100	mV
	V_{OFGX}	VFRO	–20	—	+20	mV
SGT, SGR Output Voltage	V_{SG}	SGT, SGR	—	1.4	—	V
SGT Output Impedance	R_{SGT}	SGT	—	40	80	kΩ
SGR Output Impedance	R_{SGR}	SGR	—	4	8	kΩ

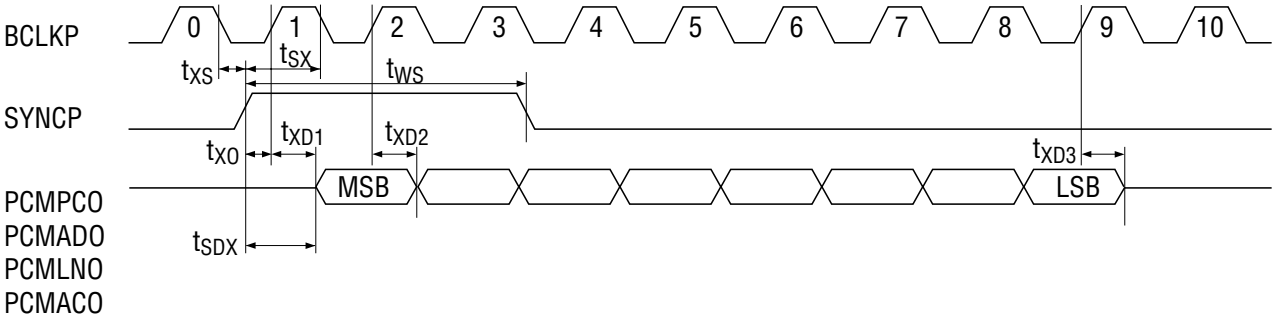
*1 –7.7 dBm (600 Ω) = 0 dBm0, +3.14 dBm0=1.30 V_{PP}

Digital Interface Characteristics

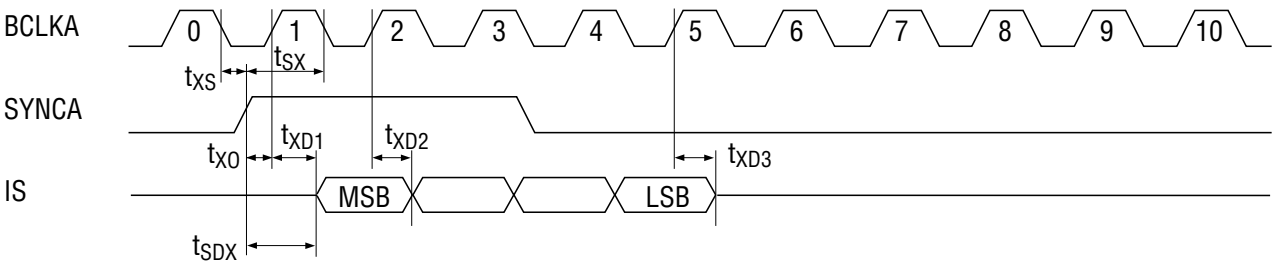
(V_{DD}= 2.7 to 3.6 V, Ta= –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time PCM, ADPCM Interface	t_{SDX}, t_{SDR}	1LSTTL+100 pF pull-up resistance : 500 Ω Values in parentheses apply when Cload = 10 pF, pull-up resistance :≦2 kΩ	0	—	200 (100)	ns
	t_{XD1}, t_{RD1}		0	—	200 (100)	ns
	t_{XD2}, t_{RD2}		0	—	200 (100)	ns
	t_{XD3}, t_{RD3}		0	—	200 (100)	ns
Serial Port Digital Input/Output Setting Time	t_{M1}	Cload=100 pF	50	—	—	ns
	t_{M2}		20	—	—	ns
	t_{M3}		20	—	—	ns
	t_{M4}		50	—	—	ns
	t_{M5}		100	—	—	ns
	t_{M6}		50	—	—	ns
	t_{M7}		50	—	—	ns
	t_{M8}		0	—	—	ns
	t_{M9}		50	—	—	ns
	t_{M10}		50	—	—	ns
	t_{M11}		0	—	—	ns
	t_{M12}		100	—	—	ns
Shift Clock Frequency	f_{ECK}	EXCK	—	—	10	MHz

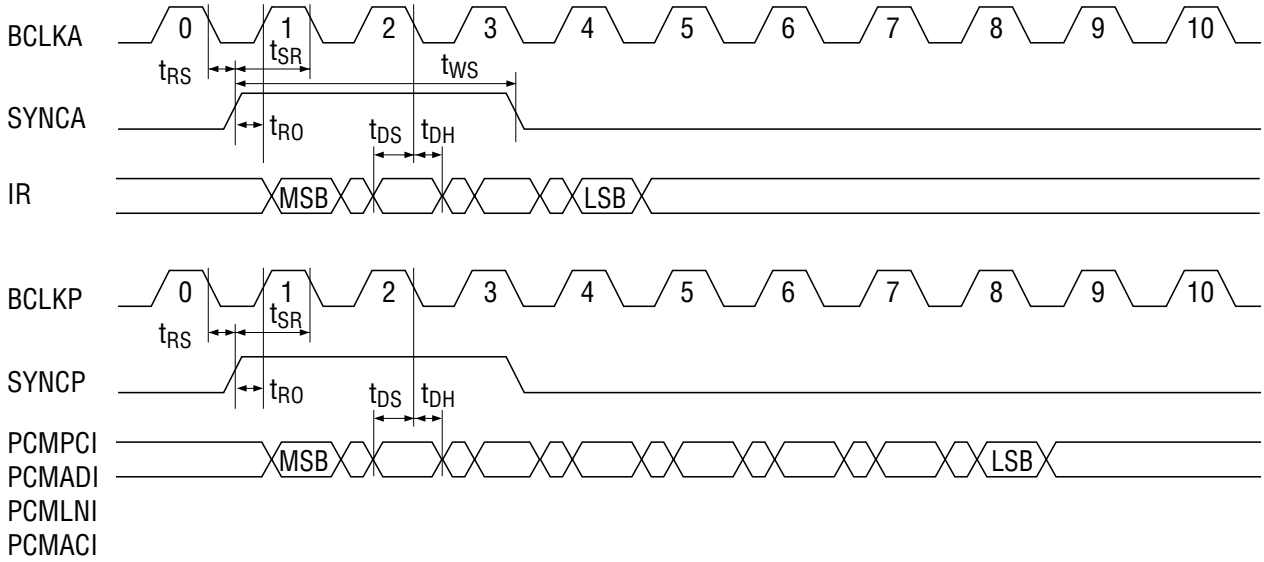
PCM/ADPCM Output Timing



Note : The timing for PCMADO, PCMLNO, and PCMACO shown above reperesents the timing when time slot 1 is selected.

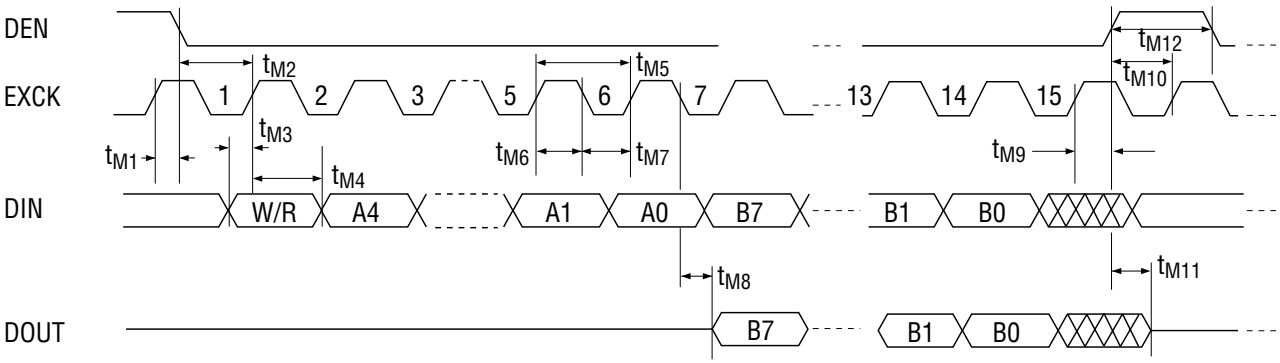


PCM/ADPCM Input Timing



Note : The timing for PCMADI, PCMLNI, and PCMACI shown above represents the timing when time slot 1 is selected.

Serial Port Timing for Microcontroller Interface



AC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq.(Hz)	level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0-60	0	—	25	—	—	dB
	L_{OSS} T2	300-3k			–0.15	—	+0.2	
	L_{OSS} T3	1020			Reference			
	L_{OSS} T4	3300			–0.15	—	+0.8	
	L_{OSS} T5	3400			0	—	0.8	
	L_{OSS} T6	3968.75			13	—	—	
Receive Frequency Response	L_{OSS} R1	0-3000	0	—	–0.15	—	+0.2	dB
	L_{OSS} R2	1020			Reference			
	L_{OSS} R3	3300			–0.15	—	+0.8	
	L_{OSS} R4	3400			0	—	0.8	
	L_{OSS} R5	3968.75			13	—	—	
Transmit Signal to Distortion	SD T1	1020	3	(*2)	35	—	—	dB
	SD T2		0		35	—	—	
	SD T3		–30		35	—	—	
	SD T4		–40		28	—	—	
	SD T5		–45		23	—	—	
Receive Signal to Distortion	SD R1	1020	3	(*2)	35	—	—	dB
	SD R2		0		35	—	—	
	SD R3		–30		35	—	—	
	SD R4		–40		28	—	—	
	SD R5		–45		23	—	—	
Transmit Gain Tracking	GT T1	1020	3	—	–0.2	—	+0.2	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.2	—	+0.2	
	GT T4		–50		–0.5	—	+0.5	
	GT T5		–55		–1.2	—	+1.2	
Receive Gain Tracking	GT R1	1020	3	—	–0.2	—	+0.2	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.2	—	+0.2	
	GT R4		–50		–0.5	—	+0.5	
	GT R5		–55		–1.2	—	+1.2	
Idle Channel Noise	N_{IDLT}	—	AIN=SG	(*2)	—	—	–68 (–75.7)	dBm0p (dBmp)
	N_{IDLR}	—	(*3)	(*2)	—	—	–72 (79.7)	dBm0p (dBmp)
Absolute Signal Amplitude	A_{VT}	1020	0	GSX2	0.285	0.32(*4)	0.359	Vrms
	A_{VR}			VFRO	0.285	0.32(*4)	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq.: 0 to 50 kHz	Noise Level: 50 mVpp	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB

*2. P-message weighted filter used
*3. PCMPCI input code: "11111111" (μ-law)
*4. 0.320 Vrms=0 dBm0=–7.7 dBm

Note : All ADPCM coder and decoder characteristics fully comply with ITU-T Recommendations G.726.

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequence Deviation	Df_{T1}	DTMF Tones		–1.5	—	+1.5	%
	Df_{T2}	Other various tones		–1.5	—	+1.5	%
Tone Reference Output Level (*5)	V_{TL}	Transmit side tone (Gain set value:0dB)	DTMF (Low group)	–10	–8	–6	dBm0
	V_{TH}		DTMF (High group), Others	–8	–6	–4	dBm0
	V_{RL}	Recieve side tone (Gain set value:0dB)	DTMF (Low group)	–10	–8	–6	dBm0
	V_{RH}		DTMF (High group), Others	–8	–6	–4	dBm0
Relative Value of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dB

*5 Not including programmable gain set values

AC Characteristics (Gain Settings)

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Recieve Gain Setting Accurancy	D_G	For all gain set values	–1	0	+1	dB

AC Characteristics (VOX Function)

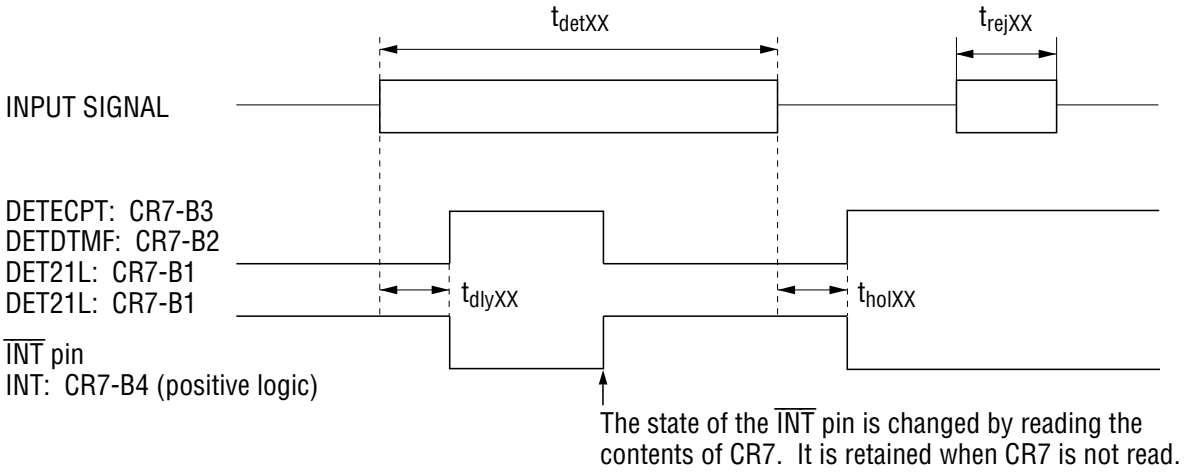
(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX Detection Time	t_{VXON}	Silence→voice	VOXO pin:see Fig.6 Voice/silence differential:10 dB	—	5	—	ms
voice signal ON/OFF Detect Time	t_{VXOFF}	Voice→silence		140/300	160/320	180/340	ms
Transmit VOX Detection Level Accuracy (Voice Detection Level)	D_{VX}	For detection level set values by CRM6-B6,B5		–2.5	0	+2.5	dB

AC Characteristics (Tone Detect Function)

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CPT Detection Frequency	f_{detcp}	—	350	—	640	Hz
CPT Non-detection Frequency	f_{rejcp}	—	700	—	—	Hz
			—	—	250	Hz
CPT Detection Level	V_{detcp}	Input Frequency: 350 to 640 Hz	–39	—	0	dBm0
CPT Non-detection Level	V_{rejcp}	—	—	—	–49	dBm0
CPT Input Signal Continuation Time	t_{detcp}	CPT detected	55	—	—	ms
	t_{rejcp}	CPT not detected	—	—	30	ms
CPT Detection Delay Time	t_{dlycp}	—	30	45	55	ms
CPT Detection Hold Time	t_{holcp}	—	7	16	24	ms
DTMF Detection Frequency	f_{detdt}	At Nominal Frequency	—	—	±1.5	%
DTMF Non-detection Frequency	f_{rejdt}	At Nominal Frequency	±3.8	—	—	%
DTMF Detection Level	V_{detdt}	Input Frequency:Nominal Frequency ±1.5%	–39	—	0	dBm0
DTMF Non-detection Level	V_{rejdt}	—	—	—	–47	dBm0
DTMF Input Signal continuation Time	t_{detdt}	CPT detected	38	—	—	ms
	t_{rejdt}	CPT not detected	—	—	16	ms
DTMF Detection Delay Time	t_{dlydt}	—	16	—	38	ms
DTMF Detection Hold Time	t_{holdt}	—	14	—	25	ms
ANS Detection Frequency	f_{detan}	—	2079	2100	2121	Hz
ANS Non-detection Frequency	f_{rejan}	—	2350	—	—	Hz
			—	—	1900	Hz
ANS Detection Level	V_{detan}	Input Frequency: 2079 to 2121 Hz	–31	—	0	dBm0
ANS Non-detection Level	V_{rejan}	—	—	—	–35	dBm0
ANS Input Signal Continuation Time	t_{detan}	CPT detected	480	—	—	ms
	t_{rejan}	CPT not detected	—	—	420	ms
ANS Detection Delay Time	t_{dlyan}	—	420	450	480	ms
ANS Detection Hold Time	t_{holan}	—	7	12	17	ms



Note : In the case of call progress tone, DTMF tone, and 2100 Hz tone, XX refers to cp, dt, and an respectively.

FUNCTIONAL DESCRIPTION

Control Registers

Table 1 Control Register Map

Reg Name	Address					Contents								R/W
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	—	PDWN	PDN/ RST	—	OPE MODE3	OPE MODE2	OPE MODE1	OPE MODE0	R/W
CR1	0	0	0	0	1	ADPCM MODE	ADPCM RESET	PCM AD SEL	TX MUTE	RX MUTE	RX MLV2	RX MLV1	RX MLV0	R/W
CR2	0	0	0	1	0	PCM PCO MUTE	PCM PCI MUTE	PCM LN SEL2	PCM LN SEL1	PCM LN SEL0	PCM AC SEL2	PCM AC SEL1	PCM AC SEL0	R/W
CR3	0	0	0	1	1	TX GAIN3	TX GAIN2	TX GAIN1	TX GAIN0	RX GAIN3	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR4	0	0	1	0	0	TX TONE GAIN3	TX TONE GAIN2	TX TONE GAIN1	TX TONE GAIN0	RX TONE GAIN3	RX TONE GAIN2	RX TONE GAIN1	RX TONE GAIN0	R/W
CR5	0	0	1	0	1	DTMF/OTHERS SEL	TX TONE SEND	RX TONE SEND	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CR6	0	0	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX. NOISE LEVEL SEL	RX. NOISE LVL1	RX. NOISE LVL0	R/W
CR7	0	0	1	1	1	VOX OUT	Silence level 1	Silence level 0	INT	DET CPT	DET DTMF	BUSY/ DET21L	RPM/ DET21A	R
CR8	0	1	0	0	0	LECTHR (HCL)*	LECCLR1	LECCLR2	LECHD	LECCCLP (NLP)*	LECHLD (ADP)*	LECATT (ATT)*	LECGC (GC)*	R/W
CR9	0	1	0	0	1	AECTHR (HCL)*	—	AECCLR	AECHD	AECCCLP (NLP)*	AECHLD (APD)*	AECATT (ATT)*	AECGC (GC)*	R/W
CR10	0	1	0	1	0	SEND/ REC	MEM SEL	ADPCM MODE1	ADPCM MODE0	CMD3	CMD2	CMD1	CMD0	R/W
CR11	0	1	0	1	1	ST7/ A7	ST6/ A6	ST5/ A5	ST4/ A4	ST3/ A3	ST2/ A2	ST1/ A1	ST0/ A0	R/W
CR12	0	1	1	0	0	ST15/ A15	ST14/ A14	ST13/ A13	ST12/ A12	ST11/ A11	ST10/ A10	ST9/ A9	ST8/ A8	R/W
CR13	0	1	1	0	1	—	—	—	ST20/ A20	ST19/ A19	ST18/ A18	ST17/ A17	ST16/ A16	R/W
CR14	0	1	1	1	0	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	R/W
CR15	0	1	1	1	1	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	R/W
CR16	1	0	0	0	0	—	—	—	SP20	SP19	SP18	SP17	SP16	R/W
CR17	1	0	0	0	1	D7/CA7	D6/CA6	D5/CA5	D4/CA4	D3/CA3	D2/CA2	D1/CA1	D0/CA0	R/W
CR18	1	0	0	1	0	WA7	WA6	WA5	WA4	D TONE3/ WA3	D TONE2/ WA2	D TONE1/ WA1	D TONE0/ WA0	R/W

R/W : Read/write enable R : Read only register

* : These are the symbols of control pins used in the MSM7602 (echo canceler LSI device).

(1) CR0 (Basic operating mode settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	—	PDWN	PDN/RST	—	OPE MODE3	OPE MODE2	OPE MODE1	OPE MODE0
Initial value *	0	0	0	0	0	0	0	0

* : Indicates the value to be set when a resetting is made through the $\overline{PDN}/\overline{RST}$ pin. (Also when reset by bit 5 (B5, PDN/RST), the other bits of CR0 are reset to initial values.)

B7 ... Not used

B6 ... Power-down (entire system) 0: Power-on 1: Power-down
ORed with the inverted external power-down signals
Set the $\overline{PDWN}$ pin to "1" when this data is used. The control registers and their internal variables are not reset.

B5 ... Power-down reset (entire system) 0: Power-on 1: Power-down reset
ORed with the inverted external power-down reset signals
Set the $\overline{PDN}/\overline{RST}$ pin to "1" when this data is used .

B4 ... Not used

B3, 2, 1, 0 ..... Selection of an operating mode

(0, 0, 0, 0) : Initial mode
This mode enables a change (see Figure 15-1,2) in memory that contains internal default values such as tone generation frequencies.
In this mode, the PCM output pin acts to output idle patterns and the PCM input pin acts to input idle patterns. When a reset or power-down occurs or when power down is released, the device enters the initial mode about 200 ms after that.

(0, 0, 0, 1) : Reserved

(0, 0, 1, 0) : Normal speech mode (see Figure 7-1)
This mode enables call services between a slave telephone and a line (including tone generation) and detection of a DTMF tone and a call progress tone.
The internal process enables the tone detector. The ADPCM encoder/decoder, the tone generator, and the line echo canceler become operative and can be controlled by the contents of the control registers.

(0, 0, 1, 1) to (0, 1, 0, 0) : Reserved

(0, 1, 0, 1) : Line echo canceler expansion mode (see Figure 7-2)
This mode can expand the delay time of the line echo canceler up to 54 ms.
Concerning the internal processing, the ADPCM encoder/decoder, the line echo canceler, and the tone generator become operative and can be controlled by the contents of the control registers.

In addition, 2100 Hz tone of PCMLNI and PCMACI (bidirectional) can be detected.

(0, 1, 1, 0) to (1, 1, 1, 1) : Reserved

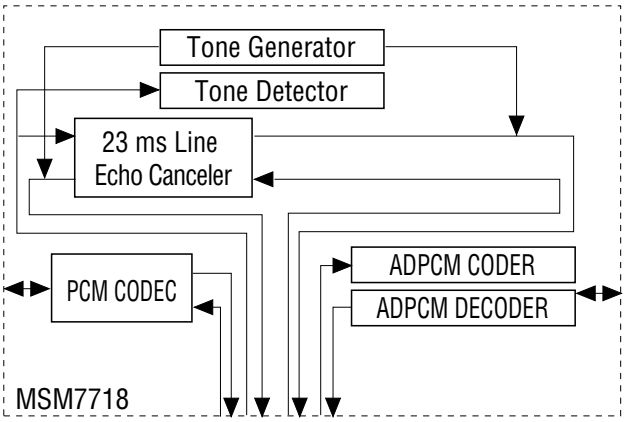


Figure 7-1 Normal Speech Mode

Note :

- When the MSM7718 is used in normal speech mode, set the TSTI4 pin to "0".
- In normal speech mode, the tone detector can detect call progress tone and DTMF tone by PMLNI input.

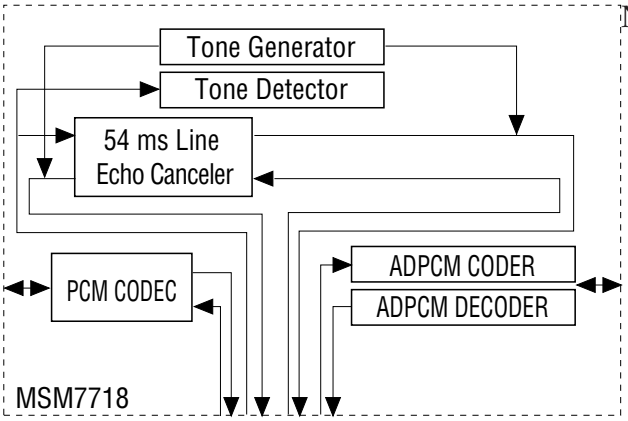


Figure 7-2 Line Echo Canceler Expansion Mode

Note :

- When the MSM7718 is used in line echo canceler expansion mode, set the TSTI4 pin to digital "1".
- In line echo canceler expansion mode, the tone detector can detect not only call progress tone and DTMF tone by PMLNI input but also 2100 Hz tone by PCMLNI and PCMACI input (bidirectional).
- The PCM CODEC does not operate in this mode. A capacitor is required between SGT and ground and between SGR and ground (see Application Circuit).

(2) CR1 (Setting of ADPCM operating mode and PCM I/O signals)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	ADPCM MODE	ADPCM RESET	PCM AD SEL	TX MUTE	RX MUTE	RX MLV2	RX MLV1	RX MLV0
Initial value	0	0	0	0	0	0	0	0

B7 ... ADPCM algorithm 0: 32 kbps (G.726) 1: Reserved
B6 ... Transmitter/receiver ADPCM resetting (conforming to G.726) 1: Reset
B5 ... PCM I/O multiple timing control (PCMADI and PCMADO pins) of the ADPCM CODEC
0: Time slot 1 1: Time slot 2
B4 ... Muting of transmitter ADPCM data 1: Mute
B3 ... Muting of receiver ADPCM data 1: Muting specified by bits B2, B1, and B0 is enabled.
This bit is valid when the MUTE pin is "0".
B2, B1, B0 ... Setting of a receiver voice path mute level

(MLV2, MLV1, MLV0) =
(0, 0, 0) : Through
(0, 0, 1) : – 6 dB
(0, 1, 0) : –12 dB
(0, 1, 1) : –18 dB
(1, 0, 0) : –24 dB
(1, 0, 1) : –30 dB
(1, 1, 0) : –36 dB
(1, 1, 1) : MUTE

(3) CR2 (Setting of PCM I/O multiple control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	PCM PCO MUTE	PCM PCI MUTE	PCM LN SEL2	PCM LN SEL1	PCM LN SEL0	PCM AC SEL2	PCM AC SEL1	PCM AC SEL0
Initial value	0	0	0	0	0	0	0	0

B7 ... ON or OFF of the PCM signal of the transmitter side of the PCM CODEC (PCMPCO pin)
0: ON 1: OFF
When this bit is "1" (OFF), the PCMPCO pin transmits a PCM idle pattern.

B6 ... ON or OFF of the PCM signal of the receiver side of the PCM CODEC (PCMPCI pin)
0: ON 1: OFF
When this bit is "1" (OFF), the PCMPCI pin receives a PCM idle pattern.

B5, 4, 3 .... PCM I/O multiple timing control (PCMLNI and PCMLNO pins) of the line echo canceler (see Table 2)

B2, 1, 0 .... PCM I/O multiple timing control (PCMACI and PCMACO pins) of the line echo canceler (see Table 2)

Table 2 PCM Multiple Timing Control Table

B5 (B2	B4 B1	B3 B0)	Corresponding time slot
0	0	0	None
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Note : When bits B5 to B3 or B2 to B0 are all zeros, the internal process inputs a PCM idle pattern. In this case, the outputs are all in high impedance state for all time slots.

(4) CR3 (Transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	TX GAIN3	TX GAIN2	TX GAIN1	TX GAIN0	RX GAIN3	RX GAIN2	RX GAIN1	RX GAIN0
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5, 4 ..... Adjustment of the transmit signal gain [ATTtx]
(see Table 3)
B3, 2, 1, 0 ..... Adjustment of the receive signal gain [ATTrx]
(see Table 3)

Table 3 Transmit/Receive Signal Gain Setting

B7	B6	B5	B4	Transmit signal gain	B3	B2	B1	B0	Receive signal gain
1	0	0	0	–16 dB	1	0	0	0	–16 dB
1	0	0	1	–14 dB	1	0	0	1	–14 dB
1	0	1	0	–12 dB	1	0	1	0	–12 dB
1	0	1	1	–10 dB	1	0	1	1	–10 dB
1	1	0	0	–8 dB	1	1	0	0	–8 dB
1	1	0	1	–6 dB	1	1	0	1	–6 dB
1	1	1	0	–4 dB	1	1	1	0	–4 dB
1	1	1	1	–2 dB	1	1	1	1	–2 dB
0	0	0	0	0 dB	0	0	0	0	0 dB
0	0	0	1	+2 dB	0	0	0	1	+2 dB
0	0	1	0	+4 dB	0	0	1	0	+4 dB
0	0	1	1	+6 dB	0	0	1	1	+6 dB
0	1	0	0	+8 dB	0	1	0	0	+8 dB
0	1	0	1	+10 dB	0	1	0	1	+10 dB
0	1	1	0	+12 dB	0	1	1	0	+12 dB
0	1	1	1	+14 dB	0	1	1	1	+14 dB

This table is for gains of transmit/receive voice signals.

(5) CR4 (Adjustment of tone generator gain)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	TX TONE GAIN3	TX TONE GAIN2	TX TONE GAIN1	TX TONE GAIN0	RX TONE GAIN3	RX TONE GAIN2	RX TONE GAIN1	RX TONE GAIN0
Initial value	0	0	0	0	0	0	0	0

B7, 6, 5, 4 ..... Transmit side gain adjustment for the tone generator [ATTtgtx] (see Table 4)
B3, 2, 1, 0 ..... Receive side gain adjustment for the tone generator [ATTtgrx] (see Table 5)

Table 4 Setting of Transmit Side Gain of Tone Generator

B7	B6	B5	B4	Tone generator gain	B7	B6	B5	B4	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

Table 5 Setting of Receive Side Gain of Tone Generator

B3	B2	B1	B0	Tone generator gain	B3	B2	B1	B0	Tone generator gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	–8 dB
0	1	1	1	–22 dB	1	1	1	1	–6 dB

Settings of Table 5 are made in relation to the following tone levels:

DTMF tone (Low frequency group) : –2 dBm0
DTMF tone (High frequency group) and other tone : 0 dBm0

For example, when bits B3, B2, B1, and B0 are set to "1, 1, 1, 1" (–6 dB), the PCMLNO pin outputs a tone of the following levels:

DTMF tone (Low frequency group) : –8 dBm0
DTMF tone (High frequency group) and other tone : –6 dBm0

The default value change command enables the gain adjustment by –1 dB step.
Writing "13CAh" into the address 00D8h adds a gain of –1 dB to the values in the above table. The default value is "1634h".

(6) CR5 (Setting of tone generator operating mode and tone frequency)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	DTMF/OTHERS SEL	TX TONE SEND	RX TONE SEND	TONE4	TONE3	TONE2	TONE1	TONE0
Initial value	0	0	0	0	0	0	0	0

B7 ... Selection of DTMF signal or others (S, F, or R tone)
0: Others 1: DTMF signal
B6 ... Transmission of transmit side tone 0: Not transmit 1: Transmit
B5 ... Transmission of receive side tone 0: Not transmit 1: Transmit
B4, 3, 2, 1, 0 ... Setting of a tone frequency (see Table 6)

Table 6 Setting of Tone Generator Frequencies

(a) when B7 = "1" (DTMF tone)

B4	B3	B2	B1	B0	Description	B4	B3	B2	B1	B0	Description
*	0	0	0	0	697 Hz + 1209 Hz (1)	*	1	0	0	0	852 Hz + 1209 Hz (7)
*	0	0	0	1	697 Hz + 1336 Hz (2)	*	1	0	0	1	852 Hz + 1336 Hz (8)
*	0	0	1	0	697 Hz + 1477 Hz (3)	*	1	0	1	0	852 Hz + 1477 Hz (9)
*	0	0	1	1	697 Hz + 1633 Hz (A)	*	1	0	1	1	852 Hz + 1633 Hz (C)
*	0	1	0	0	770 Hz + 1209 Hz (4)	*	1	1	0	0	941 Hz + 1209 Hz (*)
*	0	1	0	1	770 Hz + 1336 Hz (5)	*	1	1	0	1	941 Hz + 1336 Hz (0)
*	0	1	1	0	770 Hz + 1477 Hz (6)	*	1	1	1	0	941 Hz + 1477 Hz (#)
*	0	1	1	1	770 Hz + 1633 Hz (B)	*	1	1	1	1	941 Hz + 1633 Hz (D)

(b) When B7 = "0" (Others)
The Table below lists default frequencies. "00000" to "00011" ("B4, B3, B2, B1, B0") are tones, which are modulated by sinewave. "01000" to "01011" are wamble tones, and "10000" to "10111" are single tones. For procedures to change frequencies, see the next page.

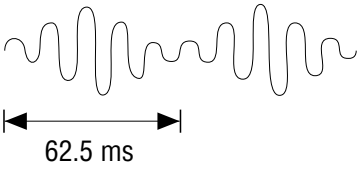
B4	B3	B2	B1	B0	Description	B4	B3	B2	B1	B0	Description
0	0	0	0	0	400/0H – 16 Hz Sine wave modulation	1	0	0	0	0	400 Hz Single tone
0	0	0	0	0	3000/0H – 16 Hz Sine wave modulation	1	0	0	0	1	1000 Hz Single tone
0	0	0	1	0	2700/0H – 16 Hz Sine wave modulation	1	0	0	0	1	2000 Hz Single tone
0	0	0	1	1	*/*H – 16 Hz Sine wave modulation	1	0	0	1	1	2667 Hz Single tone
0	0	1	0	0	—	1	0	1	0	0	1300 Hz Single tone
0	0	1	0	1	—	1	0	1	0	1	2080 Hz Single tone
0	0	1	1	0	—	1	0	1	1	0	*Hz Single tone
0	0	1	1	1	—	1	0	1	1	1	*Hz Single tone
0	1	0	0	0	513/636 Hz 12 Hz Wamble	1	1	0	0	0	—
0	1	0	0	1	800/1000 Hz 8 Hz Wamble	1	1	0	0	1	—
0	1	0	1	0	2000/2667 Hz 8 Hz Wamble	1	1	0	1	0	—
0	1	0	1	1	*/*Hz *Hz Wamble	1	1	0	1	1	—
0	1	1	0	0	—	1	1	1	0	0	—
0	1	1	0	1	—	1	1	1	0	1	—
0	1	1	1	0	—	1	1	1	1	0	—
0	1	1	1	1	—	1	1	1	1	1	—

Frequencies of tones (other than DTMF signals) to be generated by the tone generator can be changed. Tone frequencies can be changed in the Initial mode. See Figure 15-1 for procedures to change tone frequencies. The related subaddresses are shown below.

Modulation by 16 Hz sine wave

B4	B3	B2	B1	B0	Subaddress 1 (Frequency 1) *1
0	0	0	0	0	164h
0	0	0	0	1	165h
0	0	0	1	0	166h
0	0	0	1	1	167h

Modulation by 16 Hz sine wave



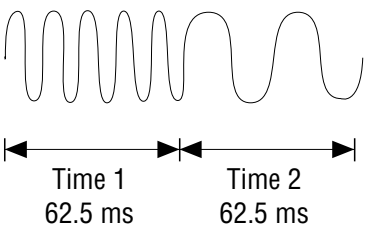
Wamble

B4	B3	B2	B1	B0	Subaddress 1 (Frequency 1) *1	Subaddress 2 (Frequency 2) *1	Subaddress 3 (Time 1) *2	Subaddress 4 (Time 2) *2
0	1	0	0	0	168h	16Ch	170h	174h
0	1	0	0	1	169h	16Dh	171h	175h
0	1	0	1	0	16Ah	16Eh	172h	176h
0	1	0	1	1	16Bh	16Fh	173h	177h

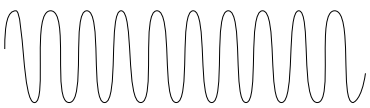
Single tone

B4	B3	B2	B1	B0	Subaddress 1 (Frequency 1) *1
1	0	0	0	0	178h
1	0	0	0	1	179h
1	0	0	1	0	17Ah
1	0	0	1	1	17Bh
1	0	1	0	0	17Ch
1	0	1	0	1	17Dh
1	0	1	1	0	17Eh
1	0	1	1	1	17Fh

8 Hz wamble tone



Transmit single tone



*1 Transmitted Tone Frequency = A × 8.192 (A = frequency)
ex. When frequency = 1000 Hz, 1000 × 8.192 = 9011.2 = 9011d (eliminate after the decimal point) = 2333h

*2 Wamble Frequency (Tone Transmit time) = (A/B)/2 – 1
(A = Transmitted tone frequency, B = wamble frequency)
ex. When wamble frequency is 8 Hz, tone frequency = 2667 Hz.
(2667/8)/2 – 1 = 166.69 = 166d (eliminate after the decimal point) = A6h

(7) CR6 (VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX. NOISE LEVEL SEL	RX. NOISE LVL1	RX. NOISE LVL0
Initial value	0	0	0	0	0	0	0	0

B7 ... Turns ON or OFF the VOX function. 0: OFF, 1: ON

B6, 5 ... Setting of transmit side voice or silence detection level

(0, 0) : –20 dBm0
(0, 1) : –25 dBm0
(1, 0) : –30 dBm0
(1, 1) : –35 dBm0

Note: • The detection level is changeable by inserting the pad of –1 dB to –5 dB in addition to the above values.

• Write $16384 \times 10^{(-A/20)}$ at address "175h". (A=pad)
Example: When –1 dB pad is inserted, $16384 \times 10^{(-(-1)/20)}$
=18383.15=18383d (eliminate after the decimal point)=47CFh

B4 ... Setting of hangover time (T_{VXOFF}) (see Figure 6)

0: 160 ms 1: 320 ms

B3 ... VOX input signal (receiver side)

0: Transmits an internal background noise.
1: Transmits a voice reception signal.
Set the VOXI pin to "0" to use this data.

B2 ... Setting of a receiver side background noise level

0: Automatic internal setting
1: Reserved

B1, 0 ... Externally-set background noise level

(0, 0) : No noise
(0, 1) : –55 dBm0
(1, 0) : –45 dBm0
(1, 1) : –35 dBm0

(8) CR7 (Detection register : read-only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	Silence level 1	Silence level 0	INT	DET CPT	DET DTMF	BUSY/ DET21L	PRM/ DET21A
Initial value	0	0	0	0	0	0	0	0

B7 ... Detection of transmit side voice or noise

0: Silence 1: Voice

B6, 5 ... Transmit side silence level (indicator)

(0, 0) : –10 dB or less with respect to the detection level defined by CR6-B6, B5.
(0, 1) : –5 to –10 dB with respect to the detection level defined by CR6-B6, B5.
(1, 0) : 0 to –5 dB with respect to the detection level defined by CR6-B6, B5.
(1, 1) : 0 dB or more. Refer to the detection level defined by CR6-B6, B5.
Note : The above outputs are valid only when the VOX function is enabled by bit 7 of CR6.

B4 ... External interrupt signal

Goes to a logic "0" when any change has been found in the tone detection results for call progress tone, DTMF tone, and 2100 Hz tone.
Goes to a logic "1" when the CR7 control register is read out .
The inverted state of this bit (B4) is output to the $\overline{INT}$ pin.

B3 ... Detection of a call progress tone 1: Detected 0: Not detected
B2 ... Detection of a DTMF tone 1: Detected 0: Not detected
B1 ... PCMLNI input 2100 Hz tone detection (DET21L: valid only in the line echo canceler expansion mode)
1: Detected 0: Not detected
B0 ... PCMACI input 2100 Hz tone detection (DET21A: valid only in the line echo canceler expansion mode)
1: Detected 0: Not detected

(9) CR8 (Setting of line echo canceler operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	LECTHR (HCL)*1	LECCLR1	LECCLR2	LECHD	LECCCLP (NLP)*1	LECHLD (ADP)*1	LECATT (ATT)*1	LECGC (GC)*1
Initial value	1	0	0	0	0	0	0	0

*1 Names of control pins used in the MSM7602

B7 ... "Through" mode control bit for the line echo canceler.
In the "Through" mode, RinL and SinL data is output directly to RoutL and SoutL respectively.
1: "Through" mode 0: Normal mode (echo cancellation)
B6 ... Selects whether or not to clear the coefficient 1 of the adaptive FIR filter (LAFF) used by the line echo canceler.
1: Resets the coefficient
0: Normal operation
B5 ... Selects whether or not to clear the coefficient 2 of the adaptive FIR filter (LAFF) used by the line echo canceler.
1: Resets the coefficient
0: Normal operation
B4 ... Howling detector (HD) ON/OFF control 1: ON 0: OFF
B3 ... Turns ON or OFF the center clip function which forcibly sets the SoutL output of the line echo canceler to minimum positive value when it is –57 dBm0 or less.
1: Center clip function ON
0: Center clip function OFF
B2 ... Selects whether or not to update the coefficient of the adaptive FIR filter (LAFF) for the line echo canceler.
1: Coefficient fixed mode
0: Normal mode (updates the coefficient)
B1 ... Turns ON or OFF the ATT function which prevents howling from occurring by means of attenuators ATTsL and ATTrL provided for the RinL input and the SoutL output of the line echo canceler.
When a signal is input to RinL only, the attenuator ATTsL of the SoutL output is activated. When a signal is input to SinL only or to both SinL and RinL, the attenuator ATTrL of the RinL input is activated. Their ATT values are both about 6 dB.
1: ATT OFF
0: ATT ON
B0 ... Turns ON or OFF the gain control function which controls the RinL input level and prevents howling from occurring by the gain controller (GainL) for the RinL input of the line echo canceler.
The gain controller adjusts the RIN level when it is –24 dBm0 or above, and it has the control range of 0 to –8.5 dB.
1: Gain control ON
0: Gain control OFF

(10) CR9 : Reserved (Setting of acoustic echo canceler operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	AECTHR (HCL)*1	—	AECCLR	AECHD	AECCCLP (NLP)*1	AECHLD (ADP)*1	AECATT (ATT)*1	AECGC (GC)*1
Initial value	1	0	0	0	0	0	0	0

*1 Names of control pins used in the MSM7602

B7 ... Acoustic echo canceler through-mode control bit
In this mode, RinA data and SinA data are through-output to RoutL and SoutL respectively.
1: Through mode 0: Normal mode (echo cancellation)

B6 ... Not used

B5 ... Selects whether or not to clear the coefficient of the adaptive FIR filter (AAFF) for the acoustic echo canceler.
1: Resets the coefficient 0: Normal operation

B4 ... Howling detector (HD) ON/OFF control 1: ON 0: OFF

B3 ... Turns ON or OFF the center clip function which forcibly sets the Sout output of the acoustic echo canceler to a minimum positive value when it is –57 dBm0 or less.
1: Center clip function ON
2: Center clip function OFF

B2 ... Selects whether or not to update the coefficient of the adaptive FIR filter (AAFF) for the acoustic echo canceler.
1: Coefficient Fixed mode
0: Normal mode (updates the coefficient.)

B1 ... Turns ON or OFF the ATT function which prevents howling from occurring by means of attenuators ATTrA and ATTsA provided for the RinA input and the SoutA output of the acoustic echo canceler.
When a signal is input to RinA only, the attenuator ATTsA of the SoutA output is activated. When a signal is input to SinA only or to both SinA and RinA, the attenuator ATTrA of the RinA input is activated. Their ATT values are both about 6 dB.
1: ATT OFF
0: ATT ON

B0 ... Turns ON or OFF the gain control function which controls the RinA input level and prevents howling from occurring by the gain controller (GainA) for the RinA input of the acoustic echo canceler.
The gain controller starts controlling when the RIN level is –24 dBm0 or above and has the control range of 0 to –8.5 dB.
1: Gain control ON
0: Gain control OFF

(11) CR10 (External memory (flash memory) interface control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	SEND/ REC	MEM SEL	ADPCM MODE1	ADPCM MODE0	CMD3	CMD2	CMD1	CMD0
Initial value	0	0	0	0	0	0	0	0

B7 ... Reserved (connection to the recording interface)

B6 ... Reserved (selection of external memory)

B5, 4 ... Reserved (selection of recording/playback ADPCM compression mode)

B3, 2, 1, 0 ... Reserved (memory interface command)

(0, 0, 0, 0) : NOP

(0, 0, 0, 1) : Reserved

(0, 0, 1, 0) : Reserved

(0, 0, 1, 1) : Reserved

(0, 1, 0, 0) : Reserved

(0, 1, 0, 1) : Reserved

(0, 1, 1, 0) : Reserved

(0, 1, 1, 1) : Reserved

(1, 0, 0, 0) : Reserved

(1, 0, 0, 1) : Reserved

(1, 0, 1, 0) : Reserved

(1, 0, 1, 1) : Reserved

(1, 1, 0, 0) : Reserved

(1, 1, 0, 1) : MDWR (Change default)
Writes the data of CR17 (D0 to D7) and CR16 (D8 to D15) in the lower byte of default storage memory. The address is specified by A0 to A7 of CR11 and A8 to A15 of CR12.

(1, 1, 1, 0) : Reserved

(1, 1, 1, 1) : Reserved

(12) CR11, 12, 13 (Memory address register 1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	ST7/ A7	ST6/ A6	ST5/ A5	ST4/ A4	ST3/ A3	ST2/ A2	ST1/ A1	ST0/ A0
Initial value	—	—	—	—	—	—	—	—

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	ST15/ A15	ST14/ A14	ST13/ A13	ST12/ A12	ST11/ A11	ST10/ A10	ST9/ A9	ST8/ A8
Initial value	—	—	—	—	—	—	—	—

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	—	—	—	ST20/ A20	ST19/ A19	ST18/ A18	ST17/ A17	ST16/ A16
Initial value	—	—	—	—	—	—	—	—

CR11 to 13 : Registers storing an address (A0 to A20) required for the default value change command

Since CR13 is assigned "0h", no setting is requited for it.

(13) CR14, 15, 16 (Memory address register 2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Initial value	—	—	—	—	—	—	—	—

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
Initial value	—	—	—	—	—	—	—	—

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	—	—	—	SP20	SP19	SP18	SP17	SP16
Initial value	—	—	—	—	—	—	—	—

CR14 to 16: When the default value change command is used, the bit 7 to bit 0 of CR16 correspond to the D15 to D8 of write data.

Note : CR14 and CR15 are the reserved registers.

(14) CR17 (Memory data register)

	B7	B6	B5	B4	B3	B2	B1	B0
CR17	D7/CA7	D6/CA6	D5/CA5	D4/CA4	D3/CA3	D2/CA2	D1/CA1	D0/CA0
Initial value	—	—	—	—	—	—	—	—

CR17 is the register to store the data used by the default value store command.

(15) CR18 (Setting of tone detection frequency, memory address register 3)

	B7	B6	B5	B4	B3	B2	B1	B0
CR18	WA7	WA6	WA5	WA4	D TONE3/ WA3	D TONE2/ WA2	D TONE1/ WA1	D TONE0/ WA0
Initial value	—	—	—	0	0	0	0	0

D TONE3 to 0: Valid only when the tone generator is operating (except for the initial mode)
B7, 6, 5, 4 ... Not used
B3, 2, 1, 0 ... Setting of a tone frequency (see Table 7)

Table 7 Setting of Tone Detector Frequencies

B3	B2	B1	B0	Frequency	B3	B2	B1	B0	Frequency
0	0	0	0	697 Hz + 1209 Hz (1)	1	0	0	0	697 Hz + 1477 Hz (3)
0	0	0	1	770 Hz + 1209 Hz (4)	1	0	0	1	770 Hz + 1477 Hz (6)
0	0	1	0	852 Hz + 1209 Hz (7)	1	0	1	0	852 Hz + 1477 Hz (9)
0	0	1	1	941 Hz + 1209 Hz (*)	1	0	1	1	941 Hz + 1477 Hz (#)
0	1	0	0	697 Hz + 1336 Hz (2)	1	1	0	0	697 Hz + 1633 Hz (A)
0	1	0	1	770 Hz + 1336 Hz (5)	1	1	0	1	770 Hz + 1633 Hz (B)
0	1	1	0	852 Hz +1336 Hz (8)	1	1	1	0	852 Hz + 1633 Hz (C)
0	1	1	1	941 Hz + 1336 Hz (0)	1	1	1	1	941 Hz + 1633 Hz (D)

Direct Access to Default Store Memory (See Figs.8-1, 8-2)

The contents of the default store memory can be changed (e.g., to change tone detection levels and tone generation frequencies) in the initial mode (CR0-B3 to CR0-B0="0000").
Refer to the following procedure:

1. Set the default value store memory address (CR11, CR12).
   Set the write data into CR16 and CR17.

2. When writing data to the upper byte, set the DMWR (change default) command (CR10-B3 to CR10-B0="1101").

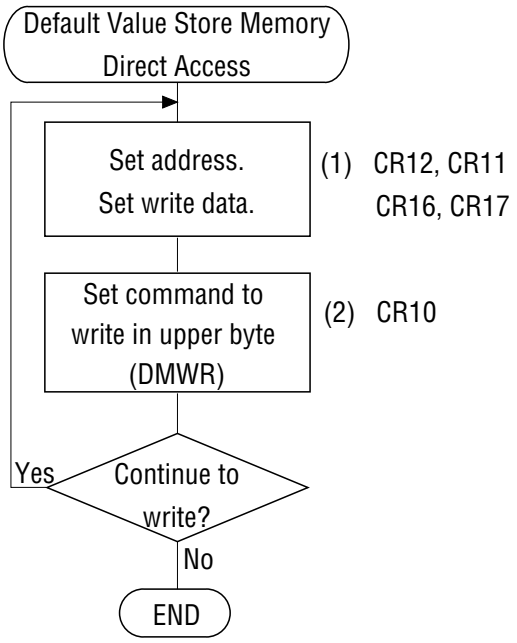


Figure 8-1 Flow Chart of Default Value Store Memory Direct Access

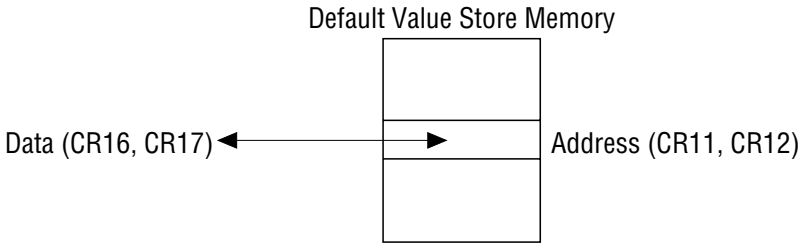
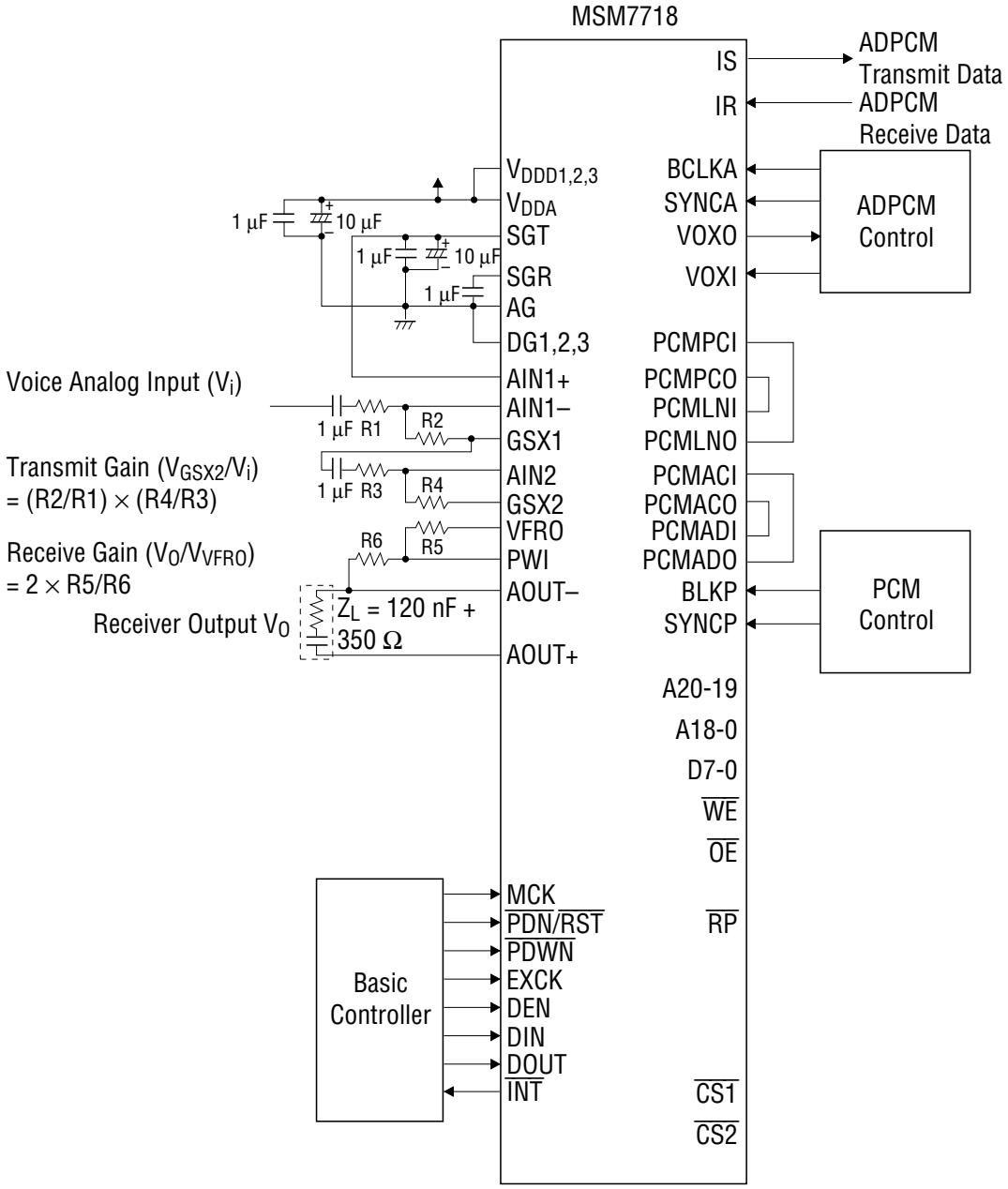


Figure 8-2 Memory Map for Default Value Store Memory Direct Access

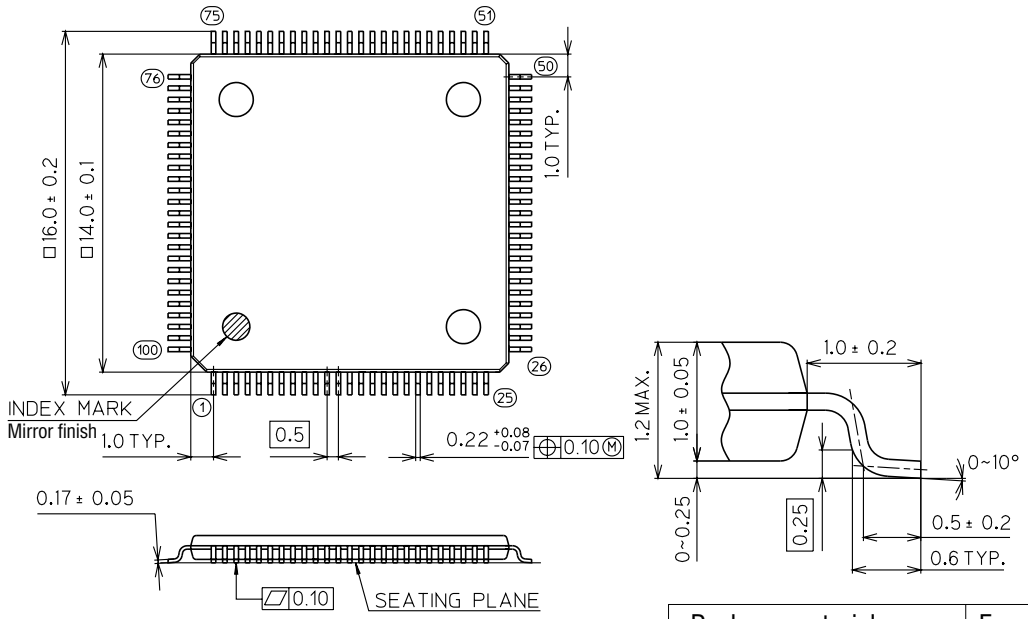
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).