OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM85C154HVS

MSM83C154S Piggy Back

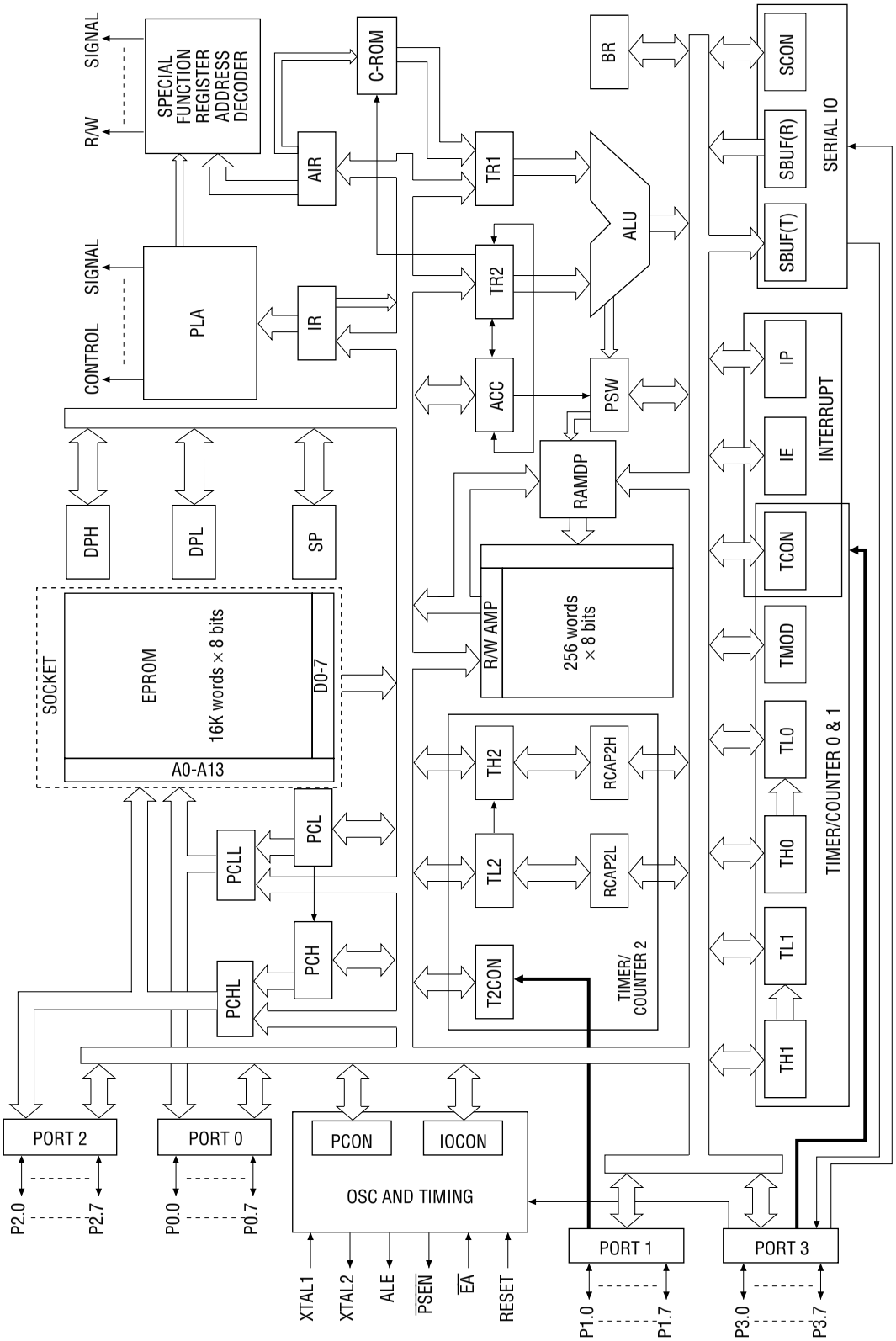
GENERAL DESCRIPTION

The MSM85C154HVS is an 8-bit microcontroller that has been developed assuming that it is used for evaluation of programs of MSM83C154S. ES (Engineering Sample) only.

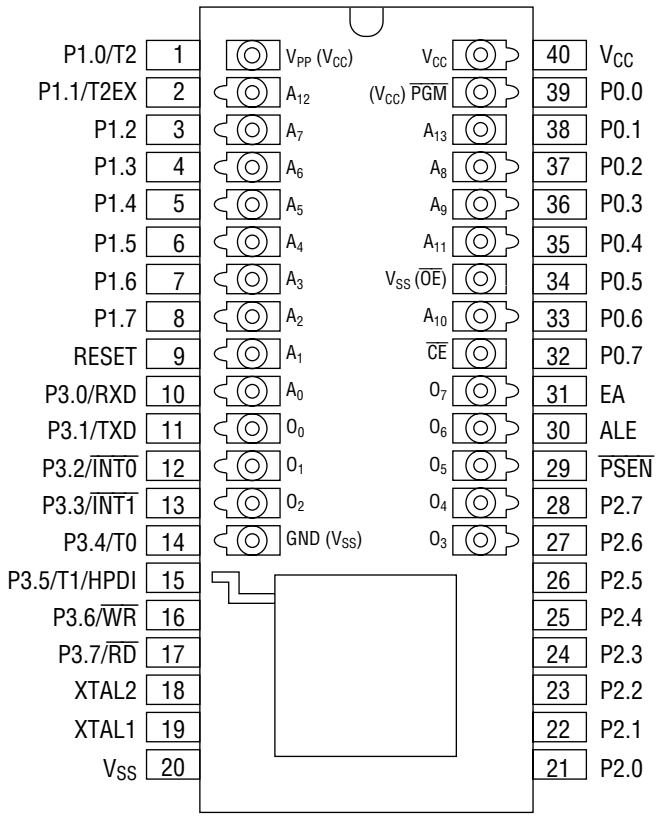
FEATURES

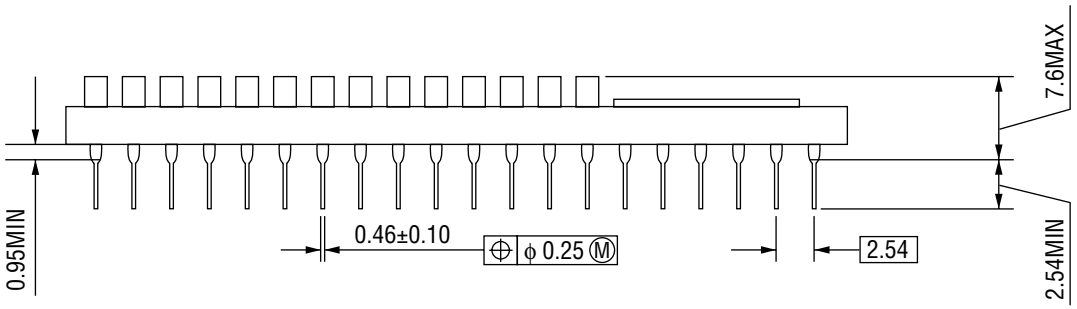
- Operating range
  - Operating frequency : 1 to 22 MHz (16 to 22 MHz is recommended for program development)
  - Operating voltage : 4.75 to 5.25 V (Use MSM85C154VS for 1 to 16 MHz)
  - Operating temperature : Room temperature
- Fully static circuit
- On-chip program memory : 16K × 8-bit ROM (EPROM)
- On-chip data memory : 256 × 8-bit RAM
- External program memory address space : 64 Kbytes
- External data memory address space : 64 Kbytes
- I/O port
  (Port 1, 2, 3, impedance programmable) : 4 ports × 8 bits
- 16-bit timer/counters : 3
- Multifunctional serial port : I/O Expansion mode
  : UART mode (featuring error detection)
- 6-source 2-priority level
  Interrupt and multi-level
  Interrupt available by programming IP and IE registers
- Memory-mapped special function registers
- Bit addressable data memory and SFRs
- Minimum instruction cycle : 545 ns @ 22 MHz operation
- "Multiply"/"divide" instruction cycle : 2.18 µs @ 22 MHz operation
- Standby functions : Power-down mode (oscillator stop)
  Activated by software or hardware; providing ports with floating or active status
  The software power-down stet mode is terminated by interrupt signal enabling execution from the interrupted address.
- Package
  40-pin ceramic Piggyback (ADIP40-C-600-2.54) (Product name: MSM85C154HVS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)





40-Pin Package (Piggy back)

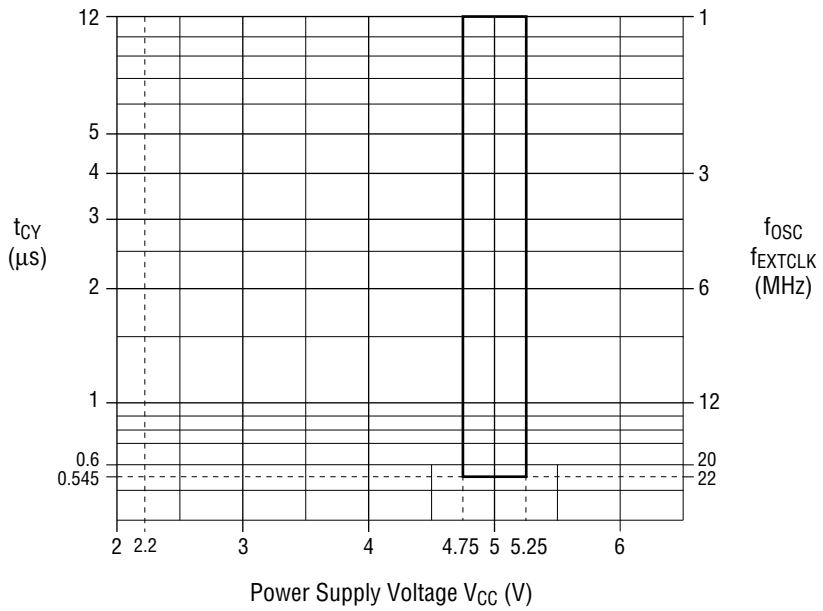
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	Ta=25°C	–0.5 to 7	V
Input Voltage	V_I	Ta=25°C	–0.5 to V_{CC}+0.5	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{CC}	See below.	4.75 to 5.25	V
Oscillation Frequency *1	V_{OSC}	See below.	1 to 22	MHz
External Clock Operating Frequency	f_{EXTCLK}	See below.	0 to 22	MHz
Ambient Temperature	Ta	—	room temp	°C

*1 Depends on the specification for crystal or ceramic resonator.



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC}=4.75 to 5.25V, V_{SS}=0V, Ta=room temp)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input Low Voltage	V_{IL}	—	–0.5	—	0.2 V_{CC}–0.1	V	1
Input High Voltage	V_{IH}	Except XTAL1, $\overline{EA}$, and RESET	0.2 V_{CC}+0.9	—	V_{CC}+0.5	V	
Input High Voltage	V_{IH1}	XTAL1, RESET and $\overline{EA}$	0.7 V_{CC}	—	V_{CC}+0.5	V	
Output Low Voltage (PORT 1, 2, 3)	V_{OL}	I_{OL}=1.6 mA	—	—	0.45	V	
Output Low Voltage (PORT 0, ALE, $\overline{PSEN}$)	V_{OL1}	I_{OL}=3.2 mA	—	—	0.45	V	
Output High Voltage (PORT 1, 2, 3)	V_{OH}	I_{OH}=–60 µA V_{CC}=5 V±10%	2.4	—	—	V	
		I_{OH}=–30 µA	0.75 V_{CC}	—	—	V	
		I_{OH}=–10 µA	0.9 V_{CC}	—	—	V	
Output High Voltage (PORT 0, ALE, $\overline{PSEN}$)	V_{OH1}	I_{OH}=–400 µA V_{CC}=5 V±10%	2.4	—	—	V	
		I_{OH}=–150 µA	0.75 V_{CC}	—	—	V	
		I_{OH}=–40 µA	0.9 V_{CC}	—	—	V	
Logical 0 Input Current/ Logical 1 Output Current/ (PORT 1, 2, 3)	I_{IL} / I_{OH}	V_I=0.45V / V_O=0.45V	–5	–60	–80	µA	2
Logical 1 to 0 Transition Current (PORT 1, 2, 3)	I_{TL}	V_{IL}=2.0V	—	–240	–500	µA	
Input Leakage Current (PORT 0 floating, $\overline{EA}$)	I_{LI}	V_{SS} < V_I < V_{CC}	—	—	±10	µA	3
RESET Pulldown Resistor	R_{RST}	—	20	40	125	kΩ	2
Pin Capacitance	C_{IO}	Ta=25°C, f=1 MHz (except XTAL1)	—	—	10	pF	—
Power Down Current	I_{PD}	—	—	1	50	µA	4

Maximum power supply current normal operation I_{CC} (mA)

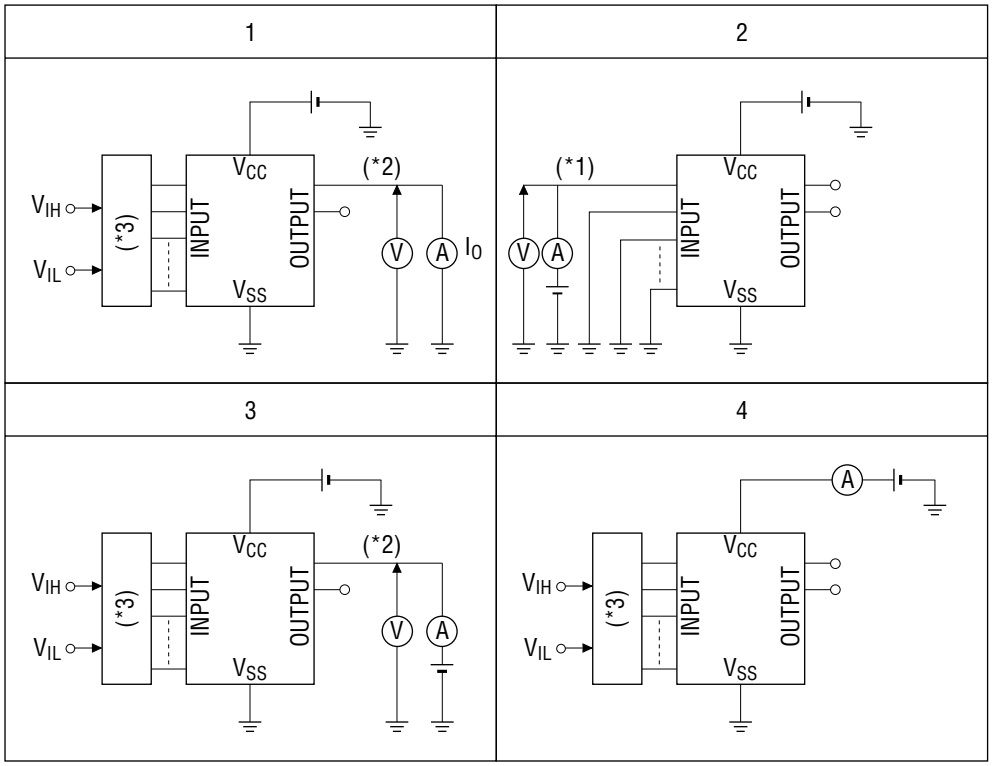
V_{CC}	4.75V	5V	5.25V
Freq			
1 MHz	2.2	3.1	4.1
3 MHz	3.9	5.2	7.0
12 MHz	15.0	16.0	17.0
16 MHz	19.0	20.0	22.0
22 MHz	25.0	27.0	29.0

Maximum power supply current idle mode I_{CC} (mA)

V_{CC}	4.75V	5V	5.25V
Freq			
1 MHz	0.8	1.2	1.6
3 MHz	1.2	1.7	2.3
12 MHz	4.1	4.4	4.8
16 MHz	5.1	5.5	6.0
22 MHz	6.5	7.0	7.5

Note: The values of Power-down current, operating current, and IDLE current do not include the current dissipated by EPROM.

Measuring circuits



*1: Repeated for specified input pins.
*2: Repeated for specified output pins.
*3: Input logic for specified status.

AC Characteristics

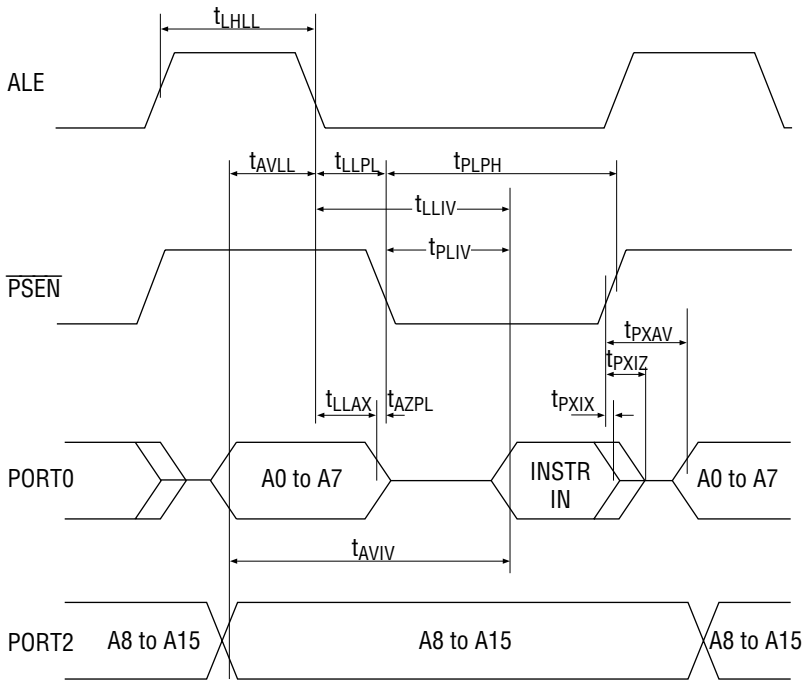
External program memory access AC characteristics

(V_{CC} = 4.75 to 5.25V, V_{SS} = 0V, Ta = room temp
PORT 0, ALE, and $\overline{PSEN}$ connected with 100 pF load, other connected with 80 pF load)

Parameter	Symble	Variable clock from*1 1 to 22 MHz		Unit
		Min.	Max.	
XTAL1, XTAL 2 Oscillation Cycle	t_{CLCL}	45.5	1000	ns
ALE Signal Width	t_{LHLL}	$2t_{CLCL}$-40	—	ns
Address Setup Time (to ALE Falling Edge)	t_{AVLL}	$1t_{CLCL}$-15	—	ns
Address Hold Time (from ALE Falling Edge)	t_{LLAX}	$1t_{CLCL}$-35	—	ns
Instruction Data Read Time (from ALE Falling Edge)	t_{LLPL}	—	$4t_{CLCL}$-100	ns
From ALE Falling Edge to $\overline{PSEN}$ Falling Edge	t_{LLPL}	$1t_{CLCL}$-30	—	ns
$\overline{PSEN}$ Signal Width	t_{PLPH}	$3t_{CLCL}$-35	—	ns
Instruction Data Read Time (from $\overline{PSEN}$ Falling Edge)	t_{PLIV}	—	$3t_{CLCL}$-45	ns
Instruction Data Hold Time (from $\overline{PSEN}$ Rising Edge)	t_{PXIX}	0	—	ns
Bus Floating Time after Instruction Data Read (from $\overline{PSEN}$ Rising Edge)	t_{PXIZ}	—	$1t_{CLCL}$-20	ns
Instruction Data Read Time (from Address Output)	t_{AVIV}	—	$5t_{CLCL}$-105	ns
Bus Floating Time($\overline{PSEN}$ Rising Edge from Address float)	t_{AZPL}	0	—	ns
Address Output Time from $\overline{PSEN}$ Rising Edge	t_{PXAV}	$1t_{CLCL}$-20	—	ns

*1 The variable check is from 0 to 22 MHz when the external check is used.

External program memory read cycle



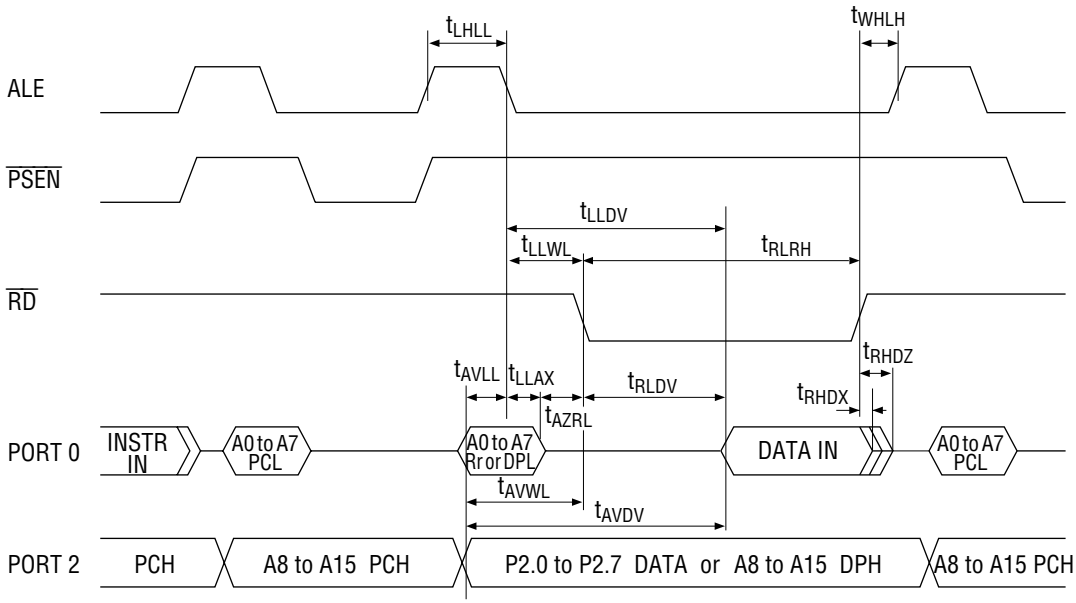
External data memory access AC characteristics

(Vcc = 4.75 to 5.25V, Vss = 0V, Ta = room temp
PORT 0, ALE, and $\overline{PSEN}$ connected with 100 pF load, other connected with 80 pF load)

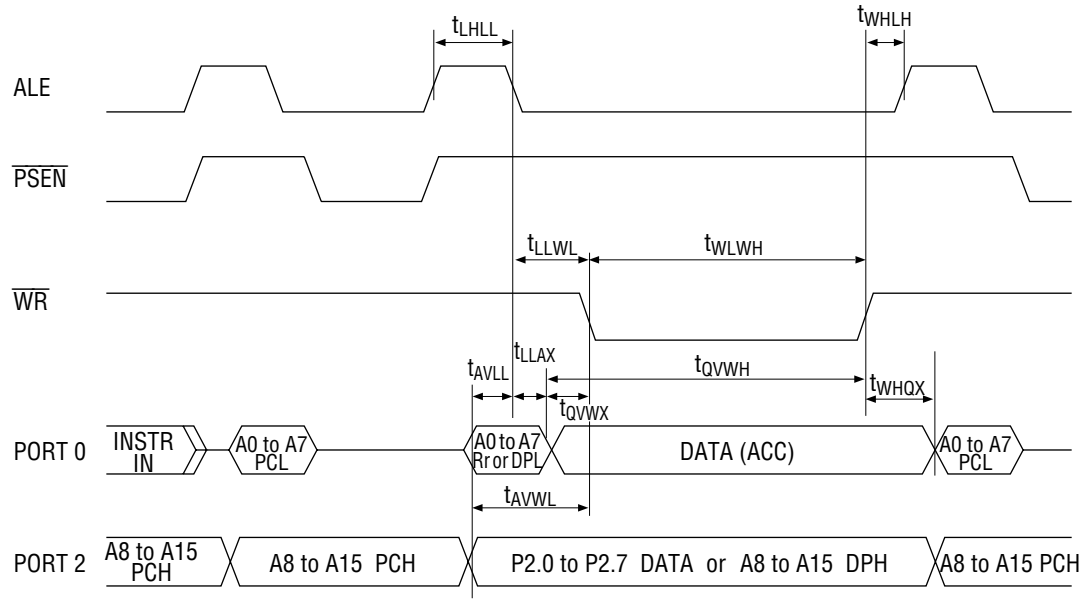
Parameter	Symble	Variable clock from*1 1 to 22 MHz		Unit
		Min.	Max.	
XTAL1, XTAL2 Oscillator Cycle	t_{CLCL}	45.5	1000	ns
ALE Signal Width	t_{LHLL}	$2t_{CLCL}$-40	—	ns
Address Setup Time (to ALE Falling Edge)	t_{AVLL}	$1t_{CLCL}$-15	—	ns
Address Hold Time (from ALE Falling Edge)	t_{LLAX}	$1t_{CLCL}$-35	—	ns
$\overline{RD}$ Signal Width	t_{RLRL}	$6t_{CLCL}$-100	—	ns
$\overline{WR}$ Signal Width	t_{WLWH}	$6t_{CLCL}$-100	—	ns
RAM Data Read Time (from $\overline{RD}$ Signal Falling Edge)	t_{RLDV}	—	$5t_{CLCL}$-105	ns
RAM Data Read Hold Time (from $\overline{RD}$ Signal Rising Edge)	t_{RHDX}	0	—	ns
Data Bus Floating Time (from $\overline{RD}$ Signal Rising Edge)	t_{RHDZ}	—	$2t_{CLCL}$-70	ns
RAM Data Read Time (from ALE Signal Falling Edge)	t_{LLDV}	—	$8t_{CLCL}$-100	ns
RAM Data Read Time (from Address Output)	t_{AVDV}	—	$9t_{CLCL}$-105	ns
$\overline{RD}$/$\overline{WR}$ Output Time from ALE Falling Edge	t_{LLWL}	$3t_{CLCL}$-40	$3t_{CLCL}$+40	ns
$\overline{RD}$/$\overline{WR}$ Output Time from Address Output	t_{AVWL}	$4t_{CLCL}$-70	—	ns
$\overline{WR}$ Output Time from Data Output	t_{QVWX}	$2t_{CLCL}$-40	—	ns
Time from Data to $\overline{WR}$ Rising Edge	t_{QVWH}	$7t_{CLCL}$-105	—	ns
Data Hold Time (from $\overline{WR}$ Rising Edge)	t_{WHQX}	$2t_{CLCL}$-50	—	ns
Time from to Address Float $\overline{RD}$ Output	t_{RLAZ}	0	—	ns
Time from $\overline{RD}$/$\overline{WR}$ Rising Edge to ALE Rising Edge	t_{WHLH}	$1t_{CLCL}$-30	$1t_{CLCL}$+40	ns

*1 The variable check is from 0 to 22 MHz when the external check is used.

External data memory read cycle



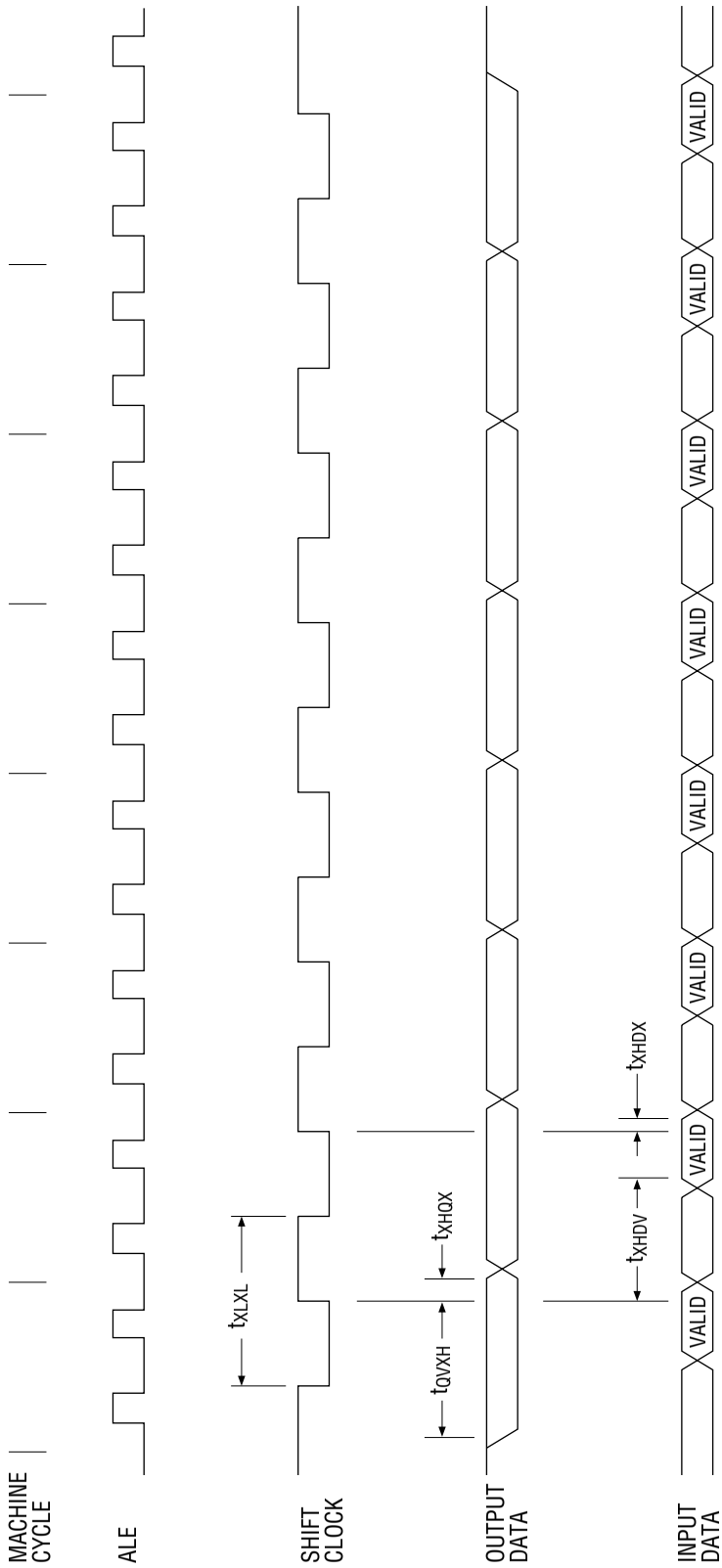
External data memory write cycle



Serial port (I/O extension mode) AC characteristics

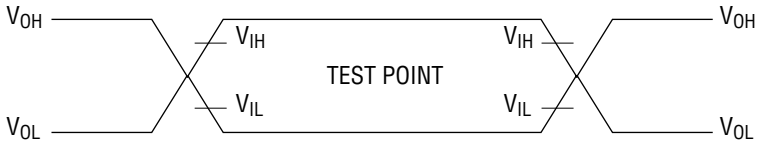
(V_{CC} = 4.75 to 5.25V, V_{SS} = 0V, Ta = room temp)

Parameter	Symbol	Min.	Max.	Unit
Serial Port Clock Cycle Time	t_{XLXL}	$12t_{CLCL}$	—	ns
Output Data Setup to Clock Rising Edge	t_{QVXH}	$10t_{CLCL}$-133	—	ns
Output Data Hold After Clock Rising Edge	t_{XHQX}	$2t_{CLCL}$-75	—	ns
Input Data Hold After Clock Rising Edge	t_{XHDX}	0	—	ns
Clock Rising Edge to Input Data Valid	t_{XHDV}	—	$10t_{CLCL}$-133	ns


MACHINE CYCLE
ALE
SHIFT CLOCK
OUTPUT DATA
INPUT DATA
tXLXL
tQVXH
tXHQX
tXHDV
tXHDX
VALID

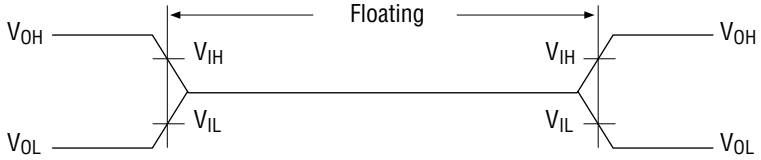
AC characteristics measuring conditions

1. Input/output signal



* The input signals in AC test mode are either V_{OH} (logic "1") or V_{OL} (logic "0") input signals where logic "1" corresponds to a CPU output signal waveform measuring point in excess of V_{IH}, and logic "0" to a point below V_{IL}.

2. Floating

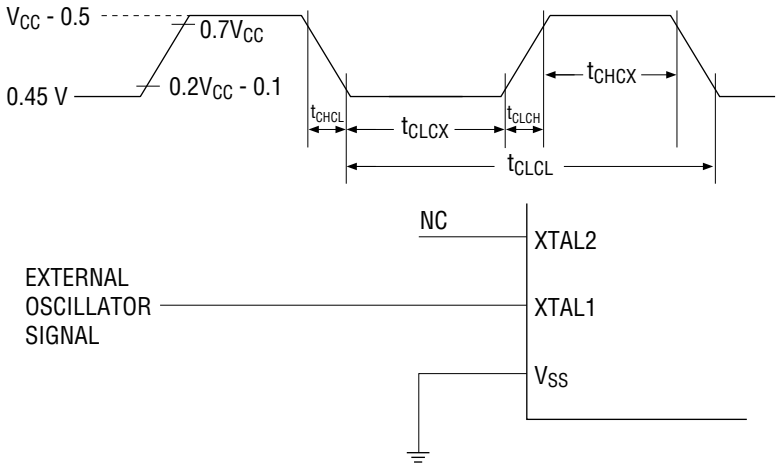


* The port 0 floating interval is measured from the time the port 0 pin voltage drops below V_{IH} after sinking to GND at 2.4 mA when switching to floating status from a "1" output, and from the time the port 0 pin voltage exceeds V_{IL} after connecting to a 400 µA source when switching to floating status from a "0" output.

XTAL1 external clock input waveform conditions

Parameter	Symbol	Min.	Max.	Unit
External Clock Freq.	$1/t_{CLCL}$	0	22	MHz
Clock Pulse width 1	t_{CHCx}	15	—	ns
Clock Pulse width 2	t_{CLCX}	15	—	ns
Rise Time	t_{CLCH}	—	5	ns
Fall Time	t_{CHCL}	—	5	ns

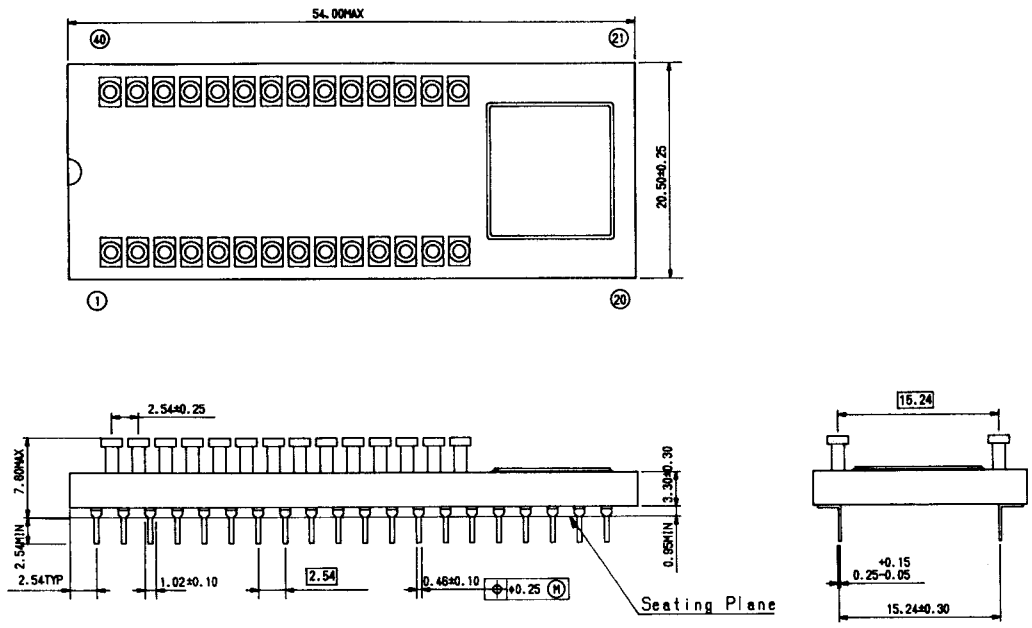
External clock drive waveform



PACKAGE DIMENSIONS

(Unit : mm)

ADIP40-C-600-2.54



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).