OKI semiconductor

MSM5265

160-DOT LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM5265GS is an LCD driver which can directly drive up to 80 segments in the static display mode, while it can directly drive up to 160 segments in the 1/2 duty dynamic display mode.

The MSM5265GS is fabricated by low power CMOS metal gate technology, consisting of 160-stage shift register, 160-bit latch, 80 sets of LCD driver and a common signal generator.

The display data is serially input from the DATA-IN terminal to the 160-stage shift register synchronized with the CLOCK pulse. The data is shifted to the 160-bit latch by the LOAD signal. Then the latched data is directly output to the LCD from the 80 sets of LCD driver as serial output.

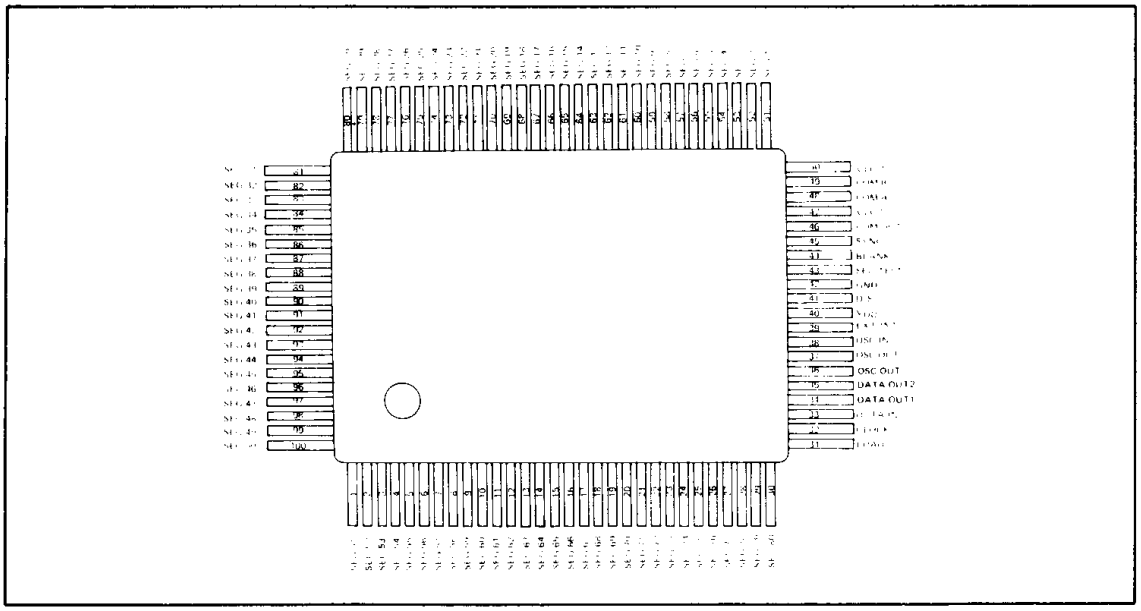
The common signal can be generated by the on-chip generator, or can be externally input. The common synchronization circuit which is used in the dynamic display mode is integrated on the chip.

FEATURES

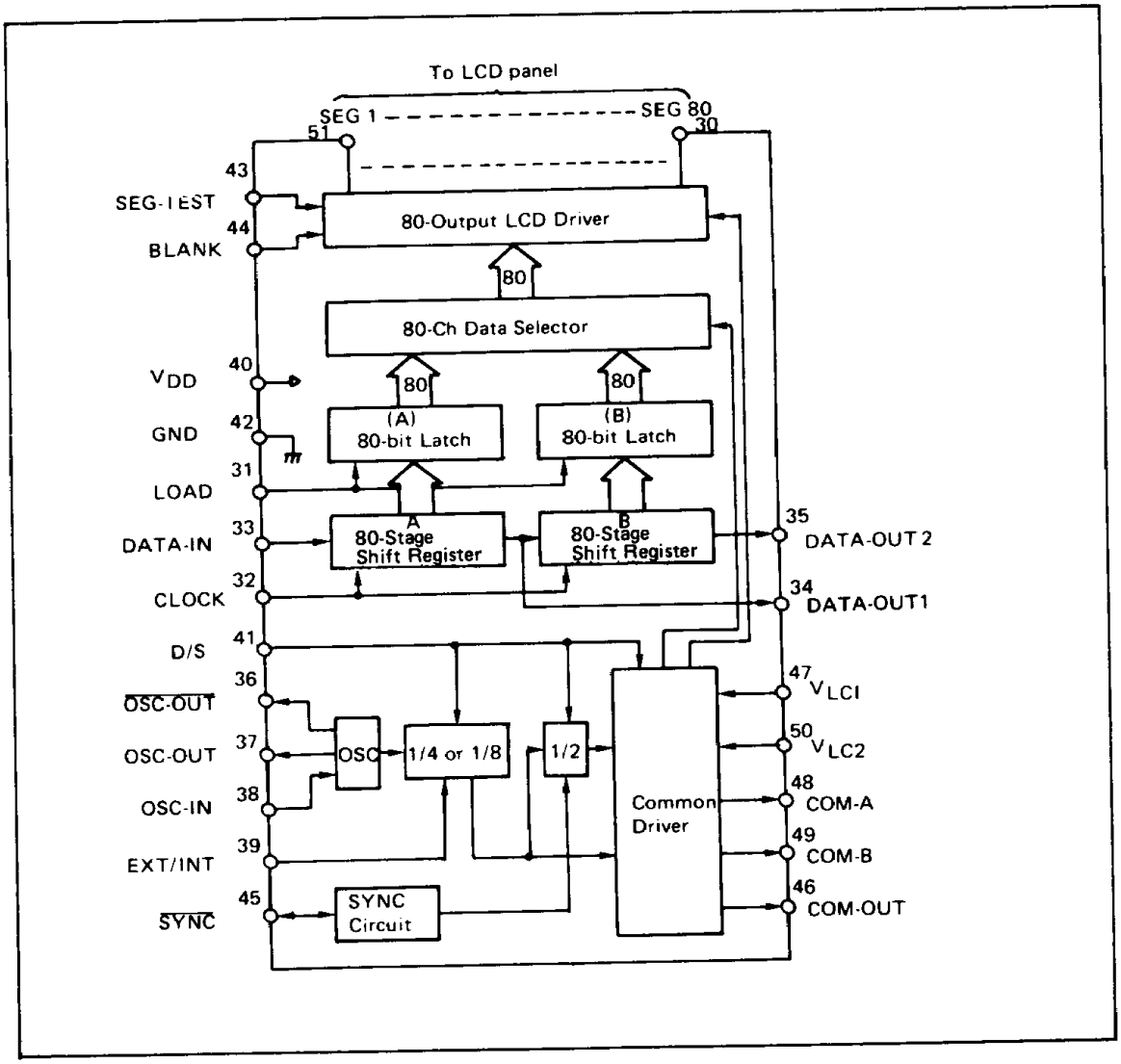
- 80 segments display drive (in the static display mode)
- 160 segments display drive (in the dynamic display mode)
- Simple interface with microcomputer
- Bit-to-bit correspondence between input data and output data
  H : Display L : No display
- Cascade connection capability
- On-chip common signal generator
- Can be synchronized with the external common signal
- Testing terminals for all-on (SEG-TEST) and all-off (BLANK)
- Applicable as an output expander
- LCD driving voltage can be adjusted by the combination of V_{LC1} and V_{LC2}
- Supply voltage: 3.0 ~ 6.0V
- 100 pin plastic QFP (QFP100-P-1420-K)
- 100 pin -VI plastic QFP (QFP100-P-1420-VIK)

PIN CONFIGURATION

(Top view) 100 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

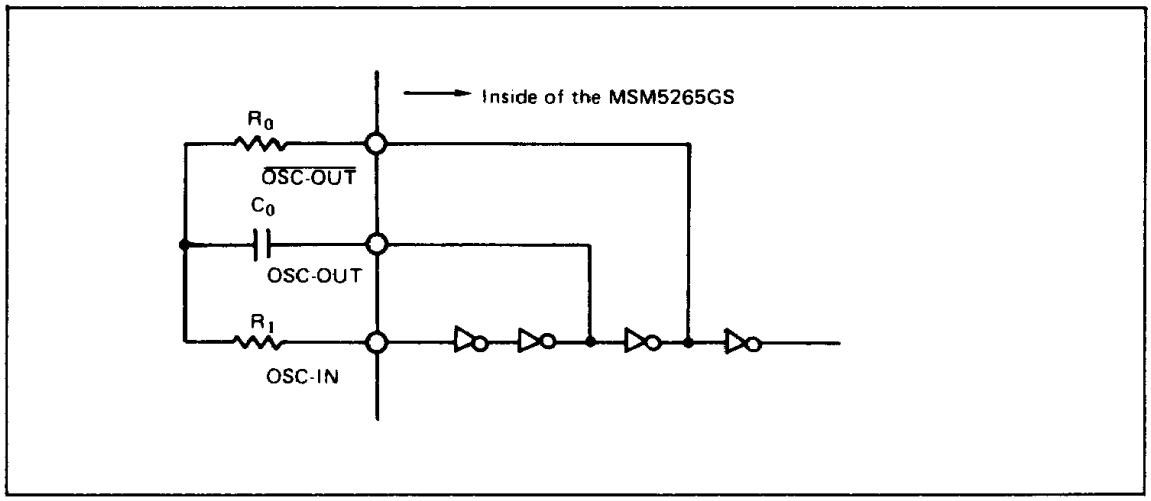
Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	T_a = 25°C	− 0.3 ~ + 6.5	V
Input voltage	V_I	T_a = 25°C	GND − 0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	− 55 ~ + 150	°C

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	V_{DD}	—	3 ~ 6	V
Operating temperature	T_{OP}	—	−40 ~ 85	°C
LCD driving voltage	$V_{DD} - V_{LC2}$	—	3 ~ V_{DD}	V

RECOMMENDING OSCILLATION CIRCUIT CONDITION

Parameter	Symbol	Corresponding pin	Condition	MIN	TYP	MAX	Unit
Oscillator resistance	R_0	36 $\overline{\text{OSC-OUT}}$	—	56	100	220	kΩ
Oscillator capacitance	C_0	37 OSC-OUT	Film capacitor	0.001	–	0.047	μF
Current limiter resistance	R_1	38 OSC-IN	$R_1 \geqq 10\,R_0$	0.56	1	2.2	MΩ
Common signal frequency	f_{COM}	48 COM-A 49' COM-B	—	25	–	150	Hz



D.C. CHARACTERISTICS

(V_{DD} = 5.0V T_a = −40 ~ +85°C)

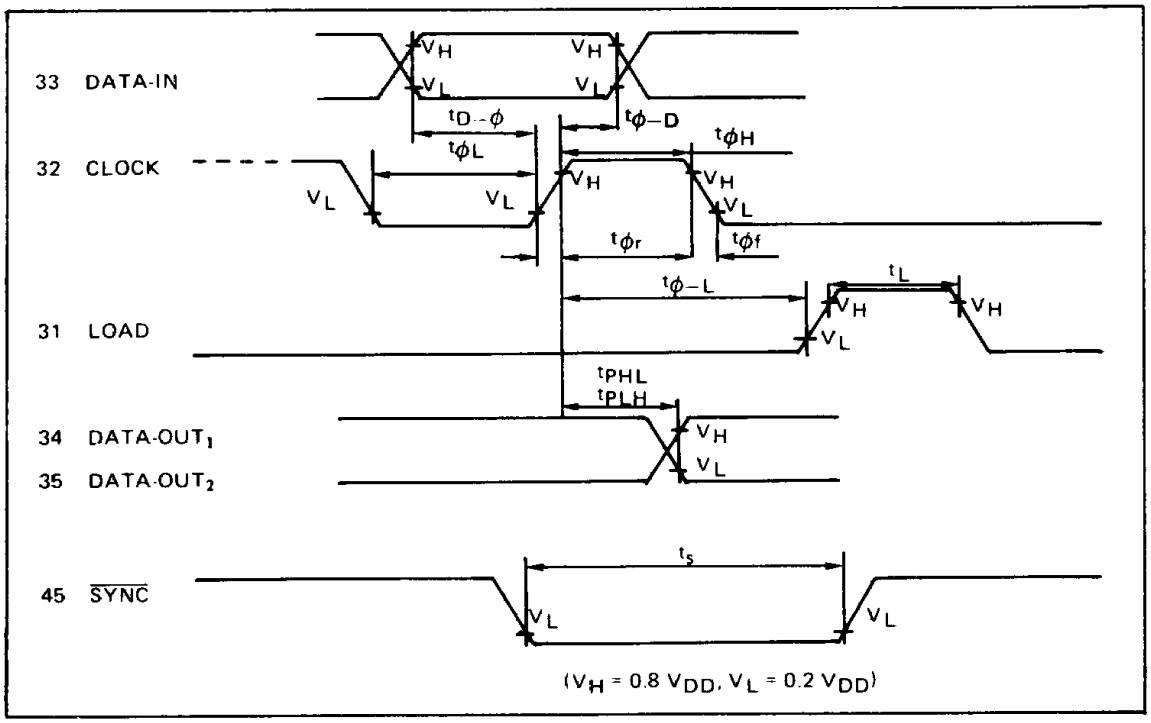
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable pin
"H" Input voltage	V_{IH}	—	3.6	–	–	V	SEG-TEST, BLANK, LOAD, DATA-IN, CLOCK, D/S, EXT/INT, OSC-IN
"L" Input voltage	V_{IL}	—	–	–	1.0	V	
Input leakage current	I_{IL}	V_I = 5.0V/0V	–	–	±1	μA	
"H" Output voltage	V_{OH}	I_O = −100μA	4.5	–	–	V	DATA-OUT1 DATA-OUT2 COM-OUT
		I_O = −200μA	4.5	–	–	V	OSC-OUT $\overline{\text{OSC-OUT}}$
		V_{LC1} = 2.5V V_{LC2} = 0V I_O = −30μA	4.8	–	–	V	SEG1 ~ SEG80
		V_{LC1} = 2.5V V_{LC2} = 0V I_O = 150μA	4.8	–	–	V	COM-A COM-B
"M" Output voltage	V_{OM}	V_{LC1} = 2.5V V_{LC2} = 0V I_O = ±150μA	2.3	–	2.7	V	COM-A COM-B
"L" Output voltage	V_{OL}	I_O = 100μA	–	–	0.5	V	DATA-OUT1 DATA—OUT2 COM-OUT
		I_O = 200μA	–	–	0.5	V	OSC-OUT $\overline{\text{OCS-OUT}}$
		V_{LC1} = 2.5V V_{LC2} = 0V I_O = 30μA	–	–	0.2	V	SEG1 ~ SEG80
		V_{LC1} = 2.5V V_{LC2} = 0V I_O = 150μA	–	–	0.2	V	COM-A COM-B
		I_O = 250μA	–	–	0.8	V	$\overline{\text{SYNC}}$
Output leakage current	I_{LO}	V_O = 5V when internal Tr is off	–	–	5	μA	$\overline{\text{SYNC}}$
Segment output impedance	R_{SEG}	V_{LC1} = (5 + V_{LC2})/2 V_{LC2} = 0 ~ 2V	–	–	10	kΩ	SEG1 ~ SEG80

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Applicable Pin
Common output impedance	R_{COM}	$V_{LC1} = (5 + V_{LC2})/2$ $V_{LC2} = 0 \sim 2V$	–	–	1.5	kΩ	COM-A COM-B
Static mode consumption current	I_{DD1}	Set all input level either "H" or "L"			100	μA	V_{DD}
Dynamic mode consumption current	I_{DD2}	No load oscillation. R_0 = 100 kΩ, C_0 = 0.01 μF, R_1 = 1MΩ		0.12	0.5	mA	

SWITCHING CHARACTERISTICS

(V_{DD} = 3.0 ~ 6.0V T_a = −40 ~ +85°C)

Parameter	Symbol	Condition	MIN	MAX	Unit	Applicable Pin
Maximum clock frequency	$f_{\phi MAX}$	—	1	–	MHz	CLOCK
Clock "H" time	$t_{\phi H}$	—	0.3	–	μs	
Clock "L" time	$t_{\phi L}$	—	0.5	—	μs	
Data setup time	$t_{D-\phi}$	—	0.1	–	μs	DATA—IN CLOCK
Data hold time	$t_{\phi-D}$	—	0.1	–	μs	
"H", "L" propagation delay time	t_{PHL} t_{PLH}	When 15PF output capacitors are locaded [34] and [35].	–	0.8	μs	DATA-OUT1 DATA-OUT2 CLOCK
LOAD "H" time width	t_L	—	0.2	–	μs	LOAD
CLOCK → LOAD time	$t_{\phi-L}$	—	0.1	–	μs	CLOCK LOAD
OSC-IN Maximum input frequency	f_{OSCMAX}	—	5	–	kHz	OSC-IN
$\overline{SYNC}$ "L" time width	t_s	—	0.2	–	μs	$\overline{SYNC}$

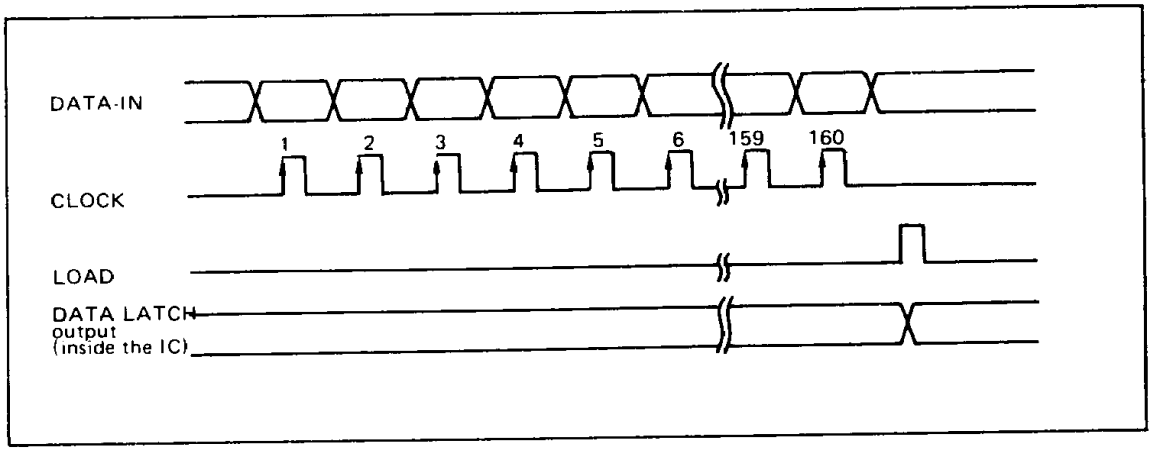


(V_H = 0.8 V_{DD}, V_L = 0.2 V_{DD})

FUNCTIONAL DESCRIPTION

- **Operational description**

The MSM5265GS consists of 160-stage shift register, 160-bit latch, and 80 sets of LCD driver. The display data is input from the DATA-IN terminal to the 160-stage shift register at the rising edge of the CLOCK pulse and it is shifted to the 160-bit latch when the LOAD signal is set at "H" level, then it is directly output to the LCD panel from the 80 sets of LCD driver.



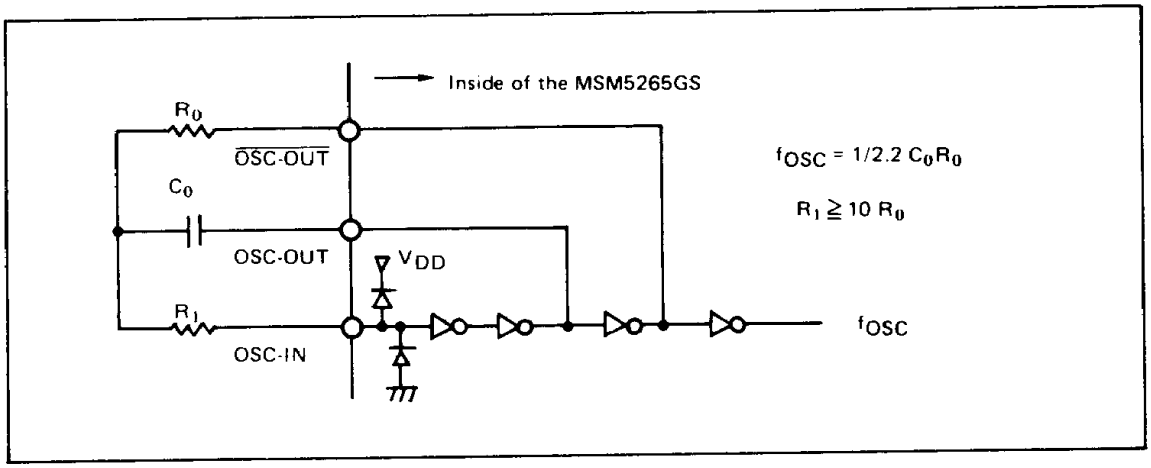
- **OSC-IN, OSC-OUT, $\overline{\text{OSC-OUT}}$**

By connecting the external resistors R_0, R_1 and external capacitor C_1 with OSC-IN, OSC-OUT and $\overline{\text{OSC-OUT}}$ respectively as shown in the figure below, an oscillating circuit to generate the common signal is formed.

This frequency is divided into either 1/8 or 1/4 by the internal dividing circuit. The 1/8 divided frequency is used in the static display mode, while the 1/4 divided frequency is used as the common signal in the dynamic display mode which is output from the COM-OUT terminal. (EXT/INT should be set at low level.)

The resistor R_1 is to limit the current on the OSC-IN terminal's protecting diodes. The value of the R_1 should be 10 times more than that of R_0.

When the external common signal is used, the EXT/INT terminal should be set at high level and the external common signal should be input from the OSC-IN terminal.



- **D/S**
  When this pin is set at high level, the MSM5265GS operates in the dynamic display mode, while it operates in the static display mode when this pin is set at low level.

- **EXT/INT**
  When the external common signal is used, this pin should be set at high level and the external common signal is to be input from the OSC-IN terminal. The input common signal is used same as the internal common signal and is output from the COM-OUT pin through the buffer.
  When the on-chip common signal generator is used, this pin should be set at low level.
  When the MSM5265GS is used as an output expander, this pin should be set at high level and the OSC-IN pin should be set at low level.

- **COM-OUT**
  When more than two MSM5265GSs are connected in a series (cascade connection), this pin should be connected with all of the slave MSM5265GS's OSC-IN terminal.

- **$\overline{\text{SYNC}}$**
  This pin is an input/output pin which is used when more than two MSM5265GSs are used in a series (cascade connection) in the dynamic display mode. All of the involved MSM5265GS's $\overline{\text{SYNC}}$ pins should be connected in a same line so that they should be pulled up by the common resistor, which makes phase level of all involved MSM5265GS's COM-A terminals and COM-B terminals equal. When single MSM5265GS is used in the dynamic display mode, $\overline{\text{SYNC}}$ should be pulled up by the resistor.
  In the static display mode including single MSM5265GS's operation, cascade connection and output expander operation, this pin should be set at ground level.

- **DATA-IN, CLOCK**
  The display data is serially input from the DATA-IN terminal to the 160-stage shift register at the rising edge of the CLOCK pulse. The high level of the display data is used to turn the display on, while low level of the display data is used to turn off the display.

- **DATA-OUT$_1$**
  The 80th stage of the shift register contents is output from this pin.
  When more than two MSM5265GSs are connected in a series (cascade connection) in the static display mode, this pin should be connected to the next MSM5265GS's DATA-IN terminal.

- **DATA-OUT$_2$**
  The 160th stage of the shift register contents is output from this pin.
  When more than two MSM5265GSs are connected in a series (cascade connection) in the dynamic display mode, this pin should be connected to the next MSM5265GS's DATA-IN terminal.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at high level, the shift register contents is shifted to the 80 sets of the LCD driver. When this pin is set at low level, the last display data, which was transferred to the 80 sets of LCD driver when LOAD pin was set at high level, is held.

- **V_{LC2}**
  Supply voltage pin for the 80 sets of LCD driver. The input level to this pin should be the low level output voltage of segment output (SEG1 ~SEG80) and common output (COM-A, COM-B).
  In this case, the high level of segment output and common output is V_{DD} level, while low level of segment output and common output is V_{LC2} level. V_{LC2} should be set at more than ground level.

- **V_{LC1}**
  Supply voltage pin for the middle level voltage of the common output. The input level of this pin is the middle level output voltage of the common output (COM-A, COM-B) in the dynamic display mode.
  The value of the V_{LC1} is calculated by the following formula.

$$V_{LC1} = (V_{DD} + V_{LC2})/2$$

  In the static display mode, this pin should be set at open level.

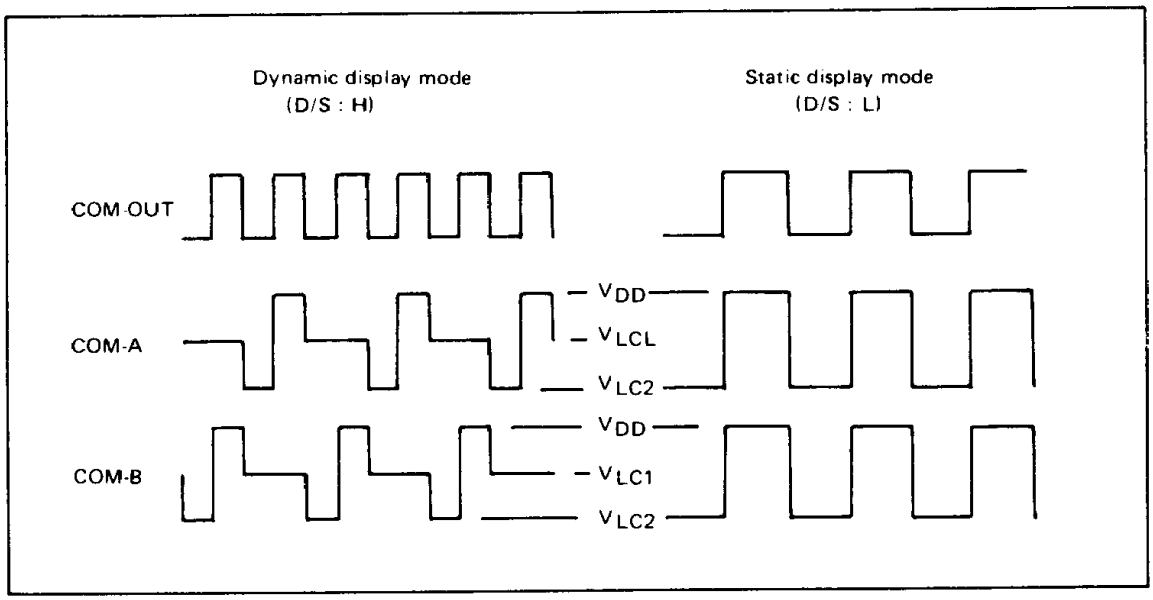
- **COM-A, COM-B**

  LCD driving common signal is output from these pins and these pins should be connected to the common side of the LCD panel.

  – In the static display mode
  Same phase pulse as COM-OUT terminal is output from both of COM-A and COM-B. In this case high level is V_{DD} level and low level is V_{LC2} level.

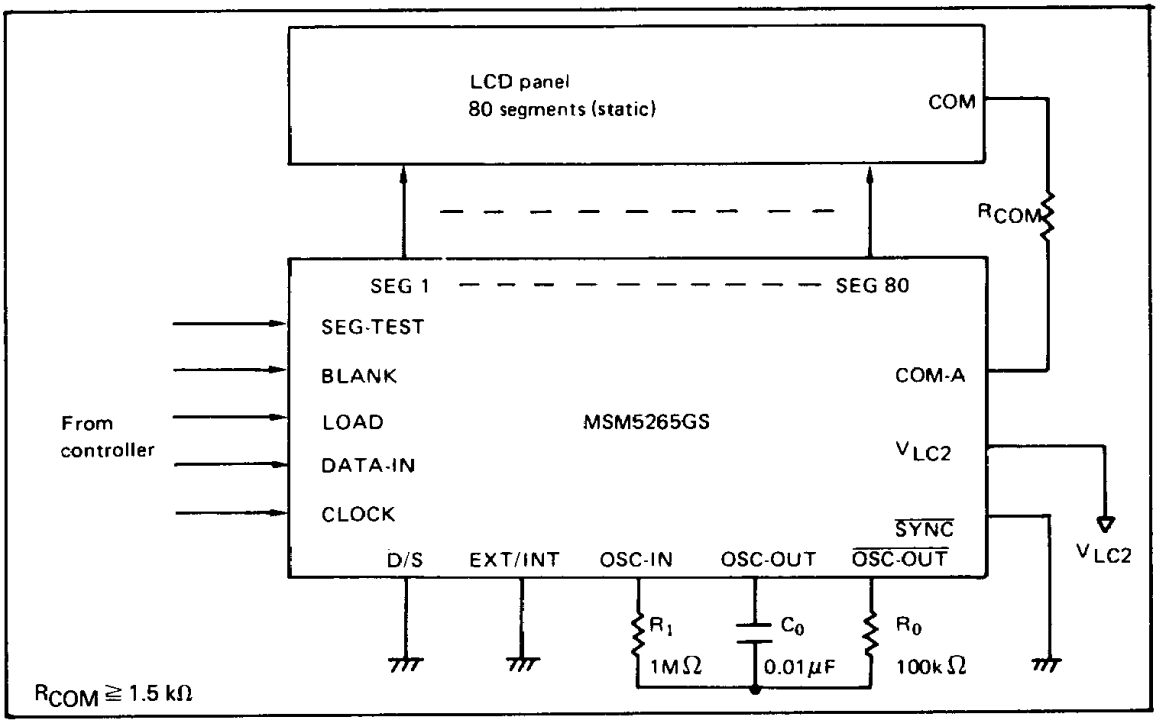
  – In the dynamic display mode
  The COM-A and COM-B output signal are alternately changed within each COM-OUT output cycle, resulting in alternately repetition of select and non-select modes.

  In the select mode the, same phase level as the COM-OUT signal is output.
  In this case, V_{DD} or V_{LC2} is output at high level or low level respectively. In the non-select mode, V_{LC1} is output at the middle level. In the select mode of COM-A (non-select mode of COM-B), the 1st ~80th latched data contents are output from the 80 sets of LCD driver to the LCD panel.
  In the select mode of COM-B (non-select mode of COM-A), the 81st ~ 160th latched data contents are output from the 80 sets of LCD driver to the LCD panel.

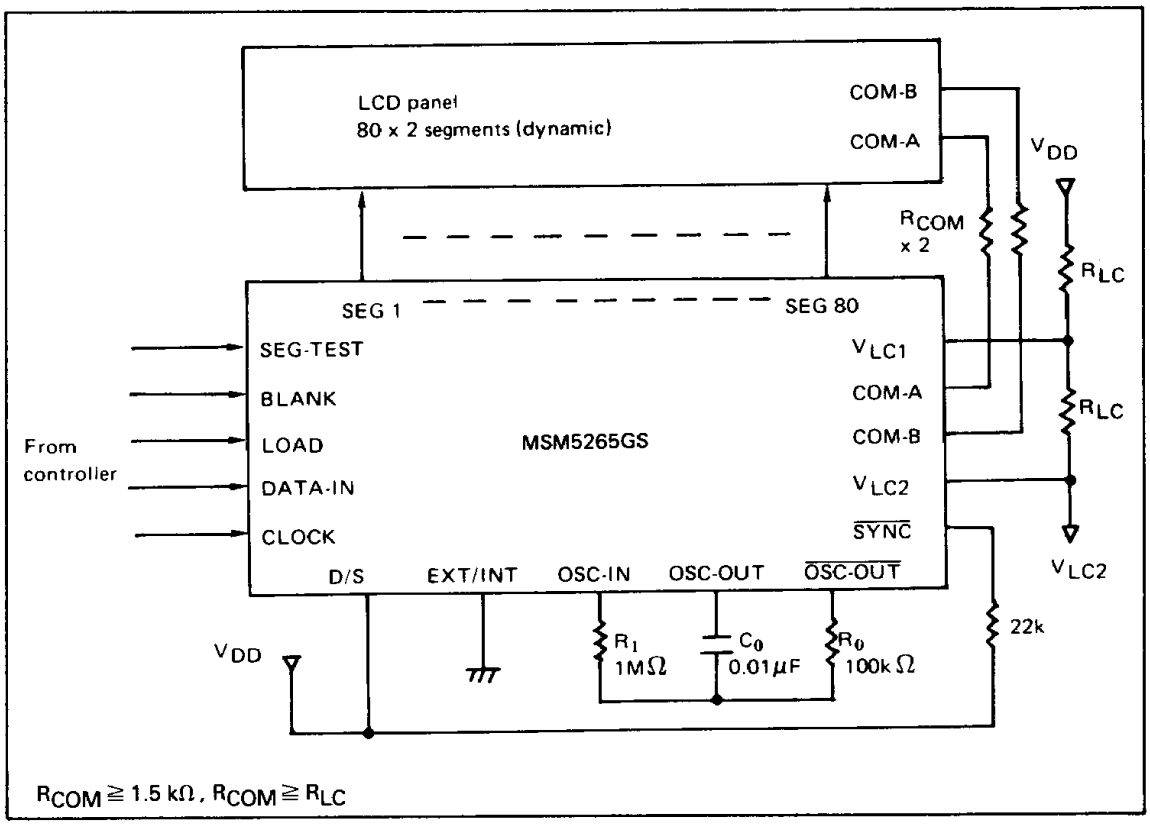


APPLICATION CIRCUIT

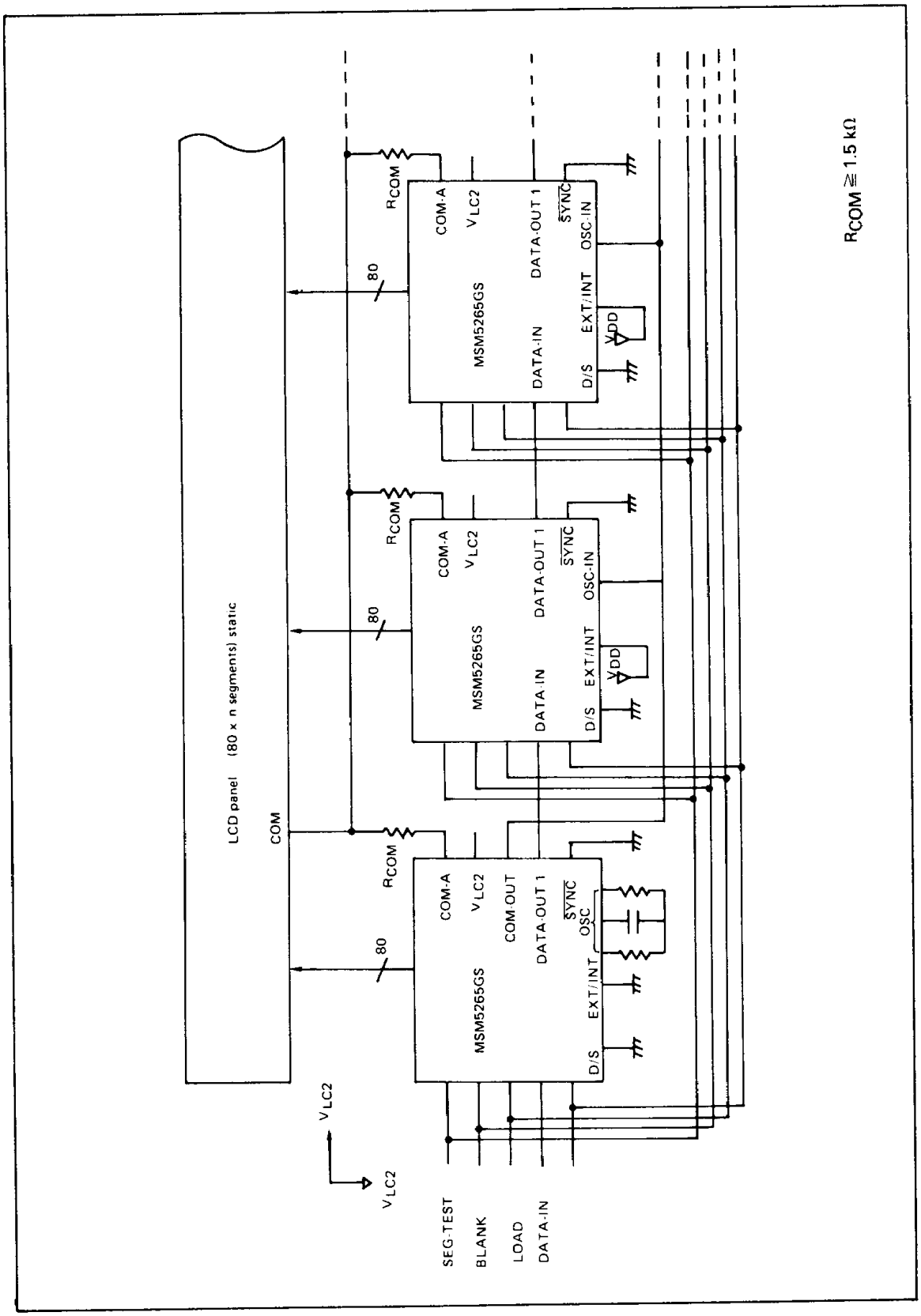
1) Single MSM5265GS operation in the static display mode.



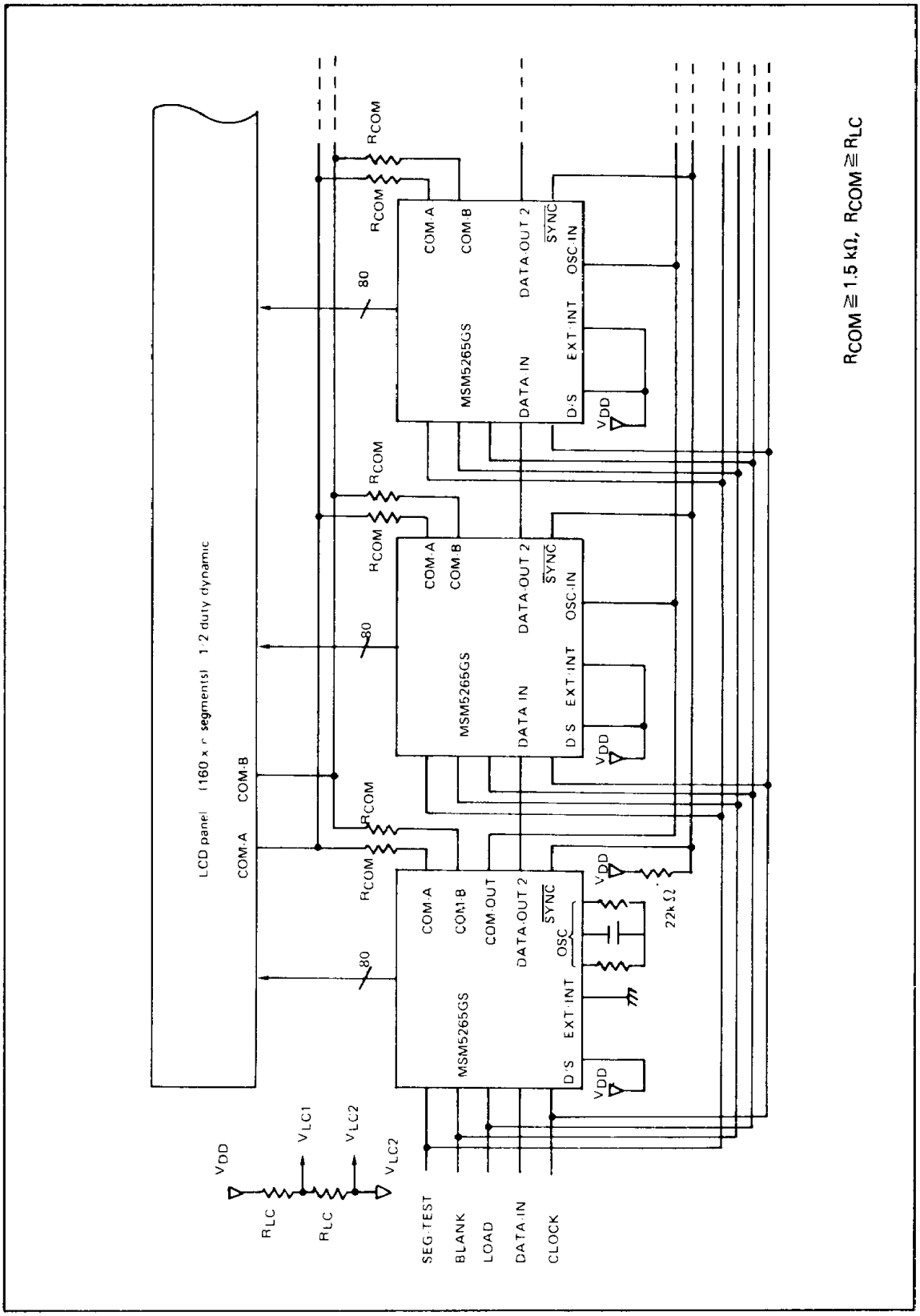
2) Single MSM5265GS operation in the dynamic display mode.



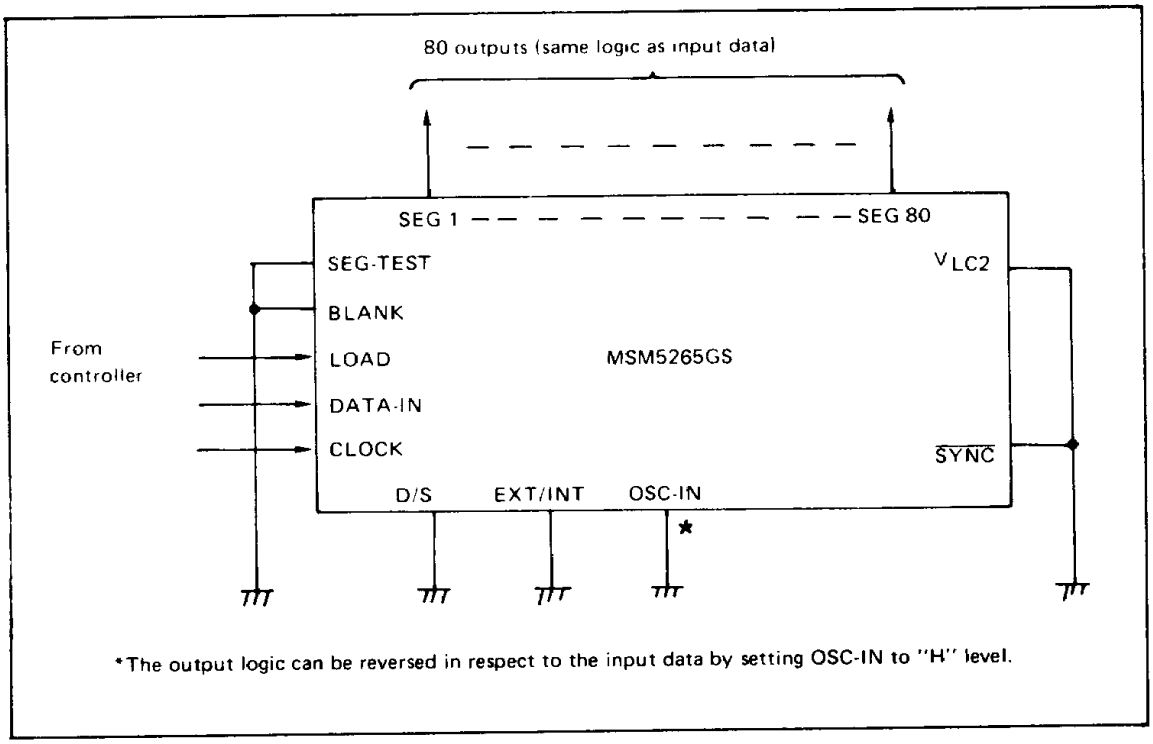
3) Cascade connection of MSM5265GSs in the static display mode.



4) Cascade connection of MSM5265GSs in the dynamic display mode.



5) Output-expander



*The output logic can be reversed in respect to the input data by setting OSC-IN to "H" level.