OKI semiconductor

MSM5260

DOT MATRIX LCD 80 DOT COMMON/SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM5260 is a dot matrix common/segment LCD driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 80-bit shift register, 80-bit data latch, 80-bit level shifter and 80-bit 4-level driver.

It converts serial data, which is received from LCD controller LSI, to parallel data and outputs LCD driving waveform to LCD.

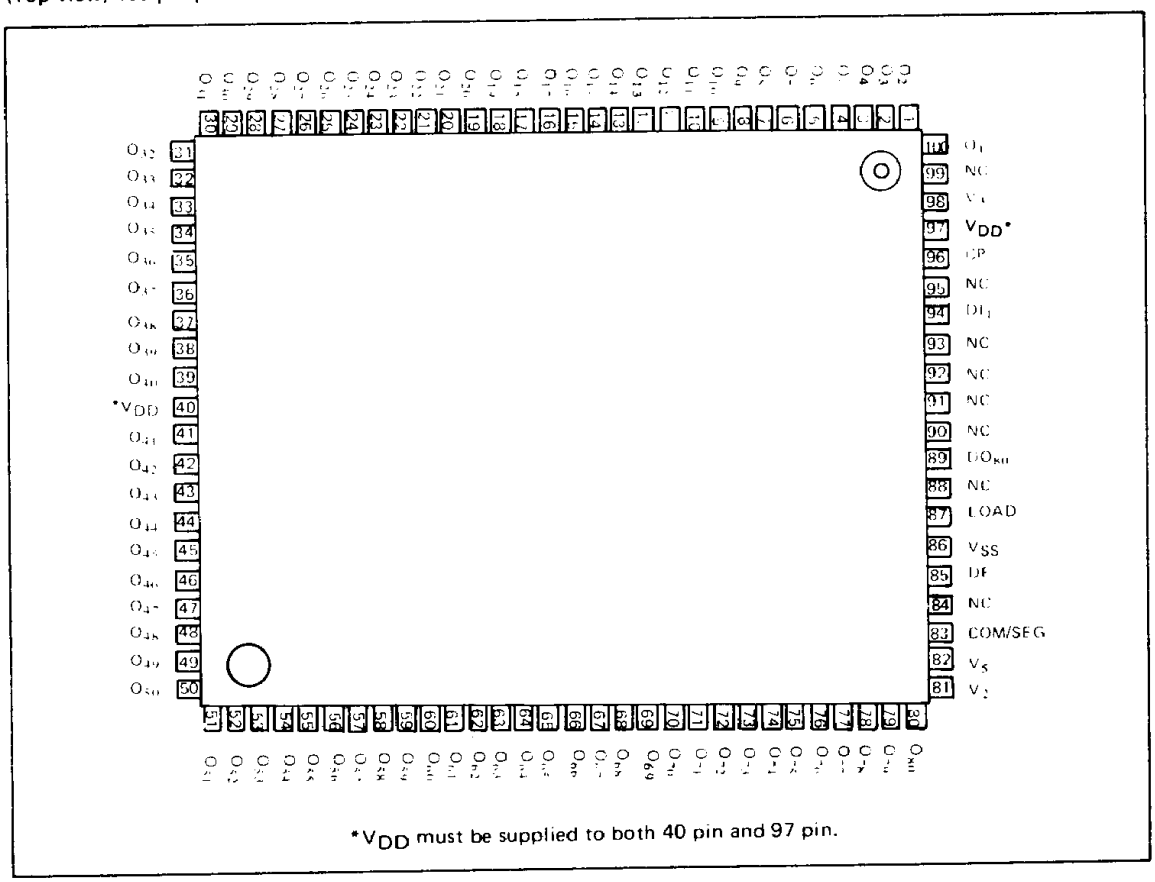
This LSI can drive a variety of LCD pannel because the bias voltage can be optionally provided from the external source.

FEATURES

- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 18V
- Duty 1/16 ~ 1/64
- Bias voltage can be supplied externally
- Can be used either as common driver or segment driver
- Interface with MSM6240GS LCD controller LSI
- 100 pin plastic QFP (QFP100-P-1420-K)
- 100 pin plastic QFP (QFP100-P-1420-L)
- 100 pin -VI plastic QFP (QFP100-P-1420-VIK)

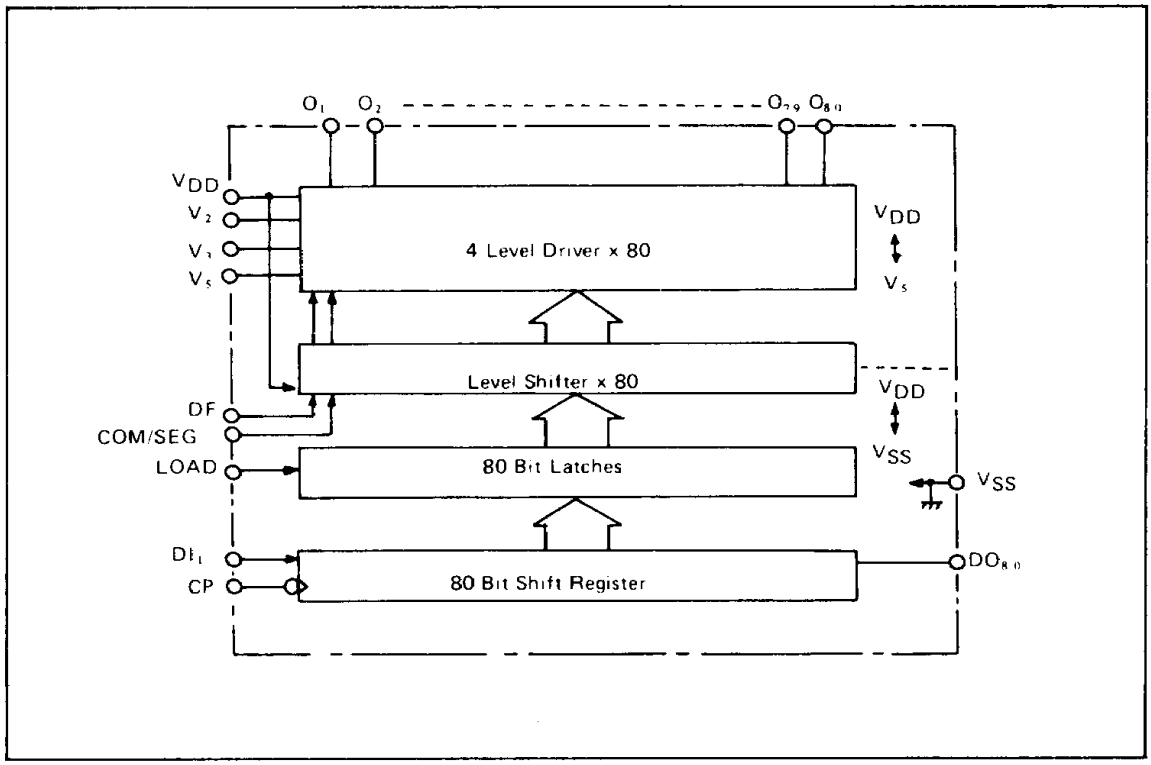
PIN CONFIGURATION

(Top view) 100 pin plastic QFP



*V_{DD} must be supplied to both 40 pin and 97 pin.

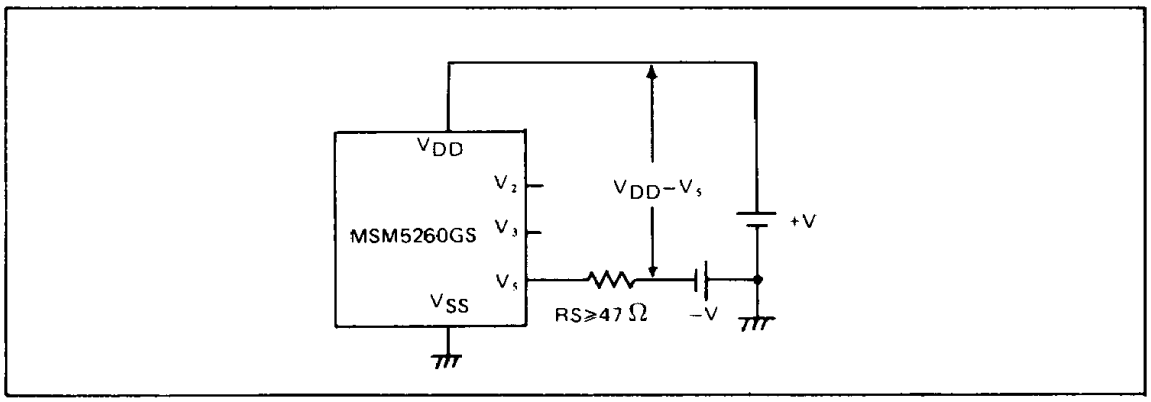
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage (1)	V_{DD}	Ta = 25°C	−0.3 ~ 6	V
Supply Voltage (2)	$V_{DD} - V_5$ *1 $V_{DD} - V_5$ *2	Ta = 25°C Ta = 25°C	0 ~ 18 0 ~ 20	V V
Input Voltage	V_I	Ta = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage Temperature	V_{stg}	—	−55 ~ +150	°C

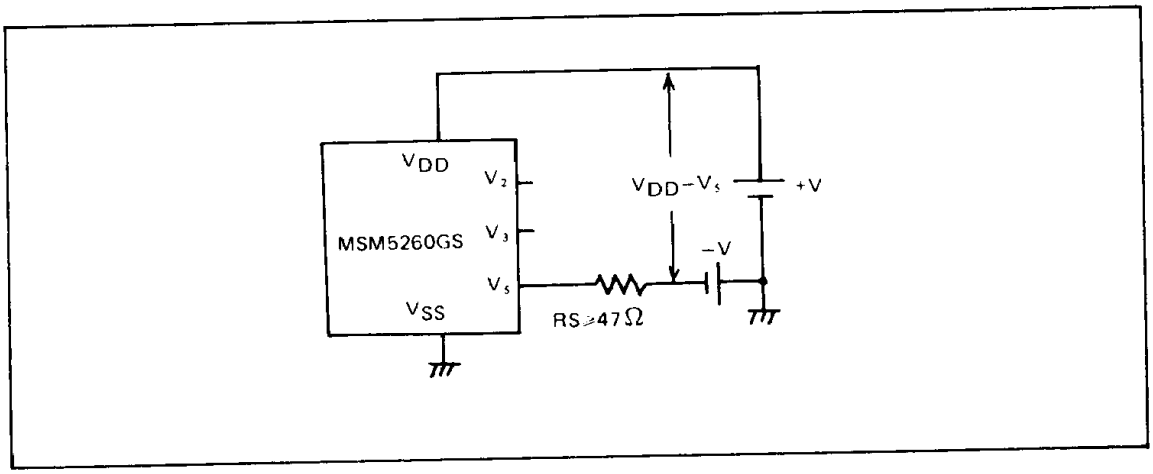
*1 : $V_{DD} > V_2 > V_3 > V_5$
*2 : When a series resistance of more than 47Ω is connected as shown below:



OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage (1)*1	V_{DD}	—	4.5 ~ 5.5	V
Supply Voltage (2)*1 *2	$V_{DD} - V_5$*1	—	8 ~ 16	V
	$V_{DD} - V_5$*2	—	8 ~ 18	V
Operating Temperature	Top	—	−20 ~ +85	°C

*1 : $V_{DD} > V_2 > V_3 > V_5$
*2 : When a series resistance of more than 47Ω is connected as shown below:



D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10% T_a = −20 ~ +85°C)

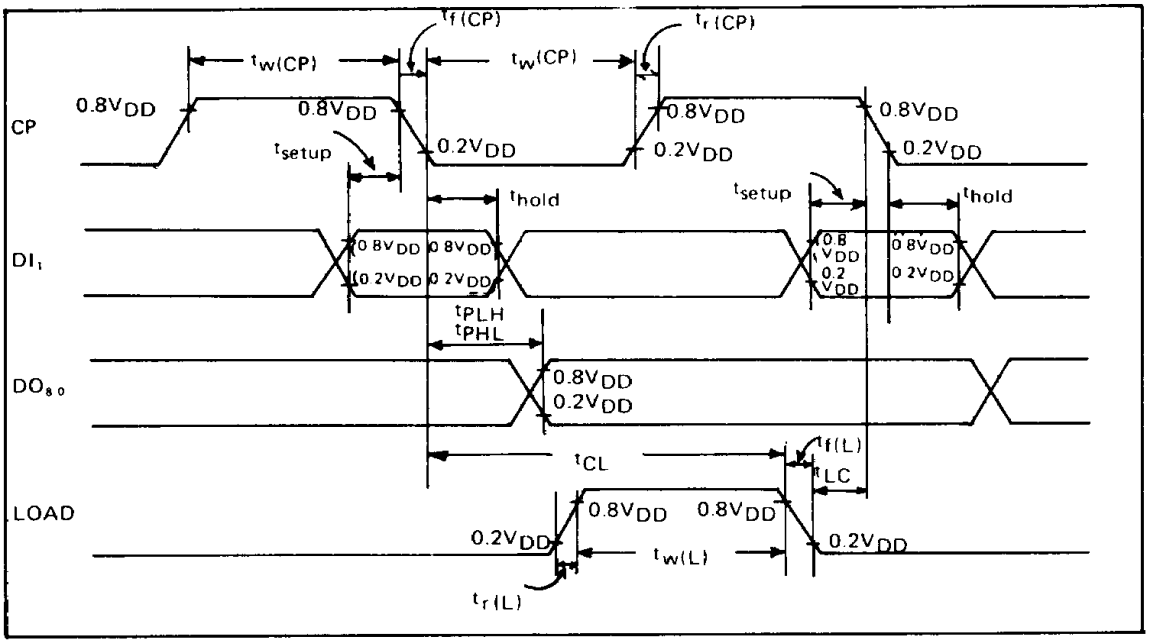
Parameter	Symbol	Condition	Limits			Unit
			MIN	TYP	MAX	
"H" Input Voltage	V_{IH}*1		0.8V_{DD}	–	–	V
"L" Input Voltage	V_{IL}*1		–	–	0.2V_{DD}	V
"H" Input Current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" Input Current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" Output Voltage	V_{OH}*2	I_O = −0.4 mA	V_{DD} − 0.4	–	–	V
"L" Output Voltage	V_{OL}*2	I_O = 0.4 mA	–	–	0.4	V
ON Resistance	R_{ON}*4	$V_{DD} - V_5$ = 10V $\lvert V_N - V_O \rvert$ = 0.25V*3	–	–	2	kΩ
Supply Current	I_{DD}	CP = DC $V_{DD} - V_5$ = 18V No load	–	–	100	μA

*1 Applicable to LOAD, CP, DT_1, DF and COM/SEG pins.
*2 DO_{80}
*3 $V_N = V_{DD} \sim V_5$ V_2 = 8/9 ($V_{DD} - V_5$) V_3 = 1/9 ($V_{DD} - V_5$)
*4 Applicable to $O_1 \sim O_{80}$ display data output pin.

SWITCHING CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = 20 ~ 85°C. CL = 15pF)

Parameter	Symbol	Condition	Limits			Unit
			MIN	TYP	MAX	
"H", "L" Propagation Delay Time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. Clock Frequency	f_{CP}	Duty = 50%	3.3	–	–	MHz
Clock Pulse Width	$t_{W(CP)}$	—	125	–	–	ns
LOAD Pulse Width	$t_{W(L)}$	—	125	–	–	ns
Data Set-up Time $D_I \rightarrow$CP	t_{setup}	—	50	–	–	ns
CP → LOAD Time	t_{CL}	—	250	–	–	ns
LOAD → CP Time	t_{LC}	—	0	–	–	ns
Data Hold Time DI → CP	t_{hold}	—	50	–	–	ns
CP Rising/Falling Time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns
LOAD Rising/Falling Time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs



PIN DESCRIPTION

- **DI_1**
  The date from the LCD controller LSI is input to 80-bit shift register from DI_1. (Positive logic)

- **CP**
  Clock pulse input pin for 80-bit shift register. The data is shifted to 80-bit latch at the falling edge of the clock pulse. A data set up time (t_{setup}) and a data hold time (t_{hold}) are required between a DI_1 signal and a clock pulse.
  Clock pulse rising time (t_r) and clock pulse falling time (t_f) should be maximum 50 ns respectively.

- **DO_{80}**
  80th bit of the shift register contents is output from DO_{80}. The data which was input from DI_1 is output from this pin with 80 bits' delay, synchronized with the clock pulse. By connecting DO_{80} with next MSM5260GS's DI_1, this LSI is applicable to a wide screen LCD. Refer to the application circuit.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H" level, the shift register contents are transferred to 80-bit 4-level driver through 80-bit level shifter.
  When LOAD pin is set at low level, the last display output data ($O_1 \sim O_{80}$), which was transferred when LOAD pin was at high level, is held.

- **DF**
  Alternate signal input pin for LCD driving.

- **COM/SEG**
  Selection signal input pin. MSM5260GS is used either as common driver or segment driver according to input signal level at COM/SEG pin.
  When this pin is set at high level, MSM5260 is used as a common driver, while it is used as a row driver at low level.

The display driving data $O_1 \sim O_{80}$, which are determined according to the combination of latched data and DF signal, are shown in the Table 1 below.

COM/SEG	Latched data level	DF	Display data output level ($O_1 \sim O_{80}$)	Note
H	High (Selected)	H	V_{DD}	Common driver
		L	V_5	
	Low (Non-selected)	H	V_3	
		L	V_2	
L	High (Selected)	H	V_5	Segment driver
		L	V_{DD}	
	Low (Non-selected)	H	V_3	
		L	V_2	

Table 1

When MSM5260GS is used as common driver, both LOAD pin and COM/SEG pin are to be connected to V_{DD}. In this case, a bias voltage of common side's non-selected level is to be supplied to V_2 and V_3 pins.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V.
  V_{SS} is a ground pin (V_{SS} = 0V)

- **V_{DD}, V_2, V_3, V_5**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the register is usually used as supply voltage source.
  Figure 1 shows the case when bias voltage, which is used to drive the LCD, is obtained by the voltage division by external registers.

- **$O_1 \sim O_{80}$**
  Display data output pins which correspond to the 80-bit latch contents.
  One of V_{DD}, V_2, V_3 and V_5 is selected as a display driving voltage source according to the combination of latched data level and DF signal. (Refer to the time chart and Table 1.)

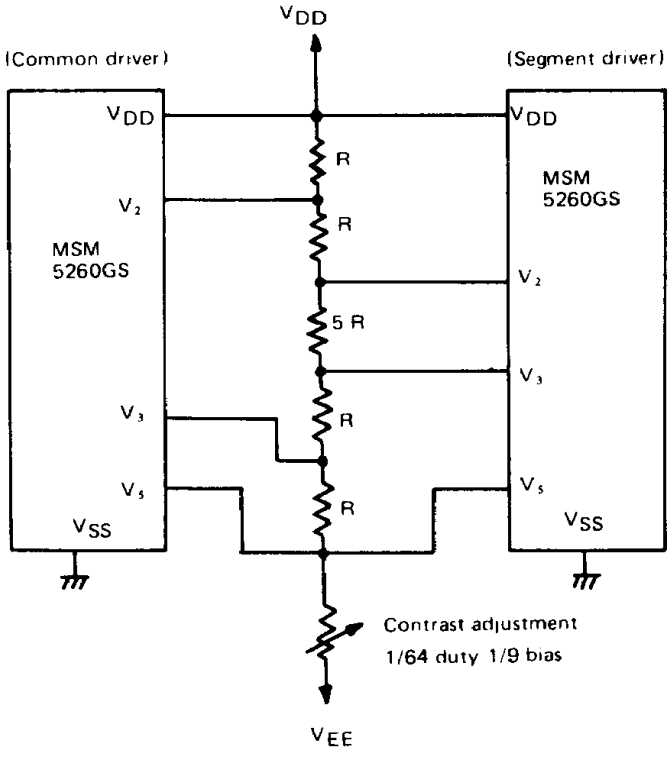
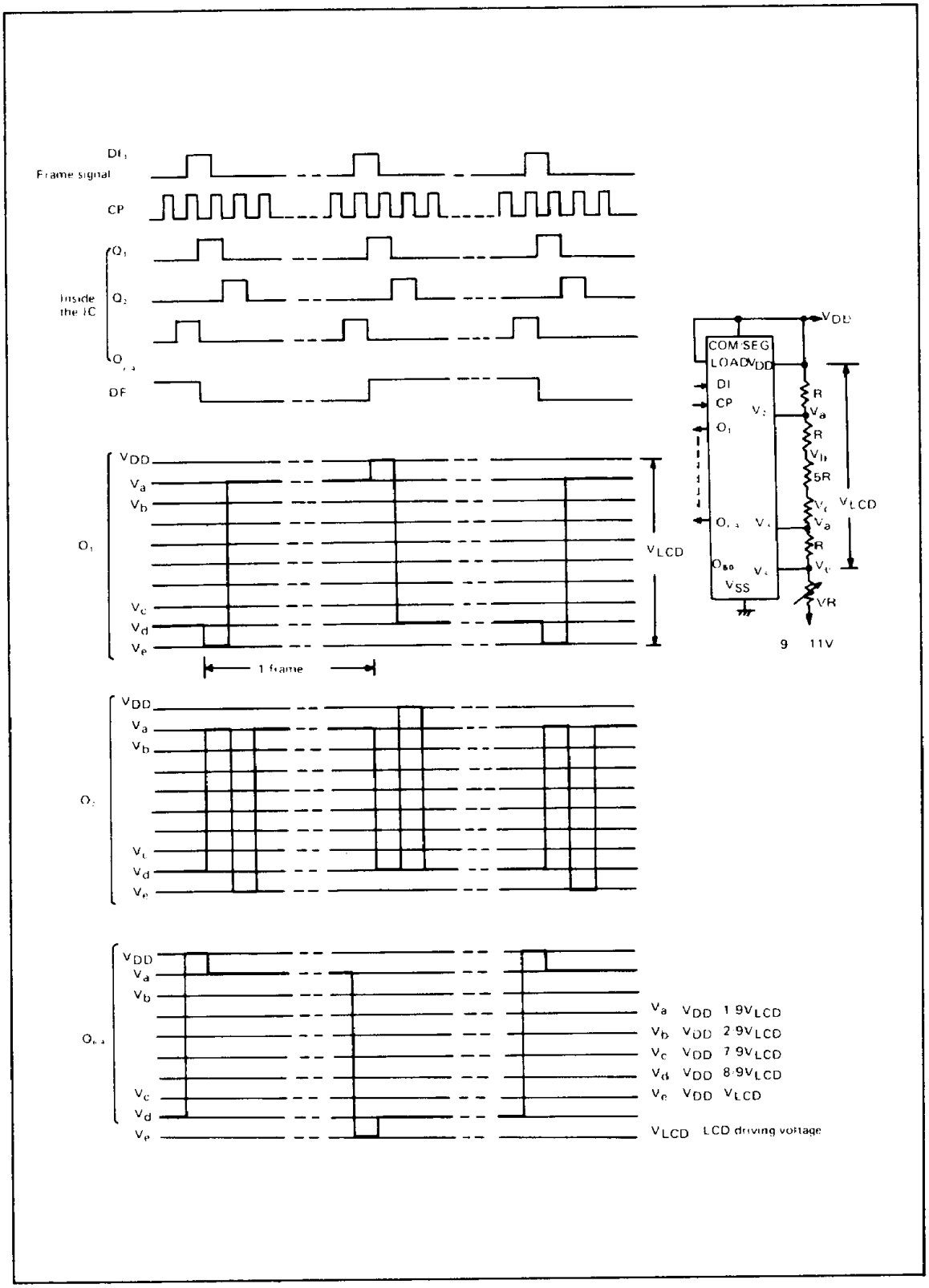


Figure 1

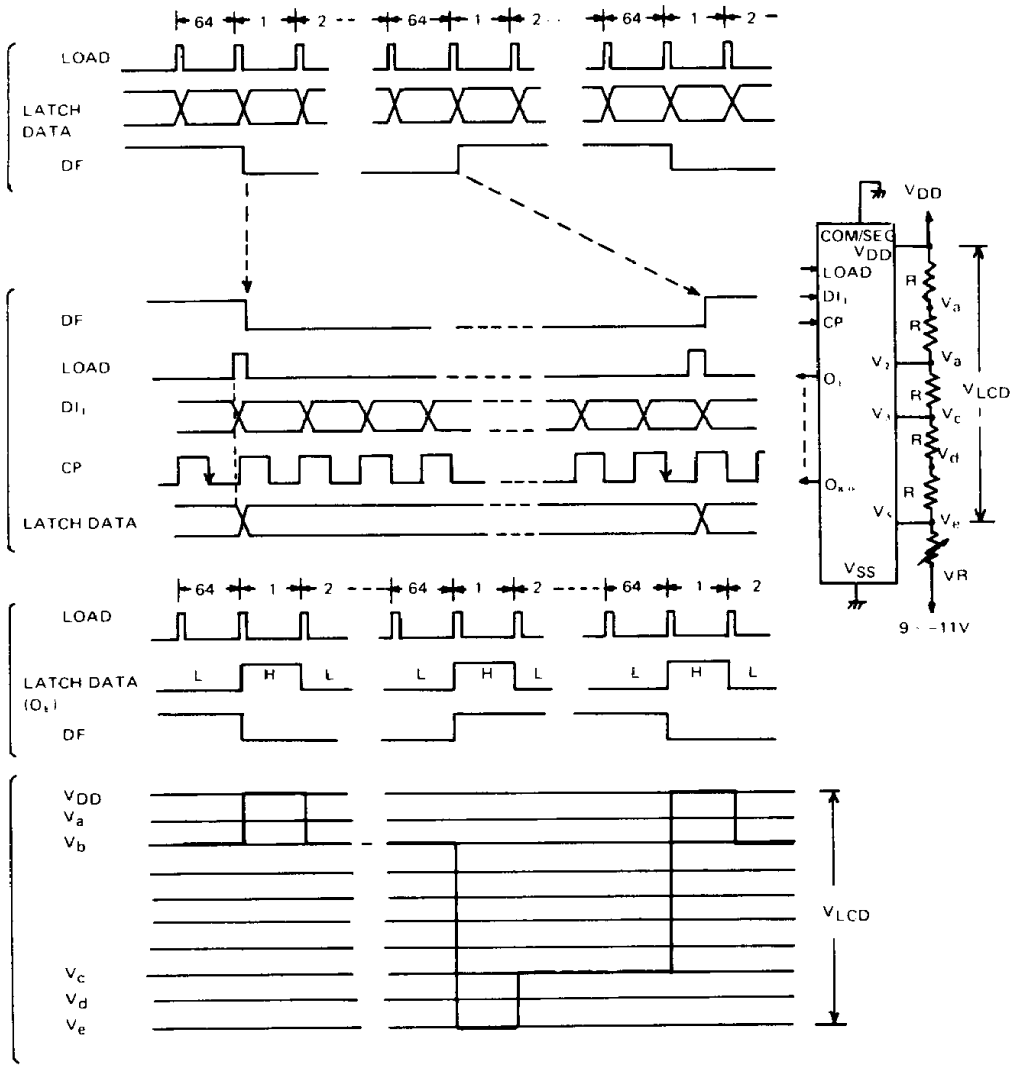
TIME CHART (COMMON DRIVER)

1/64 duty, 1/9 bias



TIMING CHART (SEGMENT DRIVER)

1/64 duty, 1/9 bias



$V_a = V_{DD} - 1/9V_{LCD}$

$V_b = V_{DD} - 2/9V_{LCD}$

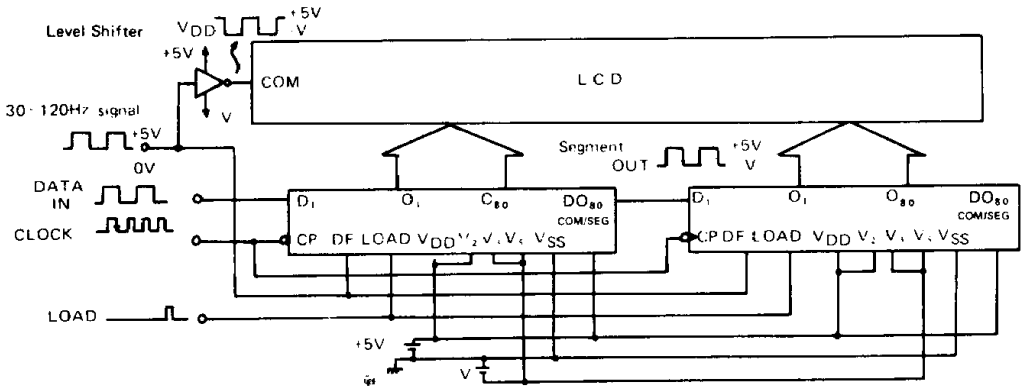
$V_c = V_{DD} - 7/9V_{LCD}$

$V_d = V_{DD} - 8/9V_{LCD}$

$V_e = V_{DD} - V_{LCD}$

APPLICATION CIRCUIT

- STATIC display



The MSM5260GS can make a static drive of a LCD by controlling the supply voltage. So it can be used to drive a color LCD which requires high driving voltage. The value $V_{DD} \sim V_5$ must be $18V > V_{DD} \sim V_5 \geq 5V$.

- 1/64 duty, 1/9 bias