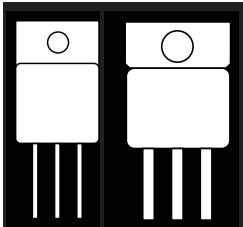


OM55N10SC OM60N10SC OM75N05SC OM75N06SC
OM55N10SA OM75N05SA OM75N06SA

LOW VOLTAGE, LOW $R_{DS(on)}$ POWER MOSFETS IN HERMETIC ISOLATED PACKAGE



50V, 60V, And 100V Ultra Low $R_{DS(on)}$
Power MOSFETs In TO-254 And TO-258
Isolated Packages

FEATURES

- Isolated Hermetic Metal Packages
- Ultra Low $R_{DS(on)}$
- Low Conductive Loss/Low Gate Charge
- Available Screened To MIL-S-19500, TX, TXV And S Levels
- Ceramic Feedthroughs available

DESCRIPTION

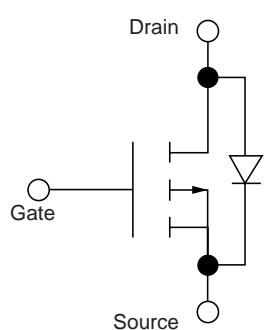
This series of hermetic packaged MOSFETs are ideally suited for low voltage applications; battery powered voltage power supplies, motor controls, dc to dc converters and synchronous rectification. The low conduction loss allows smaller heat sinking and the low gate charge simpler drive circuitry.

MAXIMUM RATINGS (Per Device)

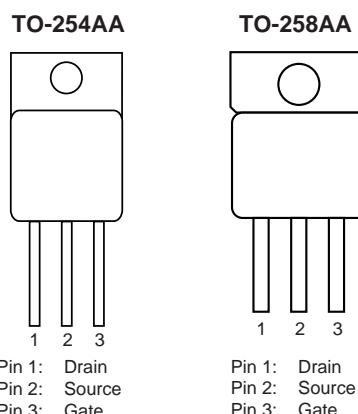
PART NO.	V_{DS} (V)	$R_{DS(on)}$ ()	I_D (A)	Package
OM60N10SC	100	.025	60	TO-258AA
OM55N10SC	100	.030	55	TO-258AA
OM55N10SA	100	.035	55	TO-254AA
OM75N06SC	60	.016	75	TO-258AA
OM75N06SA	60	.018	75	TO-254AA
OM75N05SC	50	.016	75	TO-258AA
OM75N05SA	50	.018	75	TO-254AA

3.1

SCHEMATIC



PIN CONNECTION



OM55N10SA - OM75N06SC

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	60N10SC	55N10SA 55N10SC	75N06SA 75N06SC	75N05SA 75N05SC	Units
V_{DS} Drain-Source Voltage	100	100	60	50	V
V_{DGR} Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	100	100	60	50	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current ²	60	55	75	75	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current ²	37	33	45	45	A
I_{DM} Pulsed Drain Current ¹	180	180	225	225	A
$P_D @ T_C = 25^\circ\text{C}$ Maximum Power Dissipation	130	125	125	125	W
$P_D @ T_C = 100^\circ\text{C}$ Maximum Power Dissipation	55	50	50	50	W
Junction-To-Case Linear Derating Factor	1.00	1.00	1.00	1.00	W/ $^\circ\text{C}$
T_J Operating and T_{stg} Storage Temperature Range	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Lead Temperature (1/16" from case for 10 secs.)	300	300	300	300	$^\circ\text{C}$

1 Pulse Test: Pulse width 300 μsec . Duty Cycle 1.5%.

2 Package Limited: SA $I_D = 25\text{A}$ & SC $I_D = 35\text{A}$ @ 25°C

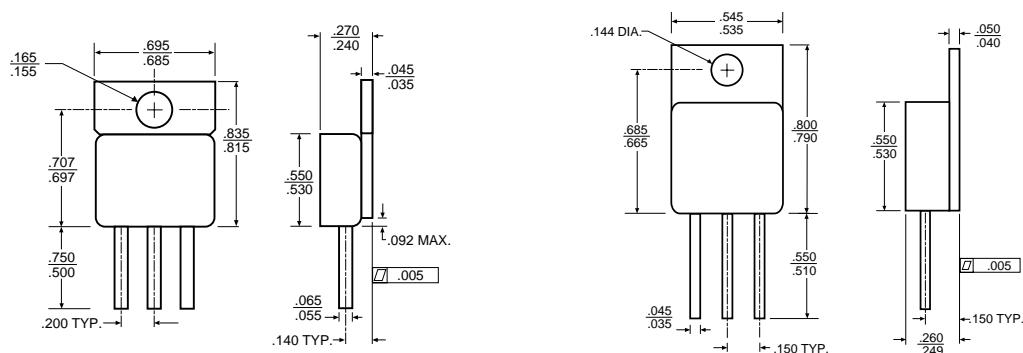
THERMAL RESISTANCE

R_{thJC} Junction-to-Case	1.0	$^\circ\text{C/W}$
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PACKAGE LIMITATIONS

Parameters	TO254AA	TO-258AA	Unit
I_D Continuous Drain Current	25	35	A
Linear Derating Factor, Junction-to-Ambient	.020	.025	W/ $^\circ\text{C}$
R_{thJA} Thermal Resistance, Junction-to-Ambient (Free Air Operation)	50	40	$^\circ\text{C/W}$

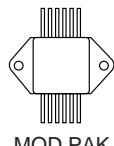
MECHANICAL OUTLINE



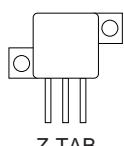
TO-258AA

TO-254AA

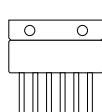
PACKAGE OPTIONS



MOD PAK



Z-TAB



6 PIN SIP

Note: MOSFETs are also available in Z-Tab, dual and quad pak styles. Duals and quads available in non-gate versions only.
Please call the factory for more information.

3.1

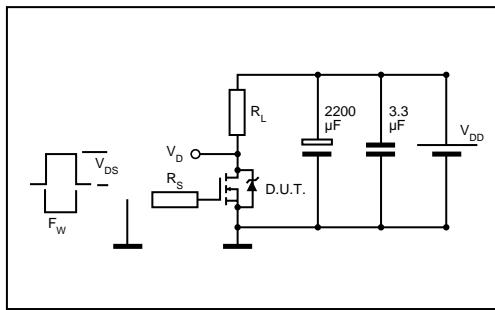
OM75N05SA ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Avalanche Characteristics		Min.	Typ.	Max.	Units	Test Conditions
I_{AR}	Avalanche Current			70	A	(repetitive or non-repetitive, $T_j = 25^\circ\text{C}$)
E_{AS}	Single Pulse Avalanche Energy			900	mJ	(starting $T_j = 25^\circ\text{C}$, $I_o = I_{AR}$, $V_{DD} = 25\text{ V}$)
E_{AR}	Repetitive Avalanche Energy			200	mJ	(pulse width limited by T_{max} , $d < 1\%$)
I_{AR}	Avalanche Current			40	A	(repetitive or non-repetitive, $T_j = 100^\circ\text{C}$)
Electrical Characteristics - OFF						
$V_{BR(0SS)}$	Drain-Source Breakdown Voltage	50			V	$I_o = 250\text{ }\mu\text{A}$, $V_{GS} = 0$
$I_{DS(on)}$	Zero Gate Voltage Drain Current ($V_{GS} = 0$)		250	μA		$V_{DS} = \text{Max. Rat.}$
			1000	μA		$V_{DS} = \text{Max. Rat.} \times 0.8$, $T_c = 125^\circ\text{C}$
I_{GSS}	Gate-Body Leakage Current ($V_{GS} = 0$)		± 100	nA		$V_{GS} = \pm 20\text{ V}$
Electrical Characteristics - ON						
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	$V_{DS} = V_{GS}$, $I_o = 250\text{ }\mu\text{A}$
$R_{DS(on)}$	Static Drain-Source On Resistance		0.018			$V_{GS} = 10\text{ V}$, $I_o = 40\text{ A}$
			0.036			$T_c = 100^\circ\text{C}$
$I_{D(on)}$	On State Drain Current	75			A	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 10\text{ V}$
Electrical Characteristics - Dynamic						
g_{ds}	Forward Transconductance	25			S	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_o = 40\text{ A}$
C_{iss}	Input Capacitance	4100			pF	$V_{DS} = 25\text{ V}$
C_{oss}	Output Capacitance	1800			pF	$V_{GS} = 0$
C_{rss}	Reverse Transfer Capacitance	420			pF	$f = 1\text{ mHz}$
Electrical Characteristics - Switching On						
$T_{d(on)}$	Turn-On Time		190		nS	$V_{DD} = 20\text{ V}$, $I_o = 40\text{ A}$
t_r	Rise Time		900		nS	$R_S = 50\text{ } \Omega$, $V_{GS} = 10\text{ V}$
$(di/dt)_{on}$	Turn-On Current Slope		150	A/ μs		$V_{DD} = 20\text{ V}$, $I_o = 40\text{ A}$
R_S						$R_S = 50\text{ } \Omega$, $V_{GS} = 10\text{ V}$
Q_g	Total Gate Charge		130		nC	$V_{DD} = 20\text{ V}$, $I_o = 40\text{ A}$, $V_{GS} = 10\text{ V}$
Electrical Characteristics - Switching Off						
$T_{f(off)}$	Off Voltage Rise Time		360		nS	$V_{DD} = 35\text{ V}$, $I_o = 75\text{ A}$
t_f	Fall Time		280		nS	$R_S = 50\text{ } \Omega$, $V_{GS} = 10\text{ V}$
t_{cross}	Cross-Over Time		600		nS	
Electrical Characteristics - Source Drain Diode						
I_{SD}	Source Drain Current		75	A		
$I_{SDM(*)}$	Source Drain Current (pulsed)		300	A		
V_{SD}	Forward On Voltage		1.5	V		$I_{SD} = 75\text{ A}$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time		120		nS	$I_{SD} = 75\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge		0.45	μC		$V_R = 20\text{ V}$
I_{RRM}	Reverse Recovery Current		6.5	A		

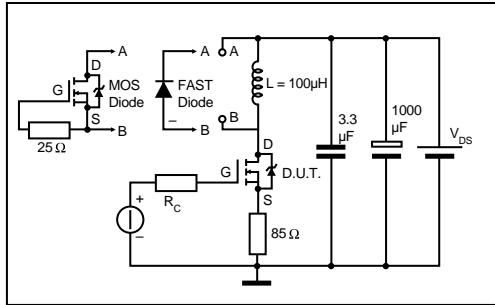
*Pulsed: Pulse Duration 300μs, Duty Cycle 1.5%.

OM55N10SA - OM75N06SC

SWITCHING TIMES TEST CIRCUITS FOR RESISTIVE LOAD



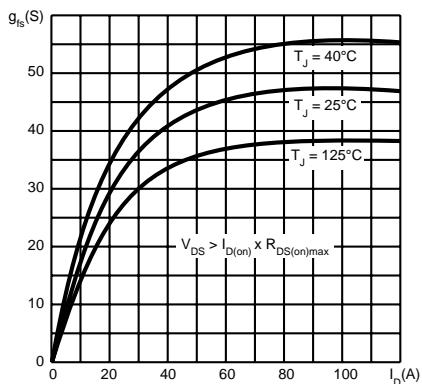
TEST CIRCUIT FOR INDUCTIVE LOAD SWITCHING AND DIODE REVERSE RECOVERY TIME



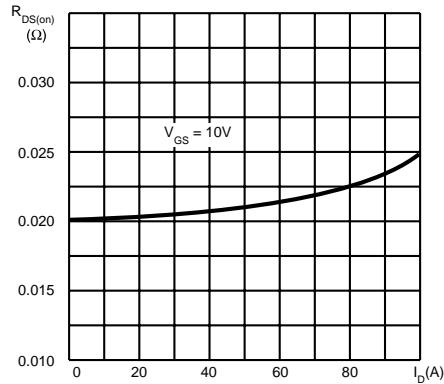
OM55N10SA - OM75N06SC

OM75N06SC, OM75N06SA, OM75N05SC, OM75N05SA

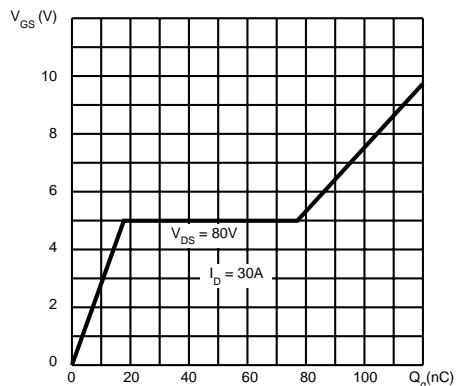
Transconductance



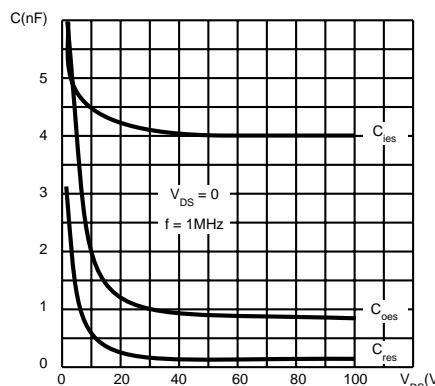
Static Drain-Source On Resistance



Gate Charge vs Gate-Source Voltage

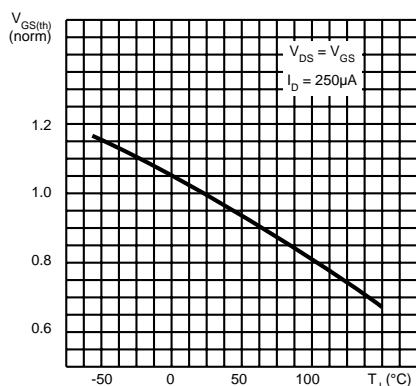


Capacitance Variations

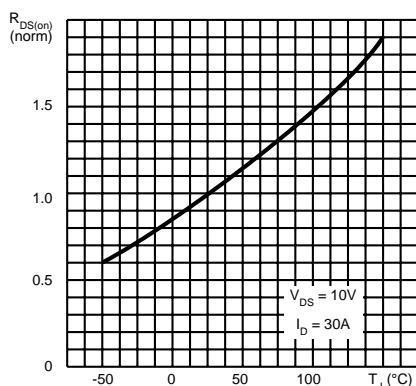


3.1

Normalized Gate Threshold Voltage vs Temperature



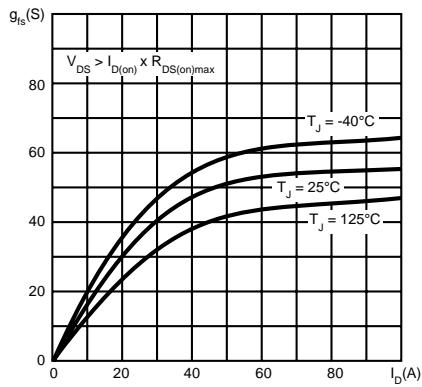
Normalized On Resistance vs Temperature



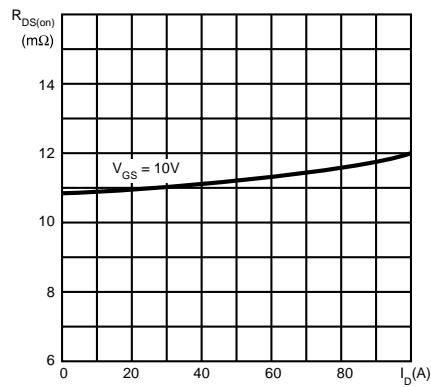
OM55N10SA - OM75N06SC

OM75N06SC, OM75N06SA, OM75N05SC, OM75N05SA

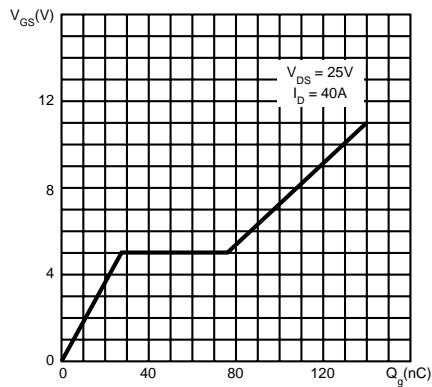
Transconductance



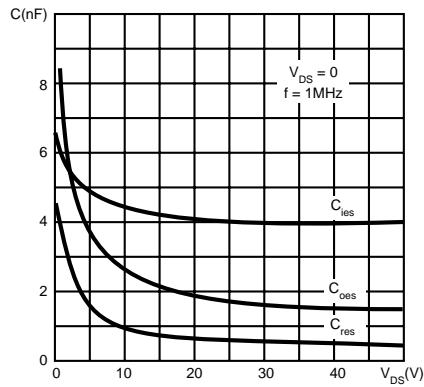
Static Drain-Source On Resistance



Gate Charge vs Gate-Source Voltage

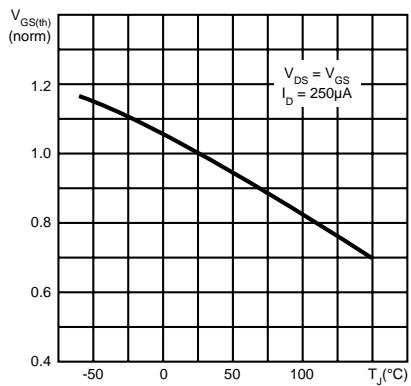


Capacitance Variations



3.1

Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature

