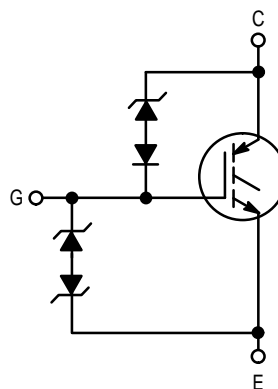


Product Preview

SMARTDISCRETES™
Internally Clamped, N-Channel
IGBT

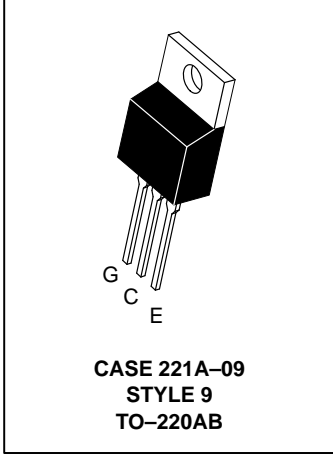
This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Collector Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability



MGP20N14CL

20 AMPERES
VOLTAGE CLAMPED
N-CHANNEL IGBT
V_{CE(on)} = 1.9 VOLTS
135 VOLTS (CLAMPED)



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	CLAMPED	V _{dc}
Collector–Gate Voltage	V _{CGR}	CLAMPED	V _{dc}
Gate–Emitter Voltage	V _{GE}	CLAMPED	V _{dc}
Collector Current — Continuous	I _C	20	Adc
— Single Pulsed (t _p = ± 10 μs)	I _{CM}	60	Apk
Total Power Dissipation (TO-220)	P _D	150	Watts
Derate Above 25°C		1.0	W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C
Single Pulse Collector–Emitter Avalanche Energy @ Starting T _J = 25°C (V _{CC} = 80 V, V _{GE} = 5 V, Peak I _L = 10 A, L = 10 mH)	E _{AS}	500	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO-220)	R _{θJC}	1.0	°C/W
— Junction to Ambient	R _{θJA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

SMARTDISCRETES is a trademark of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MGP20N14CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Clamp Voltage (I _{Clamp} = 10 mA, T _J = -40 to 150°C)	V _{(BR)CES}	135			Vdc
Zero Gate Voltage Collector Current (V _{CE} = 100 V, V _{GE} = 0 V) (V _{CE} = 100 V, V _{GE} = 0 V, T _J = 150°C)	I _{CES}	—	—	10 100	μA
Gate-Emitter Clamp Voltage (I _G = 1 mA)	V _{(BR)GES}	10			Vdc
Gate-Emitter Leakage Current (V _{GE} = ±5 V, V _{CE} = 0 V)	I _{GES}	—	—	1.0	μA

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1 mA) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	1.0	1.5 4.4	2.0	V mV/°C
Collector-Emitter On-Voltage (V _{GE} = 5 V, I _C = 10 A) (V _{GE} = 5 V, I _C = 10 Adc, T _J = 175°C)	V _{CE(on)}	—		1.9 1.8	V
Forward Transconductance (V _{CE} > 15 V, I _C = 10 A)	g _{fe}	8.0	15	—	Mhos

DYNAMIC CHARACTERISTICS

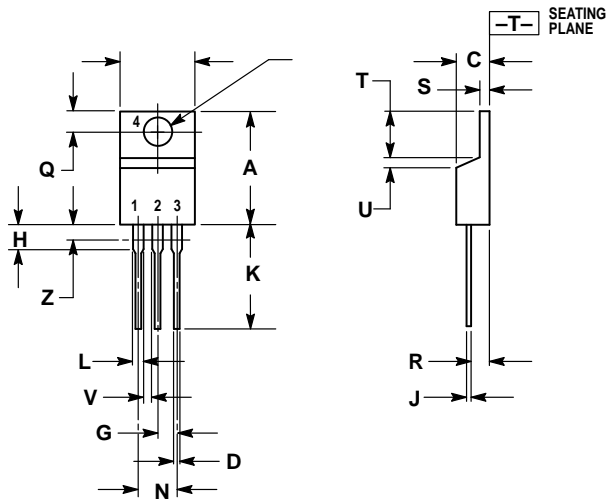
Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	430	600	pF
Output Capacitance		C _{oes}	—	182	250	
Transfer Capacitance		C _{res}	—	48	100	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{CC} = 68 V, I _C = 20 A, V _{GE} = 5 V, R _G = 9.1 Ω)	t _{d(on)}	—	TBD	TBD	ns
Rise Time		t _r	—	TBD	TBD	
Turn-Off Delay Time		t _{d(off)}	—	TBD	TBD	
Fall Time		t _f	—	TBD	TBD	
Total Gate Charge	(V _{CC} = 108 V, I _C = 20 A, V _{GE} = 5 V)	Q _T	—	14	20	nC
Gate-Emitter Charge		Q _{ge}	—	3.0	—	
Gate-Collector Charge		Q _{gc}	—	6.0	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS




STYLE 9:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-09
 ISSUE Z

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