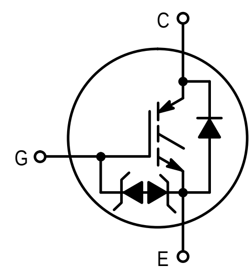
*Designer's™ Data Sheet*
# Insulated Gate Bipolar Transistor
## N–Channel Enhancement–Mode Silicon Gate

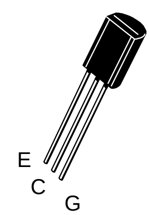
**MGS13002D**

**IGBT**
**0.5 A @ 25°C**
**600 V**

This IGBT contains a built–in free wheeling diode and a gate protection zener diodes. Fast switching characteristics result in efficient operation at higher frequencies. This device is ideally suited for high frequency electronic ballasts.

- Built–In Free Wheeling Diodes
- Built–In Gate Protection Zener Diode
- Industry Standard Package (TO92 — 1.0 Watt)
- High Speed $E_{off}$: Typical 6.5 μJ @ $I_C$ = 0.3 A; $T_C$ = 125°C and dV/dt = 1000 V/μs
- Robust High Voltage Termination
- Robust Turn–Off SOA




**CASE 029–05**
**STYLE 35**
**TO–226AE**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CES}$ | 600 | Vdc |
| Collector–Gate Voltage ($R_{GE}$ = 1.0 MΩ) | $V_{CGR}$ | 600 | Vdc |
| Gate–Emitter Voltage — Continuous | $V_{GES}$ | ±15 | Vdc |
| Collector Current — Continuous @ $T_C$ = 25°C<br>— Continuous @ $T_C$ = 90°C<br>— Repetitive Pulsed Current (1) | $I_{C25}$<br>$I_{C90}$<br>$I_{CM}$ | 0.5<br>0.3<br>2.0 | Adc |
| Total Power Dissipation @ $T_C$ = 25°C | $P_D$ | 1.0 | Watt |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |

**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance — Junction to Case – IGBT<br>Thermal Resistance — Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 25<br>125 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds | $T_L$ | 260 | °C |

**UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS** ($T_C$ ≤ 150°C)

| | | | |
|---|---|---|---|
| Single Pulse Drain–to–Source Avalanche<br>Energy – Starting @ $T_C$ = 25°C<br>@ $T_C$ = 125°C<br>$V_{CE}$ = 100 V, $V_{GE}$ = 15 V, Peak $I_L$ = 2.0 A, L = 3.0 mH, $R_G$ = 25 Ω | $E_{AS}$ | <br>125<br>40 | mJ |

(1) Pulse width is limited by maximum junction temperature repetitive rating.

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Collector–to–Emitter Breakdown Voltage ($V_{GE}$ = 0 Vdc, $I_C$ = 250 μAdc) | | $V_{(BR)CES}$ | 600 | 680 | — | Vdc |
| Temperature Coefficient (Positive) | | | — | 0.7 | — | V/°C |
| Zero Gate Voltage Collector Current ($V_{CE}$ = 600 Vdc, $V_{GE}$ = 0 Vdc) | | $I_{CES}$ | — | 0.1 | 5.0 | μAdc |
| ($V_{CE}$ = 600 Vdc, $V_{GE}$ = 0 Vdc, $T_C$ = 125°C) | | | — | 5.0 | 50 | |
| Gate–Body Leakage Current ($V_{GE}$ = ±15 Vdc, $V_{CE}$ = 0 Vdc) | | $I_{GES}$ | — | 10 | 100 | μAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Collector–to–Emitter On–State Voltage ($V_{GE}$ = 15 Vdc, $I_C$ = 0.3 Adc) | | $V_{CE(on)}$ | — | 1.6 | 2.0 | Vdc |
| ($V_{GE}$ = 15 Vdc, $I_C$ = 0.3 Adc, $T_C$ = 125°C) | | | — | 1.5 | — | |
| Gate Threshold Voltage ($V_{CE}$ = $V_{GE}$, $I_C$ = 250 μAdc) | | $V_{GE(th)}$ | 3.5 | — | 6.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | — | 6.0 | — | mV/°C |
| Forward Transconductance ($V_{CE}$ = 10 Vdc, $I_C$ = 0.5 Adc) | | $g_{fe}$ | 0.3 | 0.42 | — | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{CE}$ = 20 Vdc, $V_{GE}$ = 0 Vdc, f = 1.0 MHz) | $C_{ies}$ | — | 75 | 100 | pF |
| Output Capacitance | | $C_{oes}$ | — | 11 | 20 | |
| Transfer Capacitance | | $C_{res}$ | — | 1.6 | 5.0 | |
| **DIODE CHARACTERISTICS** | | | | | | |
| Diode Forward Voltage Drop ($I_{EC}$ = 0.3 Adc) | | $V_{FEC}$ | — | 5.0 | 6.0 | Vdc |
| ($I_{EC}$ = 0.3 Adc, $T_C$ = 125°C) | | | — | 5.2 | — | |
| ($I_{EC}$ = 0.1 Adc) | | | — | 2.3 | 3.0 | |
| ($I_{EC}$ = 0.1 Adc, $T_C$ = 125°C) | | | — | 2.3 | — | |
| Reverse Recovery Time | ($I_F$ = 0.4 Adc, $V_R$ = 300 Vdc, dIF/dt = 10 A/μs) | $t_{rr}$ | — | 150 | — | ns |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | — | 35 | — | μC |
| **SWITCHING CHARACTERISTICS(1)** | | | | | | |
| Turn–Off Delay Time | ($V_{CC}$ = 300 Vdc, $I_C$ = 0.4 Adc, $V_{GE}$ = 15 Vdc, L = 3.0 mH, $R_G$ = 25 Ω, $T_C$ = 25°C, dV/dt = 1000 V/μs) Energy losses include "tail" | $t_{d(off)}$ | — | 28 | — | ns |
| Fall Time | | $t_f$ | — | 150 | — | |
| Turn–Off Switching Loss | | $E_{off}$ | — | 3.25 | — | μJ |
| Turn–Off Delay Time | ($V_{CC}$ = 300 Vdc, $I_C$ = 0.4 Adc, $V_{GE}$ = 15 Vdc, L = 3.0 mH, $R_G$ = 25 Ω, $T_C$ = 125°C, dV/dt = 1000 V/μs) Energy losses include "tail" | $t_{d(off)}$ | — | 21 | — | ns |
| Fall Time | | $t_f$ | — | 280 | — | |
| Turn–Off Switching Loss | | $E_{off}$ | — | 8.0 | — | μJ |
| Gate Charge | ($V_{CC}$ = 300 Vdc, $I_C$ = 0.3 Adc, $V_{GE}$ = 15 Vdc) | $Q_T$ | — | 6.4 | — | nC |

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

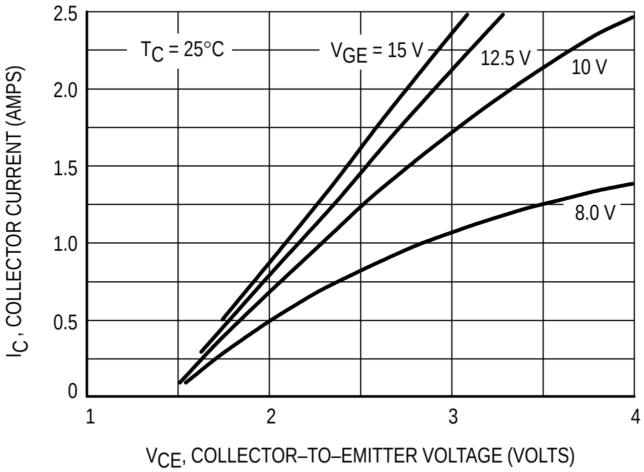



**Figure 1. Saturation Characteristics**

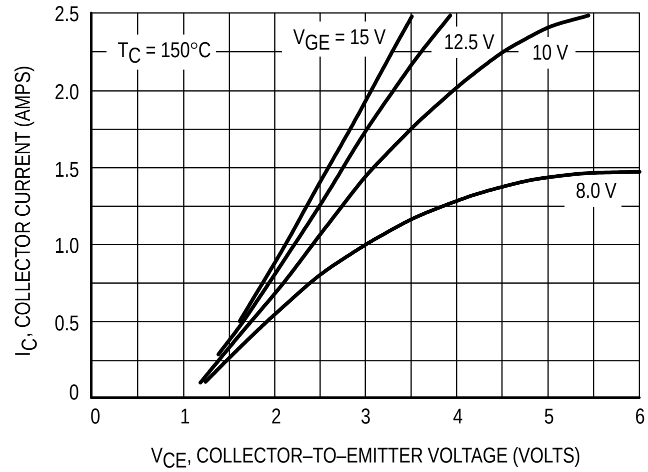



**Figure 2. Saturation Characteristics**

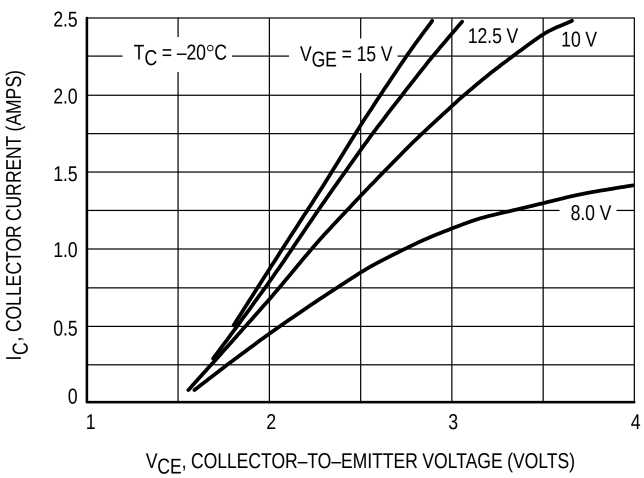



**Figure 3. Saturation Characteristics**

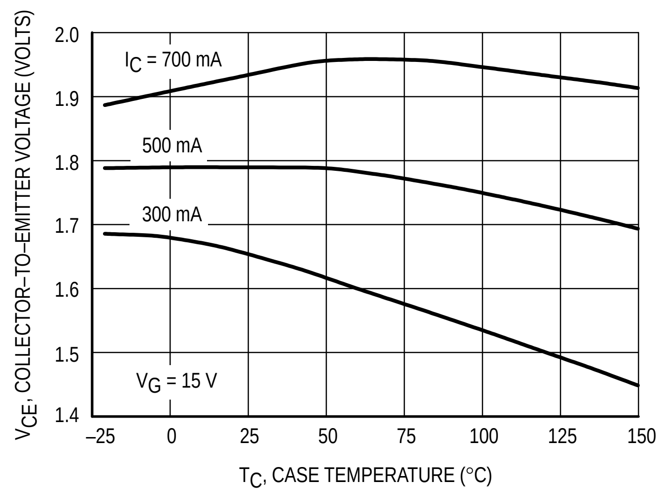



**Figure 4. Collector–To–Emitter Saturation Voltage versus Case Temperature**

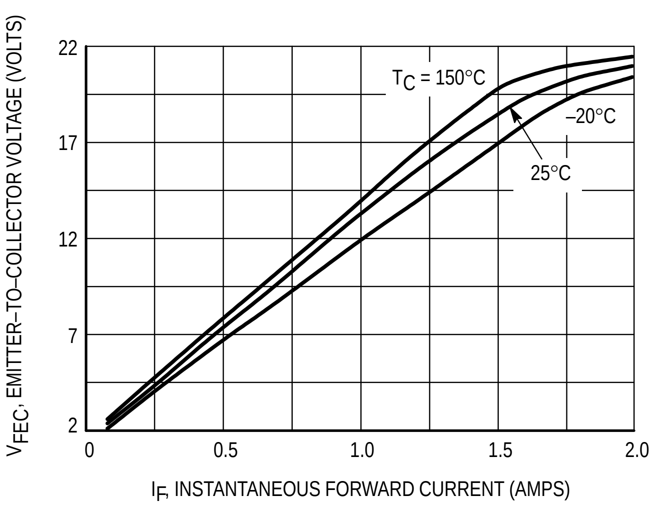



**Figure 5. Diode Forward Voltage Drop**

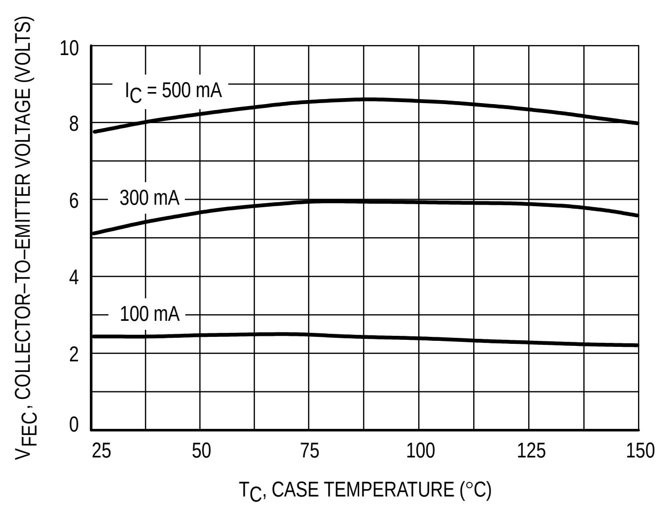



**Figure 6. Diode Forward Voltage versus Case Temperature**

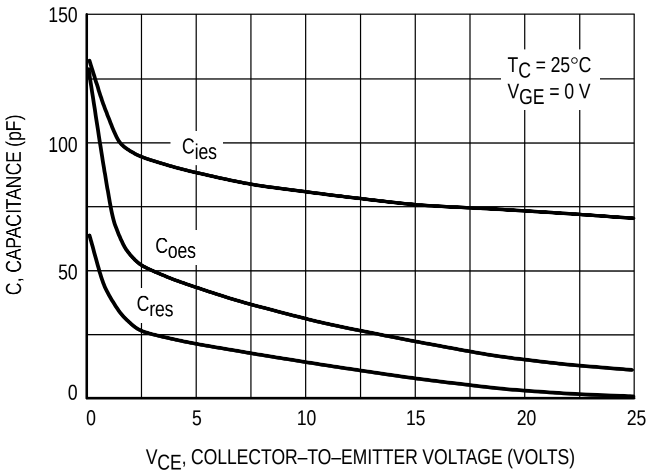



**Figure 7. Capacitance Variation**

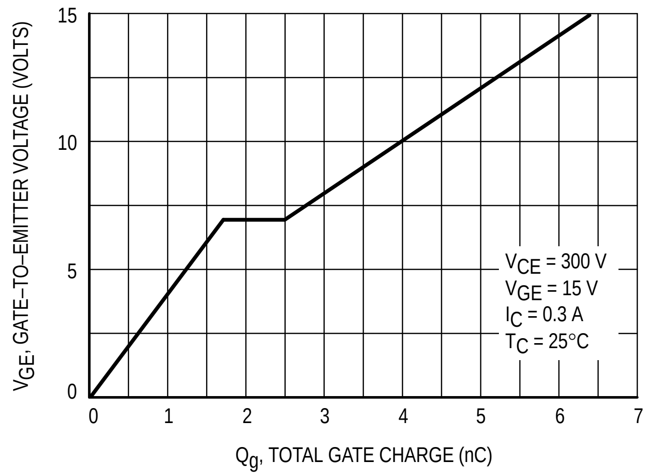



**Figure 8. Gate–To–Emitter Voltage versus Total Charge**

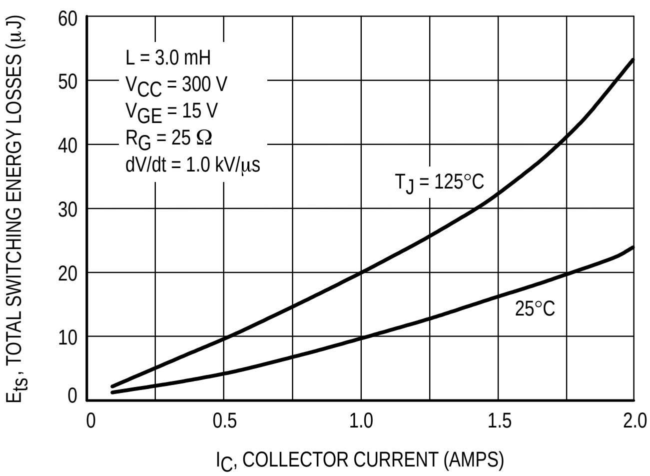



**Figure 9. Total Switching Losses versus Collector Current**

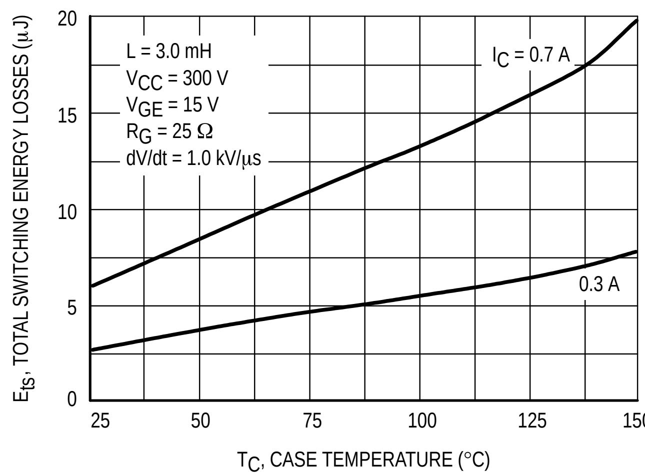



**Figure 10. Total Switching Losses versus Case Temperature**

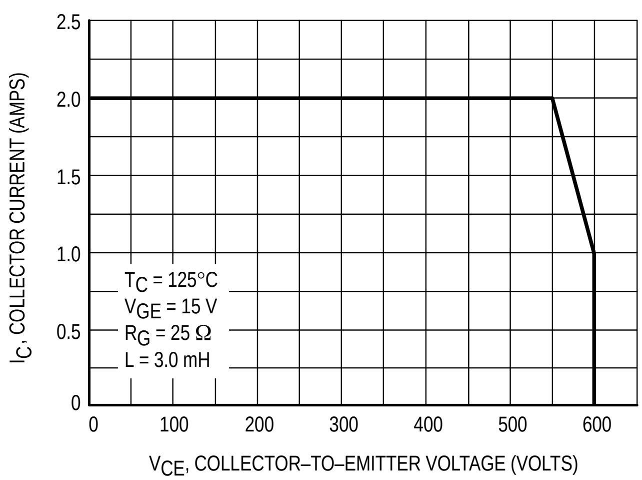



**Figure 11. Minimum Turn–Off Safe Operating Area**

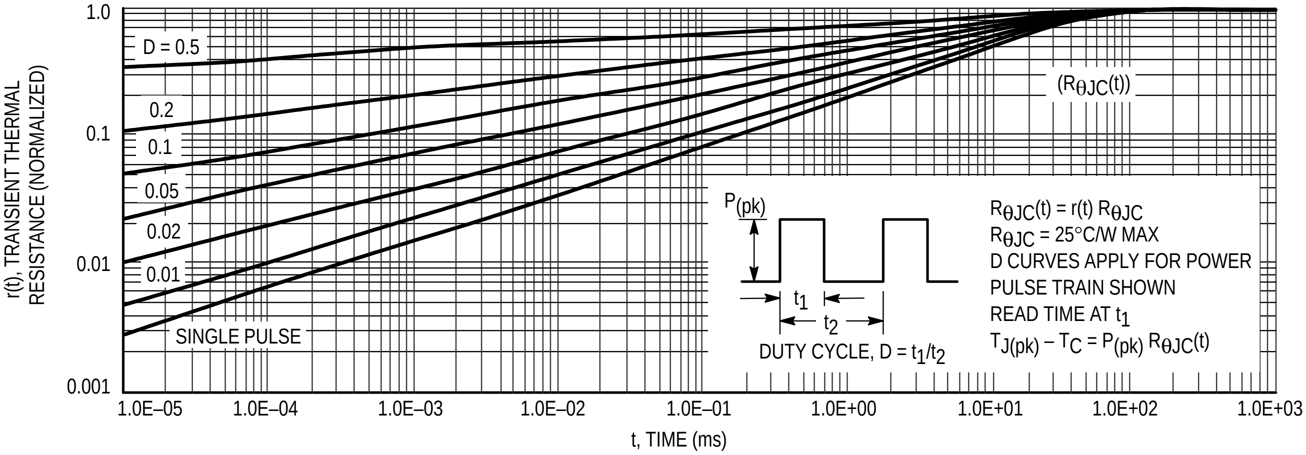
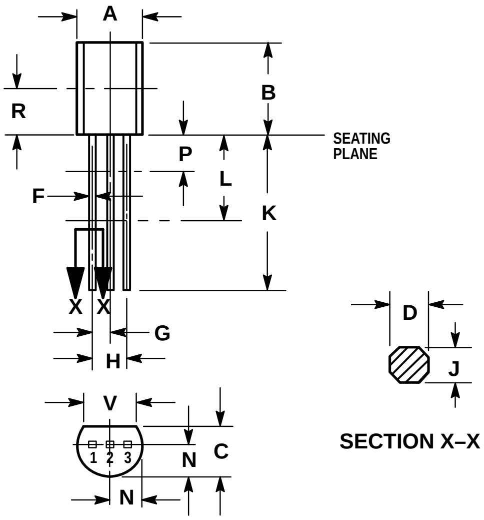



**Figure 12. Typical Thermal Response**

## PACKAGE DIMENSIONS




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MIMIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.44 | 5.21 |
| B | 0.290 | 0.310 | 7.37 | 7.87 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.018 | 0.022 | 0.46 | 0.56 |
| F | 0.016 | 0.019 | 0.41 | 0.48 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.018 | 0.024 | 0.46 | 0.61 |
| K | 0.500 | — | 12.70 | — |
| L | 0.250 | — | 6.35 | — |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | — | 0.100 | — | 2.54 |
| R | 0.135 | — | 3.43 | — |
| V | 0.135 | — | 3.43 | — |

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

**CASE 029–05**
**TO–226AE**
**ISSUE AD**



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