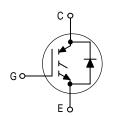
Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N-Channel Enhancement-Mode Silicon Gate

This Insulated Gate Bipolar Transistor (IGBT) is co-packaged with a soft recovery ultra-fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co-packaged IGBT's save space, reduce assembly time and cost.

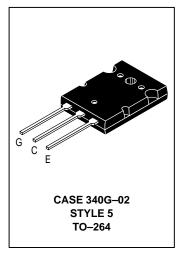
- Industry Standard High Power TO-264 Package (TO-3PBL)
- High Speed E_{off}: 160 μJ per Amp typical at 125°C
- High Short Circuit Capability 10 μs minimum
- · Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA



MGY20N120D

Motorola Preferred Device

IGBT & DIODE IN TO-264 20 A @ 90°C 28 A @ 25°C 1200 VOLTS SHORT CIRCUIT RATED



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	VCES	1200	Vdc
Collector–Gate Voltage (R _{GE} = 1.0 MΩ)	VCGR	1200	Vdc
Gate-Emitter Voltage — Continuous	V _{GE}	±20	Vdc
Collector Current — Continuous @ T _C = 25°C — Continuous @ T _C = 90°C — Repetitive Pulsed Current (1)	IC25 IC90 ICM	28 20 56	Adc Apk
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	174 1.39	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t _{SC}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	R _θ JC R _θ JC R _θ JA	0.7 1.1 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

⁽¹⁾ Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1



MGY20N120D

C	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Collector-to-Emitter Breakdown	V(BR)CES	4000			Vdc	
(V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positi		1200 —	870	_	mV/°C	
Zero Gate Voltage Collector Curr	ICES				μAdc	
(VCE = 1200 Vdc, VGE = 0 Vd (VCE = 1200 Vdc, VGE = 0 Vd		_	_	100 2500		
Gate-Body Leakage Current (Vo	IGES			250	nAdc	
ON CHARACTERISTICS (1)	E === 124, 10E = 124,	1 000	<u> </u>			
Collector-to-Emitter On-State V	VCE(on)				Vdc	
(V _{GE} = 15 Vdc, I _C = 10 Adc)	02(0)	–	2.42	3.54		
$(V_{GE} = 15 \text{ Vdc}, I_{C} = 10 \text{ Adc}, T)$ $(V_{GE} = 15 \text{ Vdc}, I_{C} = 20 \text{ Adc})$		_	2.36 2.90	— 4.99		
Gate Threshold Voltage	V _{GE(th)}				Vdc	
$(V_{CE} = V_{GE}, I_{C} = 1.0 \text{ mAdc})$	02()	4.0	6.0	8.0		
Threshold Temperature Coeffic		_	10	_	mV/°C	
Forward Transconductance (VCE	9fe		12	_	Mhos	
DYNAMIC CHARACTERISTICS		1 -				
Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc,	C _{ies}		1876	_	pF
Output Capacitance	f = 1.0 MHz)	C _{oes}	_	208		1
Transfer Capacitance		C _{res}	_	31	_	
SWITCHING CHARACTERISTICS	5(1)					1
Turn-On Delay Time	_	^t d(on)	_	88	_	ns
Rise Time	_	t _r	_	103	_	
Turn-Off Delay Time	(V _{CC} = 720 Vdc, I _C = 20 Adc,	td(off)	_	190	_]
Fall Time	$V_{GE} = 15 \text{ Vdc}, L = 300 \mu H$ $R_{G} = 20 \Omega$)	t _f	_	284	_	
Turn-Off Switching Loss	Energy losses include "tail"	E _{off}	_	1.65	2.75	mJ
Turn-On Switching Loss		E _{on}	_	2.42	3.75	
Total Switching Loss		E _{ts}	_	4.07	6.50	
Turn-On Delay Time		^t d(on)	-	83	_	ns
Rise Time	7	t _r	_	107	_]
Turn-Off Delay Time	(V _{CC} = 720 Vdc, I _C = 20 Adc,	td(off)	_	216	_	
Fall Time	V_{GE} = 15 Vdc, L = 300 μH R_{G} = 20 Ω, T_{J} = 125°C)	t _f	_	494	_	1
Turn-Off Switching Loss	Energy losses include "tail"	E _{off}	_	3.19	_	mJ
Turn-On Switching Loss	7	Eon	_	4.26	_	1
Total Switching Loss	7	E _{ts}	_	7.45	_	1
Gate Charge		QT	_	63	_	nC
	(V _{CC} = 720 Vdc, I _C = 20 Adc, V _{GE} = 15 Vdc)	Q ₁	_	20	_	1
		Q ₂	 	27	_	1
DIODE CHARACTERISTICS	1	1	1	1		<u> </u>
Diode Forward Voltage Drop		VFEC				Vdc
(I _{EC} = 10 Adc) (I _{EC} = 10 Adc, T _J = 125°C)		-	2.92 1.73	3.59		
(IEC = 10 Adc, IJ = 125°C)		_	1.73 3.67	— 4.57		

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Cha	Symbol	Min	Тур	Max	Unit			
DIODE CHARACTERISTICS — continued								
Reverse Recovery Time		t _{rr}	_	114	_	ns		
	$(I_F = 20 \text{ Adc}, V_R = 720 \text{ Vdc}, \\ dI_F/dt = 150 \text{ A}/\mu\text{s})$	ta	_	74	_			
		t _b	_	40	_			
Reverse Recovery Stored Charge		Q _{RR}	_	0.68	_	μС		
Reverse Recovery Time	(I _F = 20 Adc, V _R = 720 Vdc, dI _F /dt = 150 A/µs, T _J = 125°C)	t _{rr}	_	224	_	ns		
		ta	_	149	_			
		t _b	_	75	_			
Reverse Recovery Stored Charge		Q _{RR}	_	2.40	_	μС		
INTERNAL PACKAGE INDUCTANCE								
Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)		LE	_	13	_	nH		

TYPICAL ELECTRICAL CHARACTERISTICS

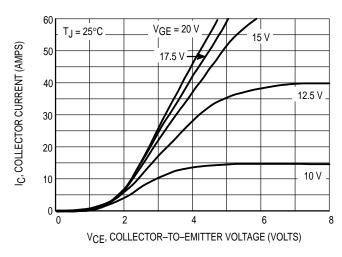


Figure 1. Output Characteristics

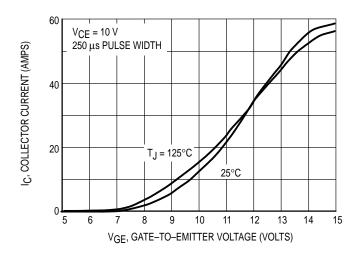


Figure 3. Transfer Characteristics

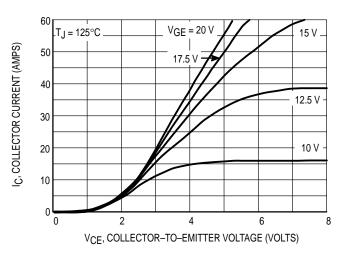


Figure 2. Output Characteristics

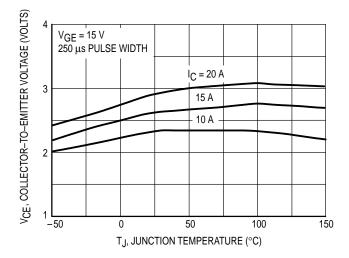


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

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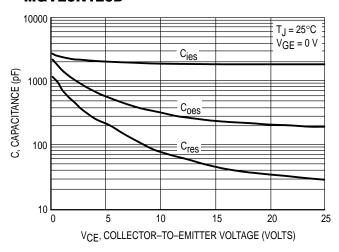


Figure 5. Capacitance Variation

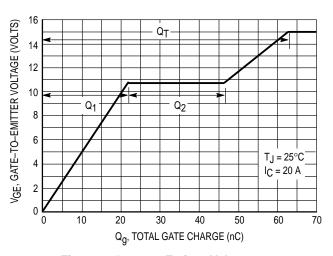


Figure 6. Gate-to-Emitter Voltage versus
Total Charge

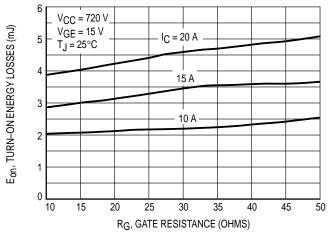


Figure 7. Turn–On Losses versus
Gate Resistance

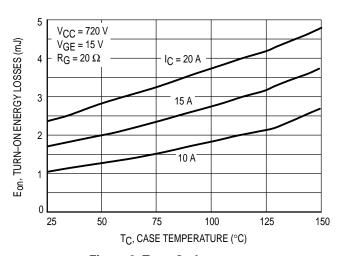


Figure 8. Turn-On Losses versus Case Temperature

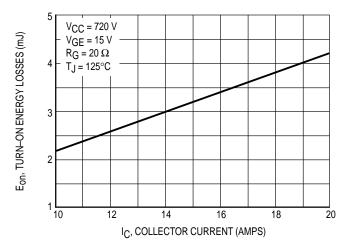


Figure 9. Turn-On Losses versus Collector Current

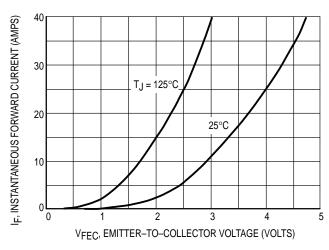


Figure 10. Diode Forward Voltage Drop

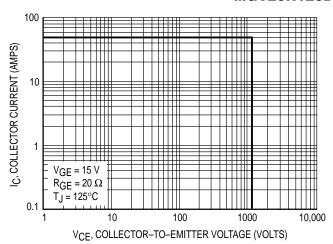


Figure 11. Reverse Biased Safe Operating Area

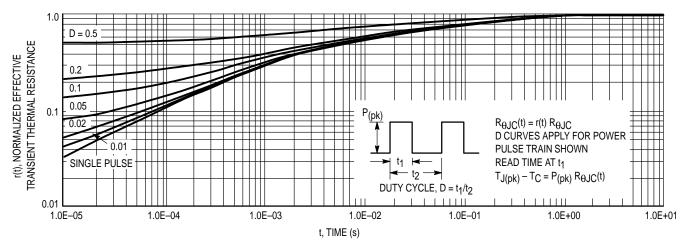
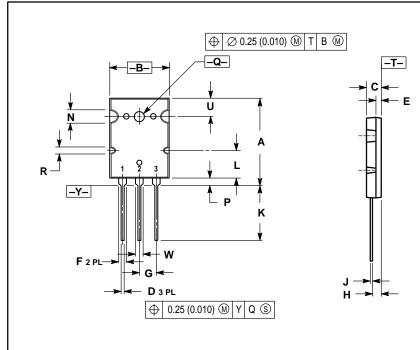


Figure 12. Thermal Response

PACKAGE DIMENSIONS



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 Y14 5M 1982
- 2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	2.8	2.9	1.102	1.142	
В	19.3	20.3	0.760	0.800	
С	4.7	5.3	0.185	0.209	
D	0.93	1.48	0.037	0.058	
Е	1.9	2.1	0.075	0.083	
F	2.2	2.4	0.087	0.102	
G	5.45	BSC 0.215 BSC		BSC	
Н	2.6	3.0	0.102	0.118	
J	0.43	0.78	0.017	0.031	
K	17.6	18.8	0.693	0.740	
L	11.0	11.4	0.433	0.449	
N	3.95	4.75	0.156	0.187	
Р	2.2	2.6	0.087	0.102	
Q	3.1	3.5	0.122	0.137	
R	2.15	2.35	0.085	0.093	
U	6.1	6.5	0.240	0.256	
W	2.8	3.2	0.110	0.125	

STYLE 5:

PIN 1. GATE 2. COLLECTOR

3. EMITTER

CASE 340G-02 TO-264 ISSUE E

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