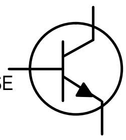
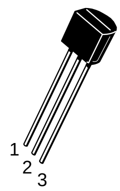
Switching Transistor
NPN Silicon

MPS3646

Motorola Preferred Device





CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	15	Vdc
Collector–Emitter Voltage	V_{CES}	40	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous — 10 µs Pulse	I_C	300 500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = 100 µAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	—	Vdc
Collector–Emitter Sustaining Voltage(1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	15	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 µAdc, I_E = 0)	$V_{(BR)CBO}$	40	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 100 µAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, V_{BE} = 0) (V_{CE} = 20 Vdc, V_{BE} = 0, T_A = 65°C)	I_{CES}	 — —	 0.5 3.0	µAdc

1. Pulse Test: Pulse Width ≤ 300 µs; Duty Cycle ≤ 2.0%.

Preferred devices are Motorola recommended choices for future use and best overall value.

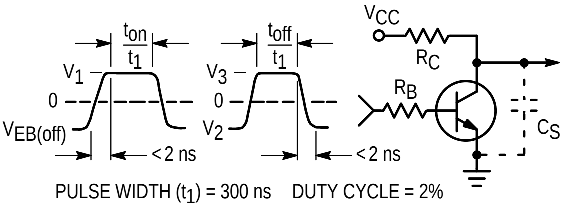
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS[1]					
DC Current Gain	(I_C = 30 mAdc, V_{CE} = 0.4 Vdc) (I_C = 100 mAdc, V_{CE} = 0.5 Vdc) (I_C = 300 mA, V_{CE} = 1.0 Vdc)	h_{FE}	30 25 15	120 — —	—
Collector–Emitter Saturation Voltage	(I_C = 30 mAdc, I_B = 3.0 mAdc) (I_C = 100 mAdc, I_B = 10 mAdc) (I_C = 300 mAdc, I_B = 30 mAdc) (I_C = 30 mA, I_B = 3.0 mA, T_A = 65°C)	$V_{CE(sat)}$	— — — —	0.2 0.28 0.5 0.3	Vdc
Base–Emitter Saturation Voltage	(I_C = 30 mAdc, I_B = 3.0 mAdc) (I_C = 100 mAdc, I_B = 10 mAdc) (I_C = 300 mAdc, I_B = 30 mA)	$V_{BE(sat)}$	0.73 — —	0.95 1.2 1.7	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)		f_T	350	—	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	5.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	9.0	pF
SWITCHING CHARACTERISTICS					
Turn–On Time	(V_{CC} = 10 Vdc, I_C = 300 mAdc, I_{B1} = 30 mAdc) (Figure 1)	t_{on}	—	18	ns
Delay Time		t_d	—	10	ns
Rise Time		t_r	—	15	ns
Turn–Off Time	(V_{CC} = 10 Vdc, I_C = 300 mAdc, I_{B1} = I_{B2} = 30 mAdc) (Figure 1)	t_{off}	—	28	ns
Fall Time		t_f	—	15	ns
Storage Time (V_{CC} = 10 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc) (Figure 2)		t_s	—	18	ns

1. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

Figure 1. Switching Time Equivalent Test Circuit

Test Condition	I_C	V_{CC}	R_S	R_C	$C_{S(max)}$	$V_{BE(off)}$	V_1	V_2	V_3
	mA	V	Ω	Ω	pF	V	V	V	V
A	10	3	3300	270	4	–1.5	10.55	–4.15	10.70
B	10	10	560	960	4	—	—	–4.65	6.55
C	100	10	560	96	12	–2.0	6.35	–4.65	6.55



CURRENT GAIN CHARACTERISTICS

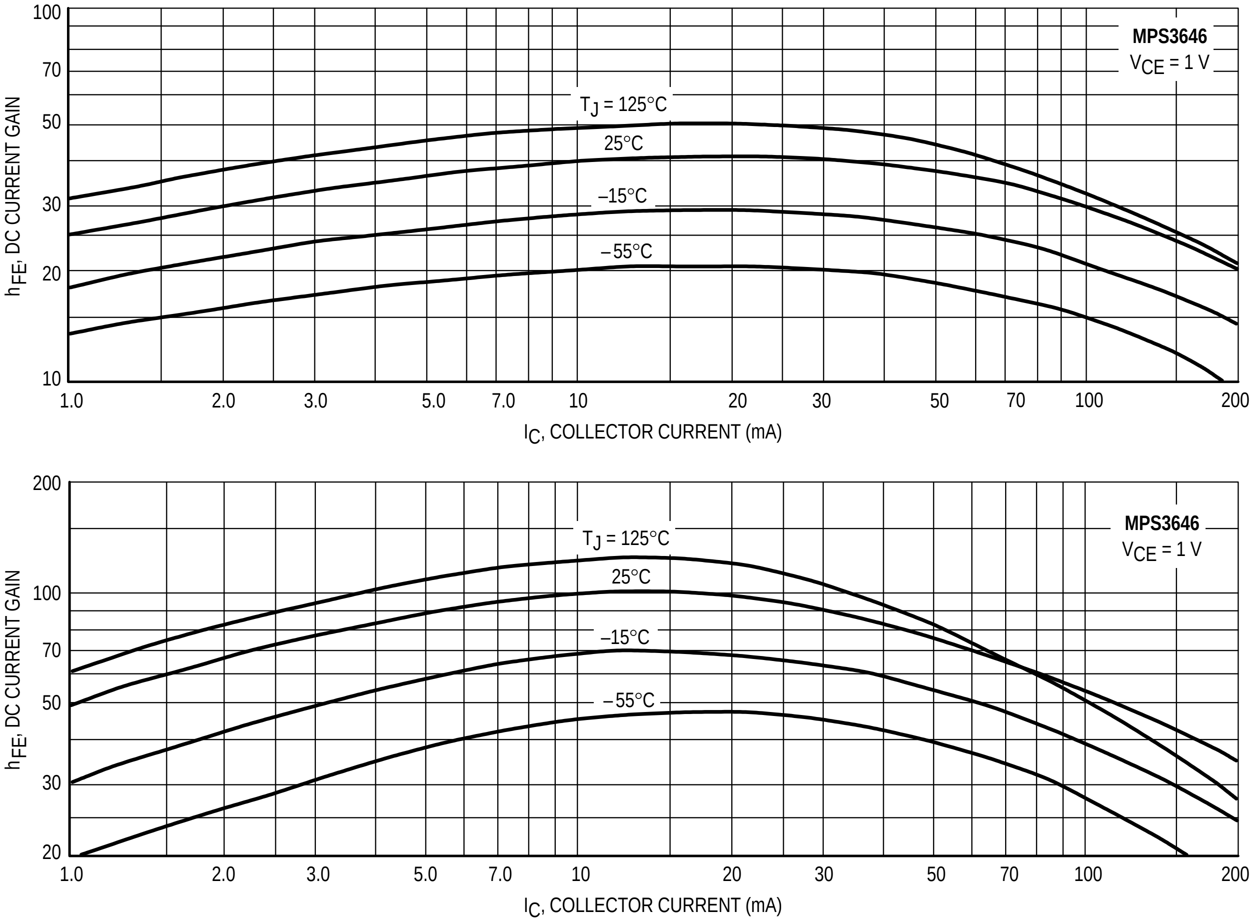


Figure 2. Minimum Current Gain

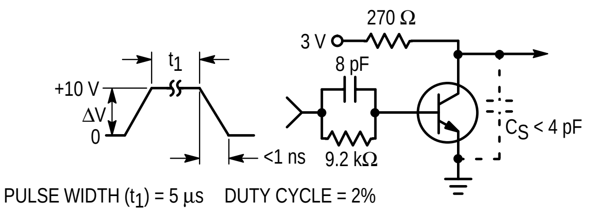


Figure 3. Q_T Test Circuit

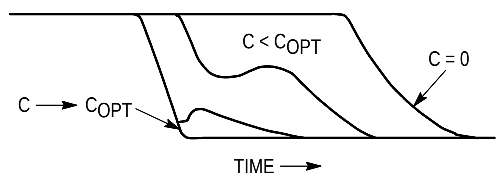


Figure 4. Turn–Off Waveform

NOTE 1

When a transistor is held in a conductive state by a base current, I_B, a charge, Q_S, is developed or “stored” in the transistor. Q_S may be written: $Q_S = Q_1 + Q_V + Q_X$.

Q_1 is the charge required to develop the required collector current. This charge is primarily a function of alpha cutoff frequency. Q_V is the charge required to charge the collector–base feedback capacity. Q_X is excess charge resulting from overdrive, i.e., operation in saturation.

The charge required to turn a transistor “on” to the edge of saturation is the sum of Q_1 and Q_V which is defined as the active region charge, Q_A. $Q_A = I_{B1}t_r$ when the transistor is driven by a constant current step (I_{B1}) and $I_{B1} << \frac{I_C}{h_{FE}}$.

If I_B were suddenly removed, the transistor would continue to conduct until Q_S is removed from the active regions through an external path or through internal recombination. Since the internal recombination time is long compared to the ultimate capability of a transistor, a charge, Q_T, of opposite polarity, equal in magnitude, can be stored on an external capacitor, C, to neutralize the internal charge and considerably reduce the turn–off time of the transistor. Figure 3 shows the test circuit and Figure 4 the turn–off waveform. Given Q_T from Figure 13, the external C for worst–case turn–off in any circuit is: $C = Q_T/\Delta V$, where ΔV is defined in Figure 3.

"ON" CONDITION CHARACTERISTICS

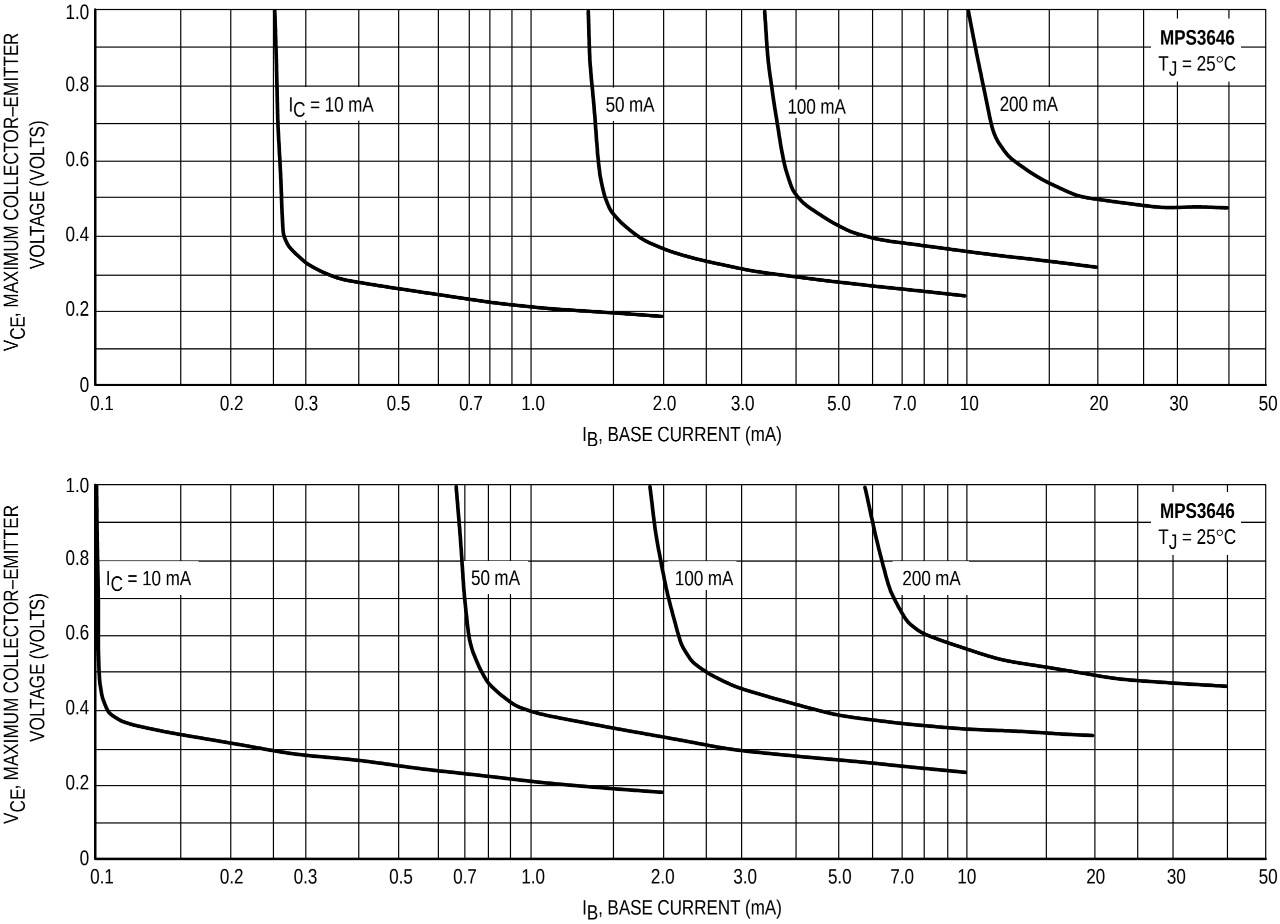


Figure 5. Collector Saturation Region

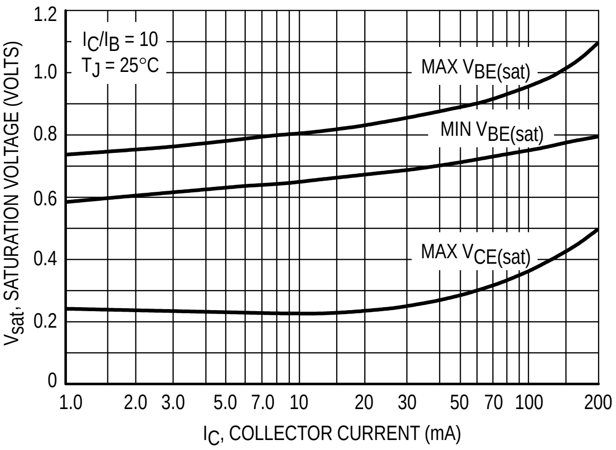


Figure 6. Saturation Voltage Limits

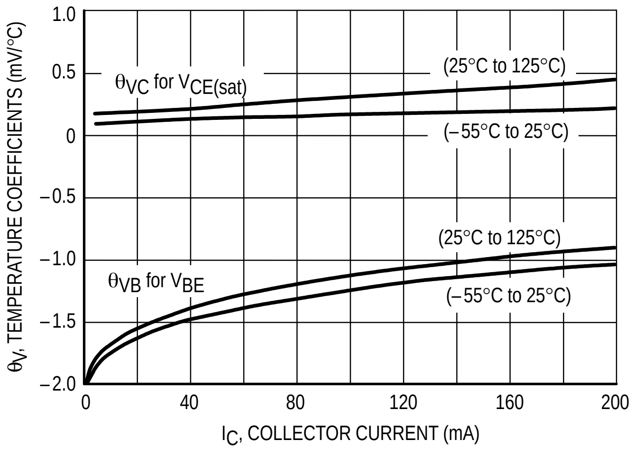


Figure 7. Temperature Coefficients

DYNAMIC CHARACTERISTICS

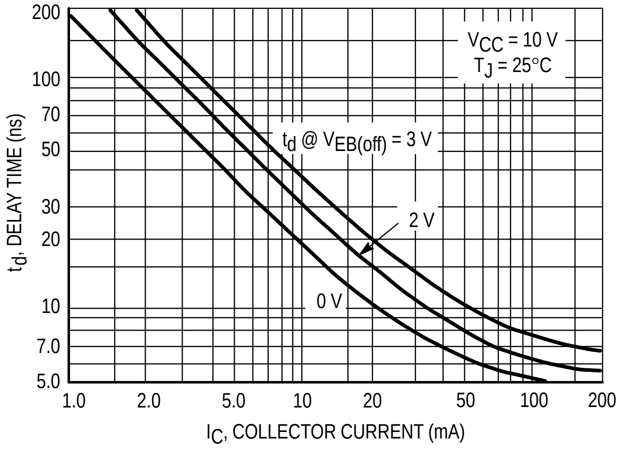


Figure 8. Delay Time

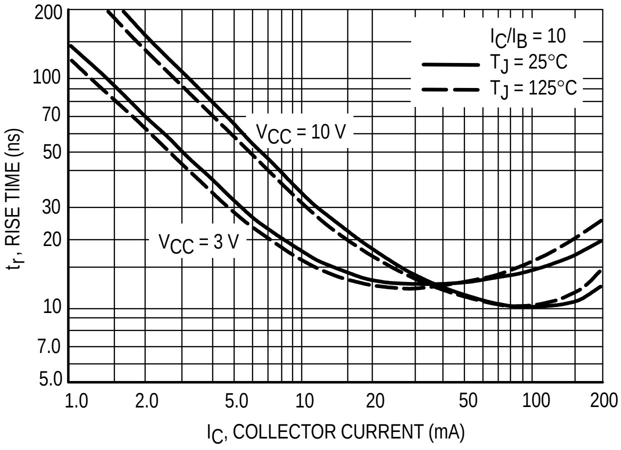


Figure 9. Rise Time

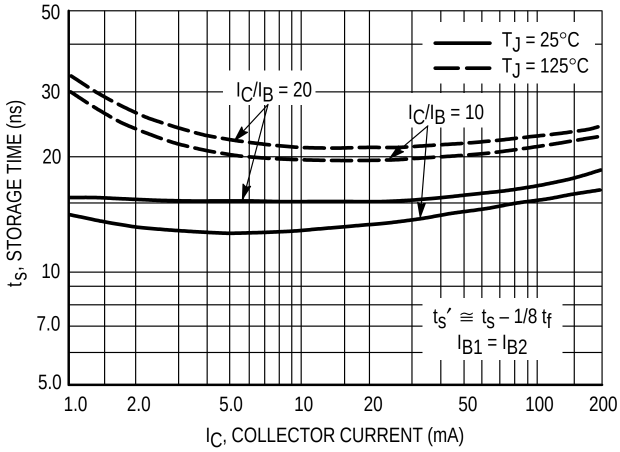


Figure 10. Storage Time

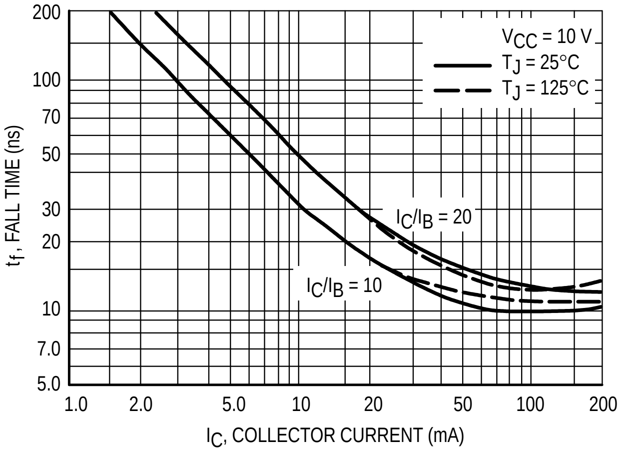


Figure 11. Fall Time

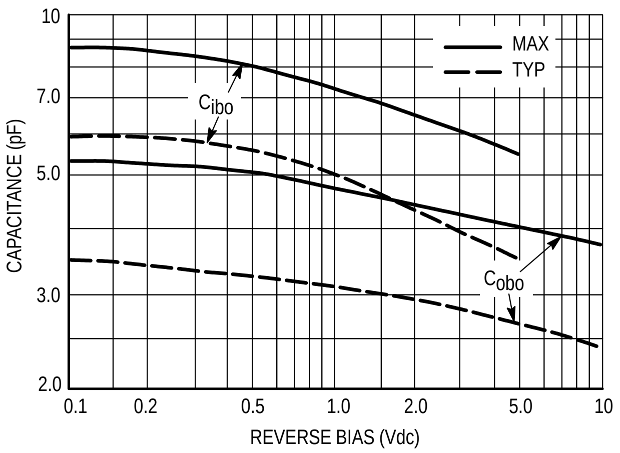


Figure 12. Junction Capacitance

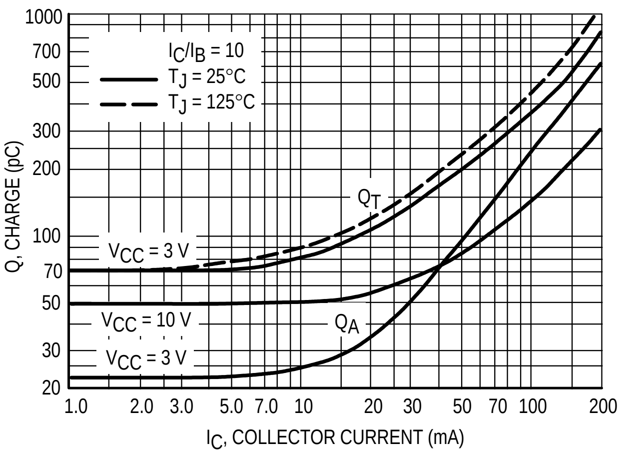
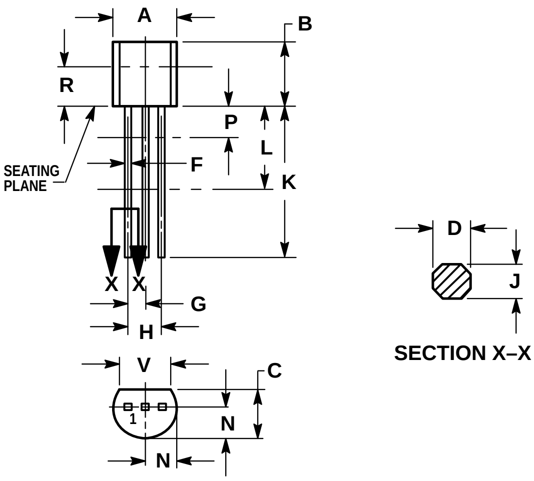


Figure 13. Maximum Charge Data

PACKAGE DIMENSIONS



SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

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