MOTOROLA

MC33365

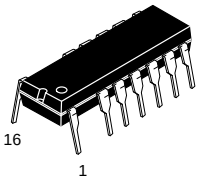
High Voltage Switching Regulator

The MC33365 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.0 A SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, bulk capacitor voltage sensing, and thermal shutdown. This device is available in a 16–lead dual–in–line package.

- On–Chip 700 V, 1.0 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Bulk Capacitor Voltage Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

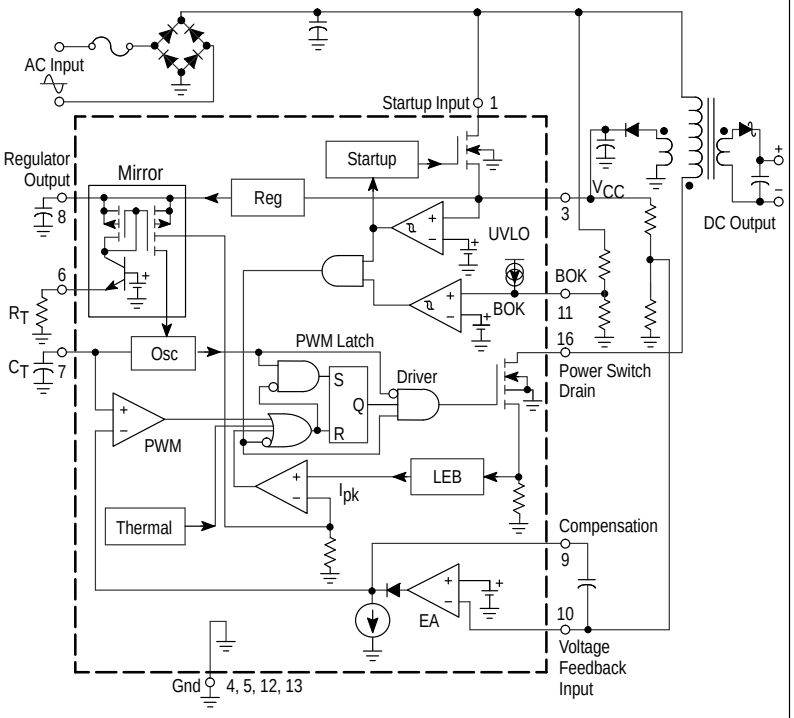
HIGH VOLTAGE OFF–LINE SWITCHING REGULATOR

SEMICONDUCTOR TECHNICAL DATA

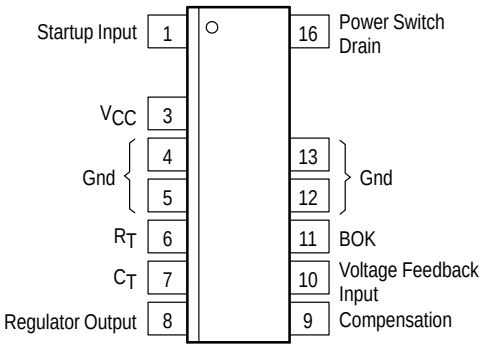


P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

Simplified Application



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33365P	T_J = –25° to +125°C	DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch (Pin 16) Drain Voltage Drain Current	 V_{DS} I_{DS}	 700 1.0	 V A
Startup Input Voltage (Pin 1, Note 1) Pin 3 = Gnd Pin 3 ≤ 1000 μF to ground	V_{in}	 400 500	V
Power Supply Voltage (Pin 3)	V_{CC}	40	V
Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Bulk OK Input (Pin 11) R_T (Pin 6) C_T (Pin 7)	V_{IR}	–1.0 to V_{reg}	V
Thermal Characteristics P Suffix, Dual–In–Line Case 648E Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	 $R_{\theta JA}$ $R_{\theta JC}$	 80 15	°C/W
Operating Junction Temperature	T_J	–25 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 μF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR (Pin 8)					
Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{reg}	5.5	6.5	7.5	V
Line Regulation (V_{CC} = 20 V to 40 V)	Reg_{line}	–	30	500	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	44	200	mV
Total Output Variation over Line, Load, and Temperature	V_{reg}	5.3	–	8.0	V
OSCILLATOR (Pin 7)					
Frequency C_T = 390 pF T_J = 25°C (V_{CC} = 20 V) T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V) C_T = 2.0 nF T_J = 25°C (V_{CC} = 20 V) T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)	f_{OSC}	 260 255 60 59	 285 – 67.5 –	 310 315 75 76	kHz
Frequency Change with Voltage (V_{CC} = 20 V to 40 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	2.0	kHz
ERROR AMPLIFIER (Pins 9, 10)					
Voltage Feedback Input Threshold	V_{FB}	2.52	2.6	2.68	V
Line Regulation (V_{CC} = 20 V to 40 V, T_J = 25°C)	Reg_{line}	–	0.6	5.0	mV
Input Bias Current (V_{FB} = 2.6 V, T_J = 0 – 125°C)	I_{IB}	–	20	500	nA
Open Loop Voltage Gain (T_J = 25°C)	A_{VOL}	70	82	94	dB
Gain Bandwidth Product (f = 100 kHz, T_J = 25°C)	GBW	0.85	1.0	1.15	MHz
Output Voltage Swing High State (I_{Source} = 100 μA, V_{FB} < 2.0 V) Low State (I_{Sink} = 100 μA, V_{FB} > 3.0 V)	 V_{OH} V_{OL}	 4.0 –	 5.3 0.2	 – 0.35	V

NOTES: 1. Maximum power dissipation limits must be observed.
2. Tested junction temperature range for the MC33363B:
T_{low} = –25°C T_{high} = +125°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 μF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
BULK OK (Pin 11)					
Input Threshold Voltage	V_{th}	1.18	1.25	1.32	V
Input Bias Current ($V_{BK} < V_{th}$, T_J = 0 – 125°C)	I_{IB}	–	100	500	nA
Source Current (Turn on after $V_{BK} > V_{th}$, T_J = 25°C – 125°C)	I_{SC}	39	–	53	μA
PWM COMPARATOR (Pins 7, 9)					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{FB} = 2.7 V)	 $DC_{(max)}$ $DC_{(min)}$	 48 –	 50 0	 52 0	%
POWER SWITCH (Pin 16)					
Drain–Source On–State Resistance (I_D = 200 mA) T_J = 25°C $T_J = T_{low}$ to T_{high}	$R_{DS(on)}$	 – –	 15 –	 17 39	Ω
Drain–Source Off–State Leakage Current V_{DS} = 650 V	$I_{D(off)}$	 –	 0.2	 100	μA
Rise Time	t_r	–	50	–	ns
Fall Time	t_f	–	50	–	ns
OVERCURRENT COMPARATOR (Pin 16)					
Current Limit Threshold (R_T = 10 k)	I_{lim}	0.5	0.72	0.9	A
STARTUP CONTROL (Pin 1)					
Peak Startup Current (V_{in} = 400 V) (Note 3) V_{CC} = 0 V $V_{CC} = (V_{th(on)} - 0.2\ V)$	I_{start}	 – –	 2.0 2.0	 4.0 4.0	mA
Off–State Leakage Current (V_{in} = 50 V, V_{CC} = 20 V)	$I_{D(off)}$	–	40	200	μA
UNDERVOLTAGE LOCKOUT (Pin 3)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11	15.2	18	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.5	9.5	11.5	V
TOTAL DEVICE (Pin 3)					
Power Supply Current Startup (V_{CC} = 10 V, Pin 1 Open) Operating	I_{CC}	 – –	 0.25 3.2	 0.5 5.0	mA

NOTES: 3. The device can only guarantee to start up at high temperature below +115°C.

Figure 1. Oscillator Frequency versus Timing Resistor

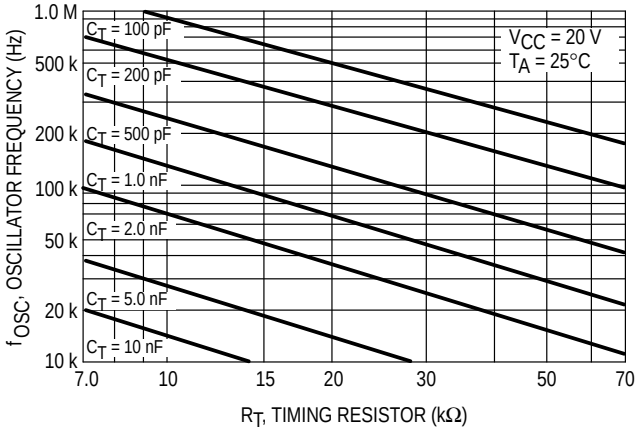


Figure 2. Power Switch Peak Drain Current versus Timing Resistor

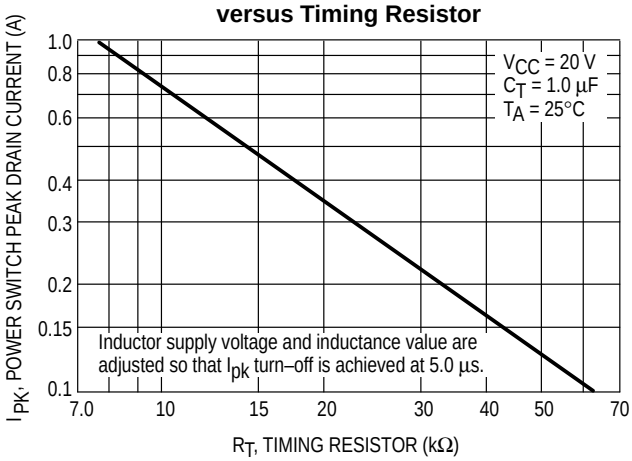


Figure 3. Oscillator Charge/Discharge Current versus Timing Resistor

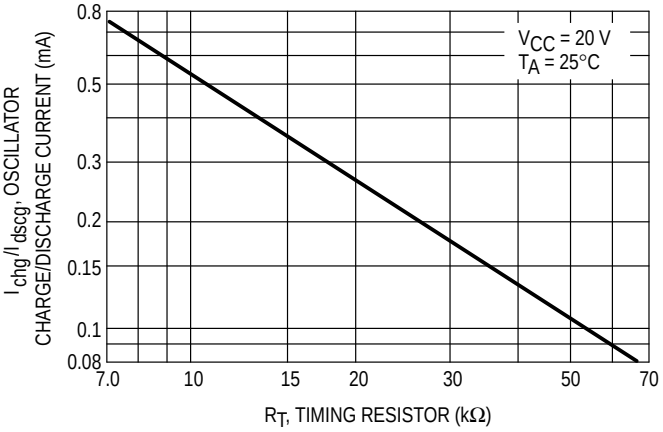


Figure 4. Maximum Output Duty Cycle versus Timing Resistor Ratio

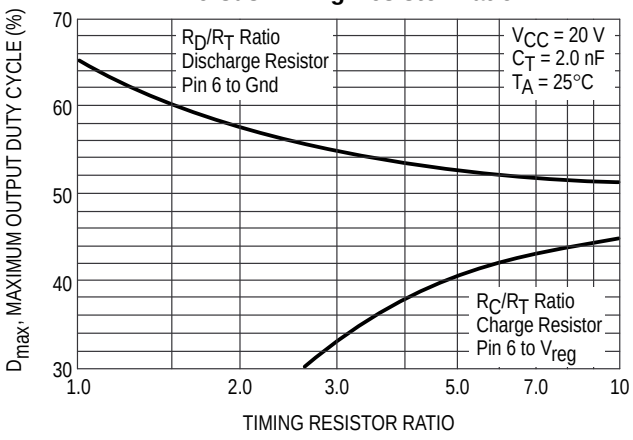


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

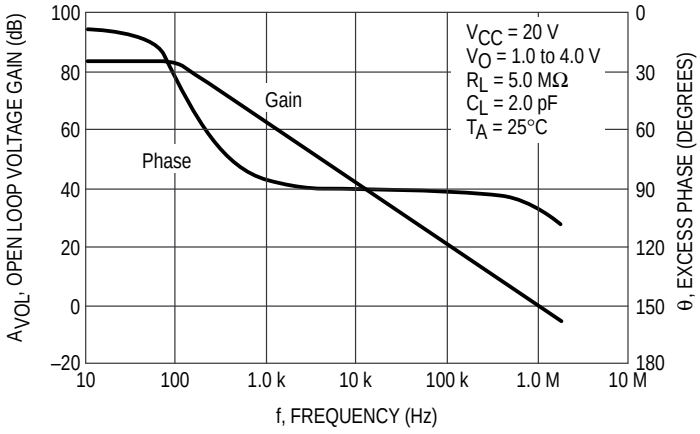


Figure 6. Error Amp Output Saturation Voltage versus Load Current

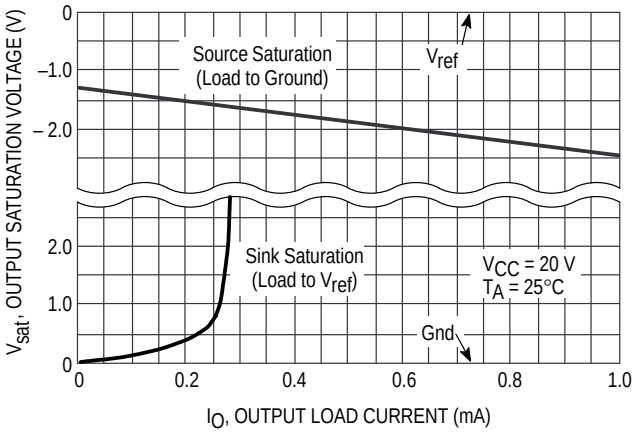


Figure 7. Error Amplifier Small Signal Transient Response

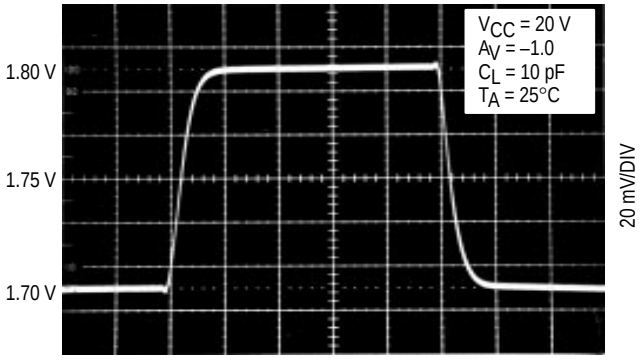


Figure 8. Error Amplifier Large Signal Transient Response

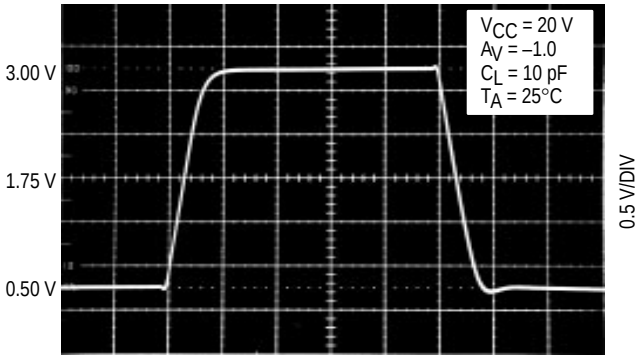


Figure 9. Regulator Output Voltage Change versus Source Current

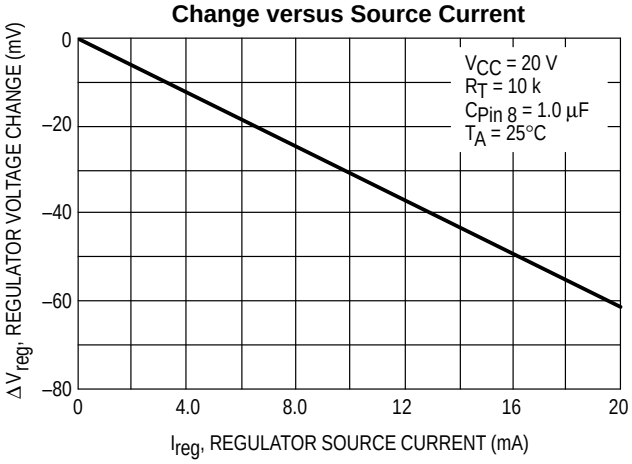


Figure 10. Peak Startup Current versus Power Supply Voltage

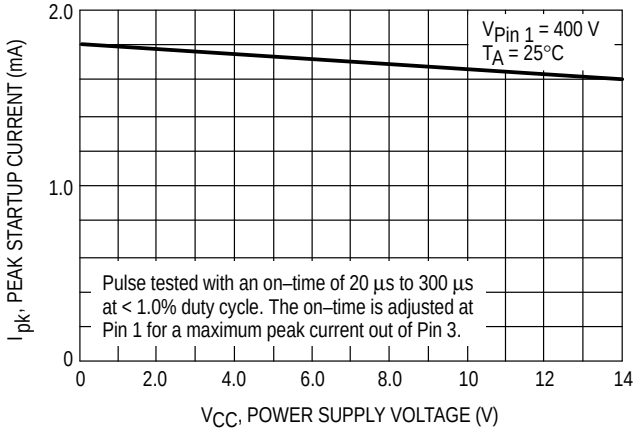


Figure 11. Power Switch Drain–Source On–Resistance versus Temperature

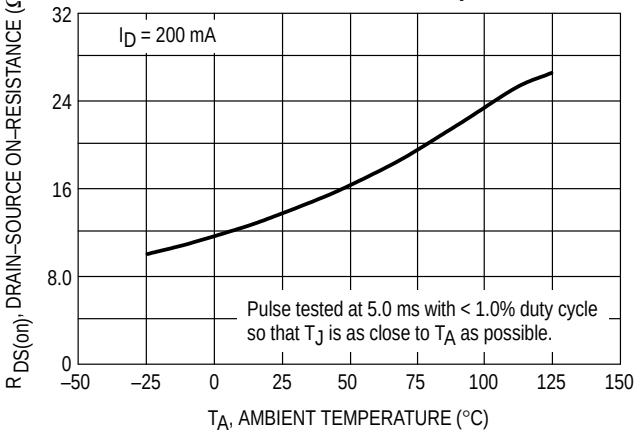


Figure 12. Power Switch Drain–Source Capacitance versus Voltage

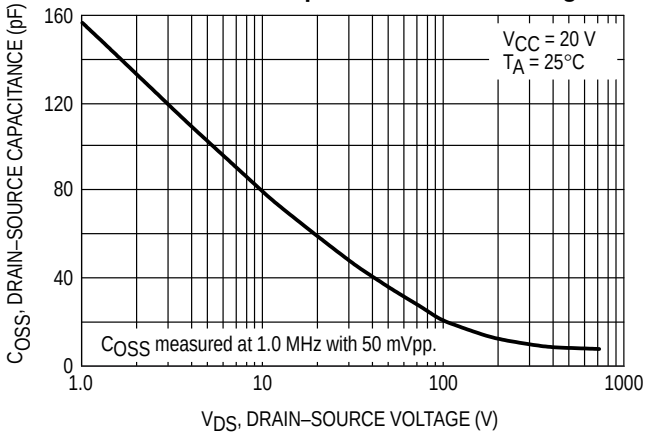


Figure 13. Supply Current versus Supply Voltage

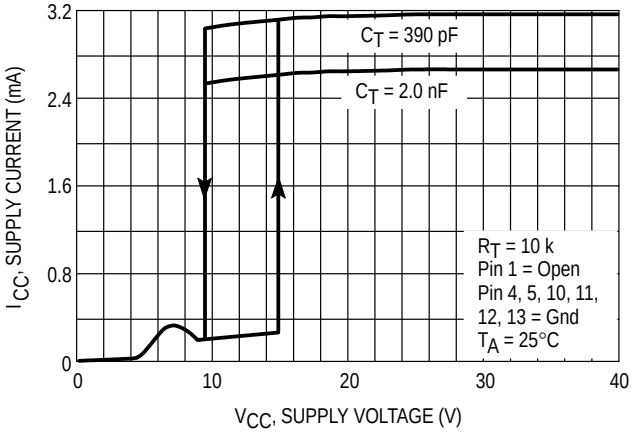


Figure 14. DW and P Suffix Transient Thermal Resistance

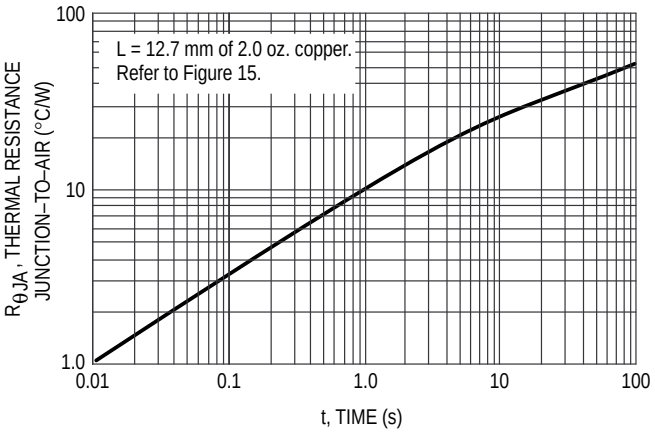
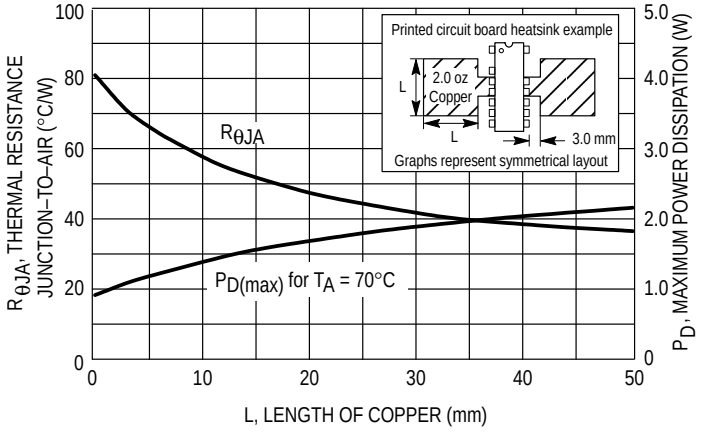


Figure 15. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Startup Input	This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the V_{CC} pin to ground.
2	–	This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the V_{CC} potential on Pin 3.
3	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When V_{CC} reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding.
4, 5, 12, 13	Ground	These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board.
6	R_T	Resistor R_T connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency.
7	C_T	Capacitor C_T connects from this pin to ground. The value selected, in conjunction with resistor R_T, programs the Oscillator frequency.
8	Regulator Output	This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least 1.0 μF for stability.
9	Compensation	This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator.
10	Voltage Feedback Input	This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
11	Bulk OK Input	This is the non–inverting input of the bulk capacitor voltage comparator. It has an input threshold voltage of 1.25V. This pin is connected through a resistor divider to the bulk capacitor line voltage.
14, 15	–	These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13.
16	Power Switch Drain	This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A.

Figure 16. Representative Block Diagram

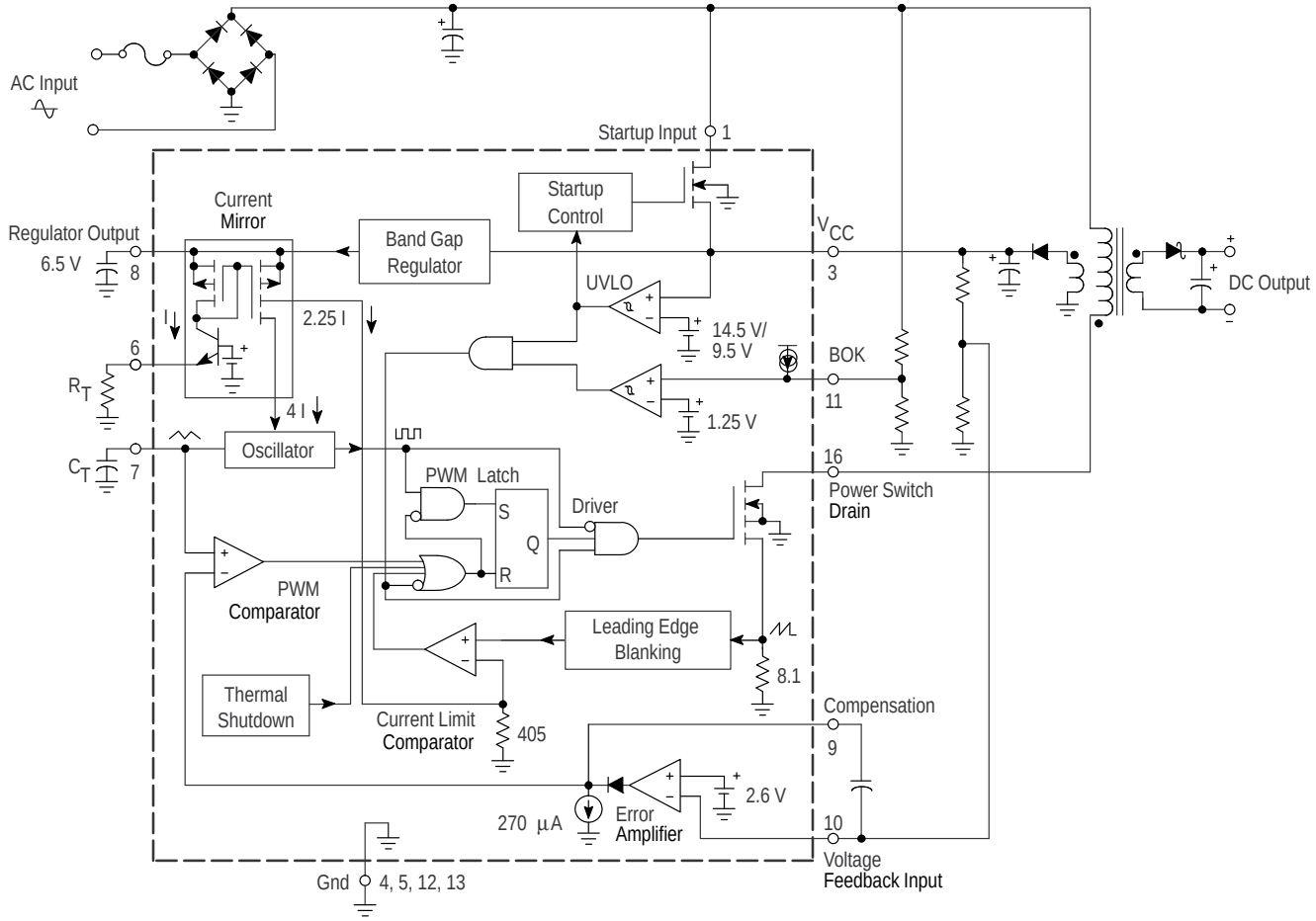
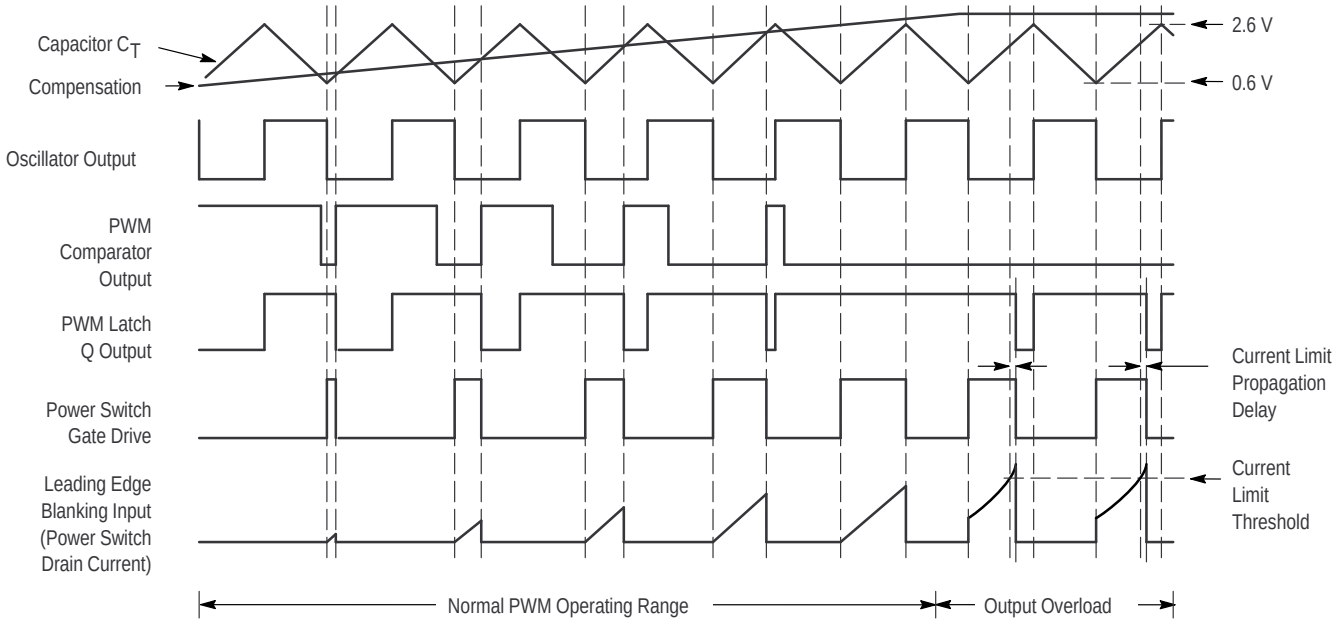


Figure 17. Timing Diagram



OPERATING DESCRIPTION

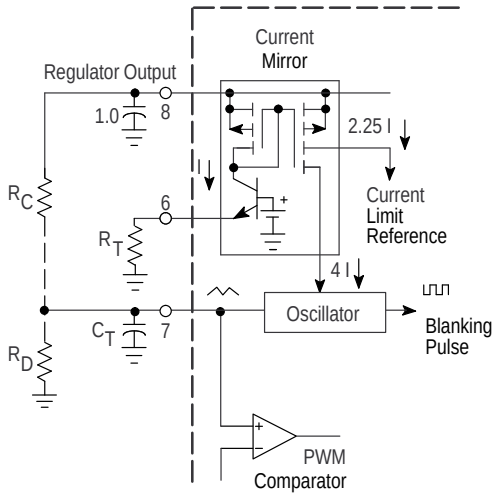
Introduction

The MC33365 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 16 and 17.

Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components R_T and C_T. Resistor R_T programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 3. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz. The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50% limit by providing an additional charge or discharge current path to C_T, Figure 18. In order to increase the maximum duty cycle, a discharge current resistor R_D is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor R_C is connected from Pin 7 to the Regulator Output. Figure 4 shows an obtainable range of maximum output duty cycle versus the ratio of either R_C or R_D with respect to R_T.

Figure 18. Maximum Duty Cycle Modification



The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for C_T values greater than 500 pF. For smaller values of C_T, refer to Figure 1. Note that resistor R_T also programs the Current Limit Comparator threshold.

$$I_{chg/dscg} = \frac{5.4}{R_T} \qquad f \approx \frac{I_{chg/dscg}}{4C_T}$$

PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non–inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while C_T is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When C_T charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp–up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 17 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

Current Limit Comparator and Power Switch

The MC33365 uses cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1462 cells, of which 36 are connected to a 8.1 Ω ground–referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the 405 Ω resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor R_T. Therefore when selecting the values for R_T and C_T, R_T must be chosen first to set the Power Switch peak drain current, while C_T is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus R_T is shown in Figure 2 with the related formula below.

$$I_{pk} = 8.8 \left(\frac{R_T}{1000} \right) - 1.077$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A. Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn–on transition is completed. The current limit propagation delay time is typically 262 ns. This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn–off.

Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 16. It features a typical dc voltage gain of 82 dB, and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 5. The noninverting input is internally biased at 2.6 V ±3.1% and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of 270 μA, allowing it to be easily overridden with a pull–up resistor. This is desirable in applications that require secondary side voltage sensing.

Bulk Capacitor Voltage Comparator

The Bulk Capacitor Voltage Comparator is included to sense the brown–out condition of the bulk capacitor line voltage. The non–inverting input, Pin 11, is connected to the voltage divider to sense the line voltage. The inverting input is connected internally to a threshold voltage of 1.25V. As the line voltage drops below 120V (Pin 11 drops below 1.25V), the reset signal is activiated from the PWM Latch to turn off the Power Switch. To prevent erratic switching as the threshold is crossed, hysteresis at Pin 11 is provided.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the V_{CC} voltage at Pin 3 and when it exceeds 14.5 V, the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33365. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off–line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the V_{CC} bypass capacitor that connects from Pin 3 to ground. When V_{CC} reaches the UVLO upper threshold of 15.2 V, the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide a steady current of 1.7 mA, Figure 10, as V_{CC} increases or shorted to ground. The startup MOSFET is rated at a maximum of 400 V with V_{CC} shorted to ground, and 500 V when charging a V_{CC} capacitor of 1000 μF or less.

Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short–circuit protection. This output requires an external bypass capacitor of at least 1.0 μF for stability.

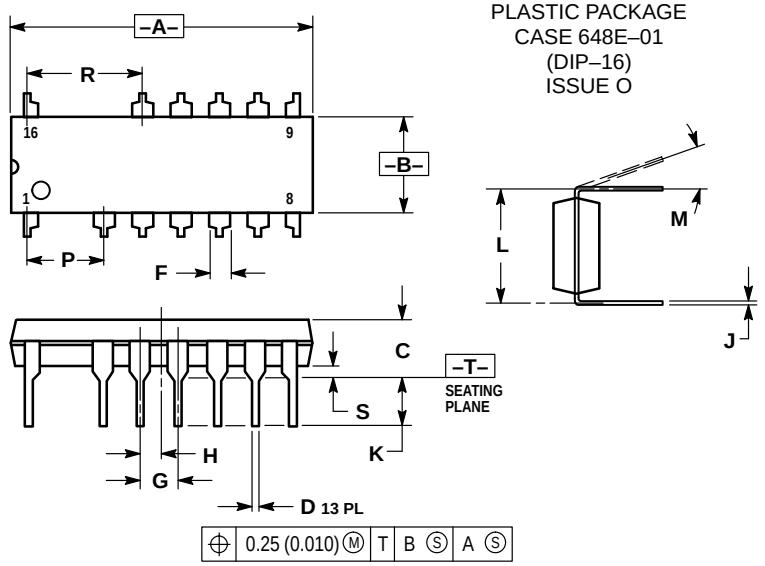
Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at 150°C, the Latch is forced into a ‘reset’ state, disabling the Power Switch. The Latch is allowed to ‘set’ when the Power Switch temperature falls below 140°C. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33365 is contained in a heatsinkable plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figure 15 shows a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 648E–01
(DIP–16)
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNER OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.760	18.80	19.30
B	0.245	0.260	6.23	6.60
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.120	0.140	3.05	3.55
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
P	0.200 BSC		5.08 BSC	
R	0.300 BSC		7.62 BSC	
S	0.015	0.035	0.39	0.88

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan. 81–3–5487–8488

Customer Focus Center: 1–800–521–6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
852–26629298

HOME PAGE: http://motorola.com/sps/