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MOTOROLA

MC33565

Smart Voltage Regulator for Peripheral Card Applications

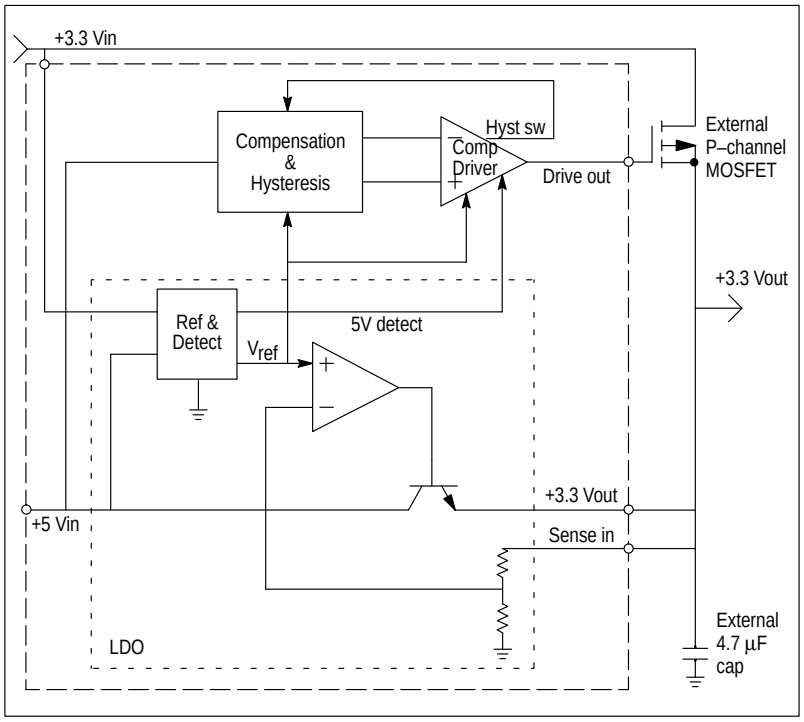
The MC33565 Low Dropout Regulator is designed for computer peripheral card applications complying with the *instantly available requirements* as specified by ACPI objectives. The MC33565 permits glitch–free transitions from “sleep” to “active” system modes and has internal logic circuitry to detect whether the system is being powered from the motherboard main 5V power supply or the 3.3V aux supply.

The MC33565 provides a regulated output voltage of 3.3V via either an internal low drop out 5.0V–to–3.3V voltage regulator or an external P–channel MOSFET, depending on the operating status of the system in which the card is installed. During normal operating mode (5V main supply available) the 3.3V output is provided from the internal low dropout regulator at an output current of 200mA. When the motherboard enters sleep mode, the MC33565 operates from the 3.3V aux supply and routes the aux current to the output via the external P–channel MOSFET bypass transistor controlled by the *drive out* pin. As a result, the output voltage provided to the peripheral card remains constant at 3.3V even during transitions to and from sleep mode.

MC33565 Features:

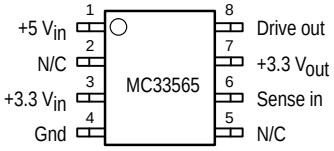
- Output Regulated to 2% Over Temperature
- Output current up to 200mA
- Excellent Line and Load Regulation
- Low Dropout Voltage
- Prevents reverse current flow during sleep mode
- Glitch–free transfer from sleep mode to active mode
- Compatible with *Instantly Available* PC systems
- Evaluation Kit Available: (P.N. MC33565EVK)

Simplified Block Diagram



200 mA INTELLIGENT LDO REGULATOR WITH SMART BYPASS CONTROL

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751–06
(SO–8)

Pins 2 and 5 Not Connected

ORDERING INFORMATION

Device	Type	Package
MC33565D	3.3V	SO–8

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Max Value	Unit
Input Voltage, V_{CC}	V_{max}	7.0	Vdc
	V_{min}	–0.5	Vdc
Operating Ambient Temperature	T_a	–5 to +70	°C
Operating Junction Temperature	T_J	– 5 to +150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$[1]	180	°C/W

NOTES: 1. Mounted on recommended minimum PCB pad on FR4, 2–oz. copper circuit board.

AC ELECTRICAL SPECIFICATIONS(3) (4)

Parameter	Symbol	Min	Typ	Max	Unit
Drive High Delay (V_{in} ramping up) C_{Drive} = 1.2 nF, measured from +5 V_{in} = $V_{thresHi}$ to V_{Drive} = 2V	t_{DH}		0.5	3.5	µS
Drive Low Delay (V_{in} ramping down) C_{Drive} = 1.2 nF, measured from +5 V_{in} = $V_{thresLo}$ to V_{Drive} = 2V	t_{DL}		0.5	3.5	µS

NOTES: (1.) See 5V Detect Thresholds Diagram.
(2.) Recommended source impedance for 5V supply: ≤ 0.25Ω. This will ensure that I_O x R_{source} < V_{hyst}, thus avoiding driveout toggling during 5V detect threshold transitions.
(3.) See Figure 2. Application Block Diagram.
(4.) See Timing Diagram.

PIN ASSIGNMENTS AND FUNCTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	+5 V_{in}	This is the input supply for the IC. Typical voltage 5 V. (1) (2)
2,5	N/C	Reserved
3	+3.3 V_{in}	Auxiliary input. Typical voltage 3.3 V.
4	Gnd	Logic and Power Gnd.
6	Sense in	Load–sense voltage input to internal regulator.
7	+3.3 V_{out}	3.3V output provided to the application circuit (output current is sourced to this pin from the 5V input.)
8	Drive out	This output drives a P–channel MOSFET with up to 2000pF of “effective” gate capacitance. Recommended device is MGSF1P02ELT MOSFET. Drive out has active internal pull–up and pull–down circuitry to guarantee fast transitions.

DEVICE MARKING

Device	Type	Sub–type	Marking (1st Line)
MC33565D	3.3 V		MC565

DC ELECTRICAL CHARACTERISTICS(1)

Characteristic	Symbol	Min	Typ	Max	Unit
+5 V_{in} Supply Voltage Range	+5 V_{in}	4.3	5.0	5.5	Vdc
Reverse Leakage Current from Output	$I_{reverse}$	—	—	25	μA
V_{Aux} quiescent current		—	—	3.0	mA
+5 V_{in} quiescent current, operating		—	—	10	mA
Load Capacitance(2)	C_{load}	4.7	22	—	μF
REGULATOR OUTPUT					
Output Voltage (4.3V ≤ V_{in} ≤ 5.5V, 0mA ≤ I_O ≤ 200mA) T_A = 25°C (T_A = –5°C to 150°C)	+3.3 V_{out}	 3.267 3.234	 3.30 3.30	 3.333 3.366	Vdc
In–to–Out Voltage (3.9V ≤ V_{in} ≤ 4.3V, V_{aux} = 3.3V)	V_d	3.0	—	—	Vdc
Voltage Out at Max Voltage In (V_{in} = 7V)	V_{outmax}	3.1	3.3	3.5	Vdc
Line Regulation (I_O = 200 mA)		—	—	0.4	%
Load Regulation (I_O = 0 to 200 mA)		—	—	0.4	%
5V DETECT					
Low Threshold Voltage (+5 V_{in} falling)	$V_{thresLo}$	3.9	4.05	4.3	Vdc
High Threshold Voltage (+5 V_{in} rising)	$V_{thresHi}$	—	4.2	4.3	Vdc
Hysteresis	V_{Hyst}	0.12	0.15	0.18	Vdc
DRIVE OUTPUT					
Output peak source Current (+5 V_{in} > $V_{thresHi}$)	I_{peak}	15	—	—	mA
Output peak sink Current (+5 V_{in} < $V_{thresLo}$)	I_{peak}	15	—	—	mA
Low Output Voltage (I_{oL} = 200 μA, V_{in} < $V_{thresLo}$)	V_{oL}	—	100	200	mVdc
High Output Voltage (I_{oH} = 200 μA)	V_{oH}	3.4	V_5–0.8	—	Vdc

NOTE: 1. (–5°C<T_a<70°C, 4.3V<5V<5.5V, C_{load} = 4.7μF unless otherwise noted)
NOTE: 2. 4.7μF minimum over temperature; 22μF recommended; 500mΩ ESR maximum.

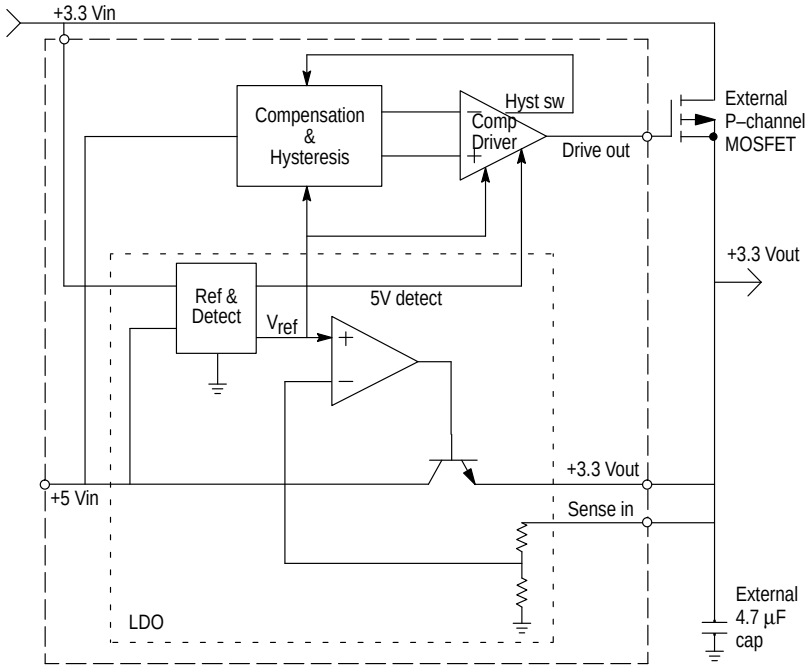


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Input Blocking – The internal NPN pass transistor of the LDO regulator ensures that no significant reverse current will flow from +3.3 V_{out} back to the +5 V_{in} input when the 5V input is not powered and the 3.3 V_{in} supply is present.

5 Volt Detect – Internal circuitry detects the presence of the 5V input supply. When the 5V supply drops below a given threshold, the +3.3 V_{in} bypass transistor (an external P–channel MOSFET) is enabled. The 5V detect logic is active throughout the entire range of ramp–up from 0 to 5.5V. Additionally, the Drive out signal is never turned ON or OFF inappropriately during ramp–up of the +5 V_{in} supply. Also, +3.3 V_{out} never drops below 3.0V while +5 V_{in} is above the 5V detect minimum threshold.

Glitch–free Transfer – The design of the 5V detect circuitry and Drive out control circuitry guarantees that the +3.3 V_{out} will not exceed the output voltage specification listed in the table of DC Operating Specifications even with +5 V_{in} ramping up and down at the extremes of the slew rates in the table of AC Operating Specifications (provided the device is used with an MGSF1P02ELT PMOS FET on Drive out along with a minimum 4.7µF capacitor on the +3.3 V_{out}).

Offset Voltage Performance – To ensure performance when external offsets are present on the +5 V_{in} and +3.3 V_{in} power inputs, the device has been designed to be capable of operating with either one or both of these inputs rising from or falling to zero volts, or with offsets of 0.05V to 0.9V as the inputs ramp up and down.

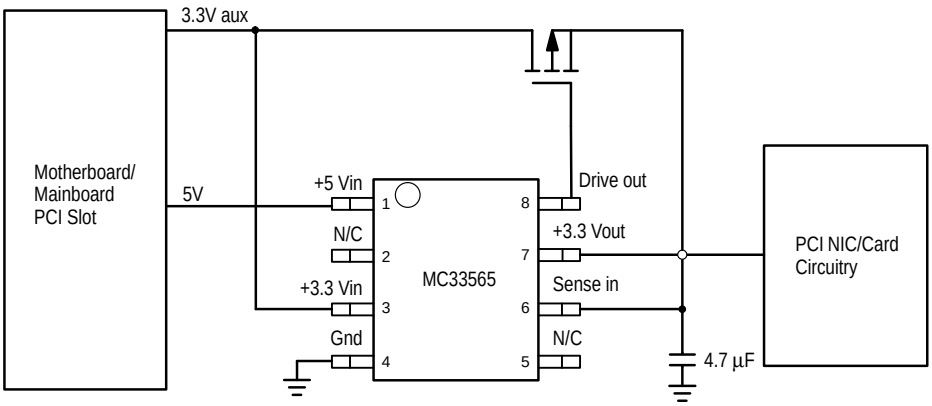
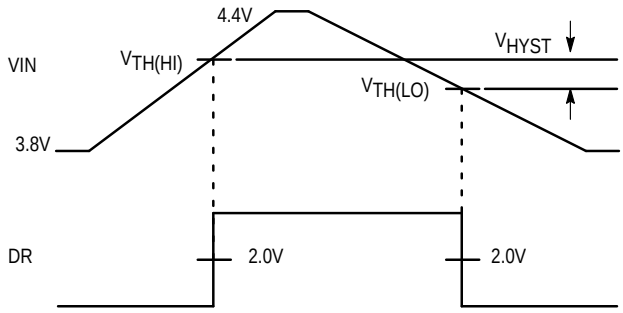
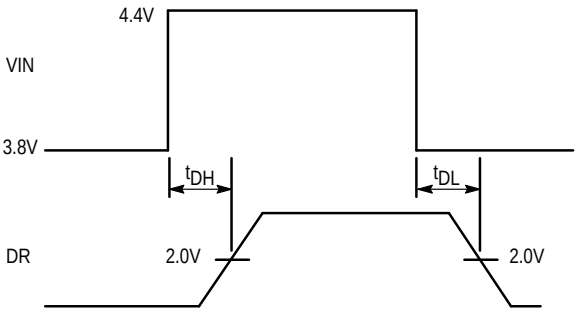


Figure 2. Application Block Diagram



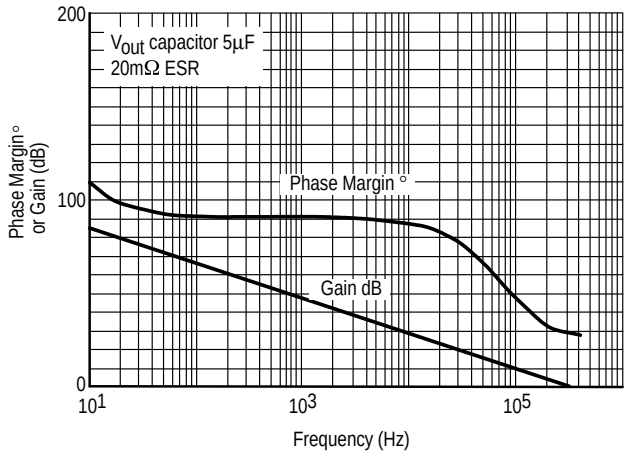
NOTE:
(1) VIN rise and fall times (10% to 90%) to be ≥ 100µs.

Figure 3. 5V Detect Thresholds Diagram



NOTE:
(1) VIN rise and fall times (10% to 90%) to be ≤ 100ns.

Figure 4. Timing Diagram



NOTE: V_{out} capacitor ≥ 4.7µF over operating temperature range.
Maximum ESR permissable = 500mΩ over operating temperature range.

Figure 5. Predicted Gain and Phase at Zero Load Current

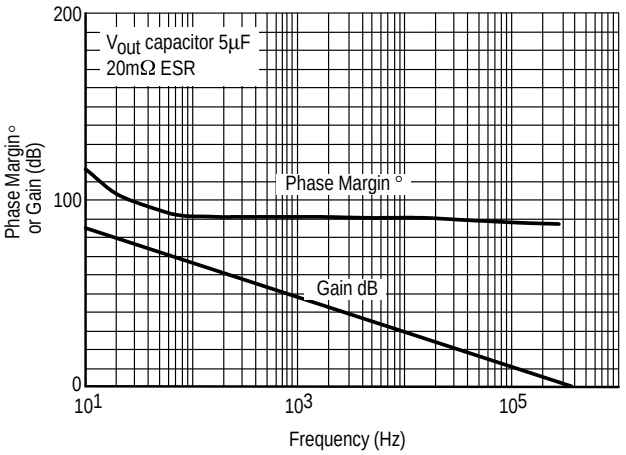
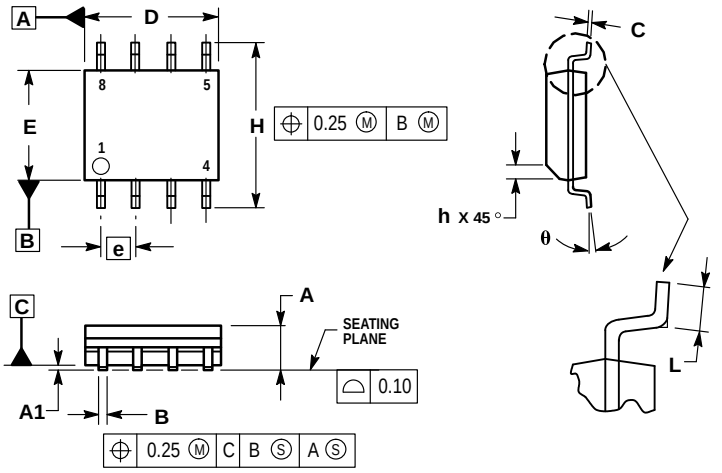


Figure 6. Predicted Gain and Phase at Full Load Current

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC PACKAGE
CASE 751–06
(SO–8)
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0 °	7 °

NOTES

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