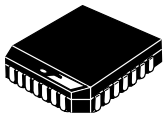
8-Bit Ripple Counter

MC10E137
MC100E137

8-BIT RIPPLE COUNTER

The MC10E/100E137 is a very high speed binary ripple counter. The two least significant bits were designed with very fast edge rates while the more significant bits maintain standard ECLinPS™ output edge rates. This allows the counter to operate at very high frequencies while maintaining a moderate power dissipation level.

- 1.8GHz Minimum Count Frequency
- Differential Clock Input and Data Output Pins
- V_{BB} Output for Single-Ended Use
- Internal 75kΩ Input Pulldown Resistors
- Synchronous and Asynchronous Enable Pins
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of –4.2V to –5.46V



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The device is ideally suited for multiple frequency clock generation as well as a counter in a high performance ATE time measurement board.

Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted enables the counter while overriding any synchronous enable signals. The E137 features XORed enable inputs, EN1 and EN2, which are synchronous to the CLK input. When only one synchronous enable is asserted the counter becomes disabled on the next CLK transition; all outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. If EN1 (or EN2) and CLK edges are coincident, sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip flop setup time) to insure that the synchronous enable signal is clocked correctly, hence, the counter is disabled.

The E137 can also be driven single-endedly utilizing the V_{BB} output supply as the voltage reference for the CLK input signal. If a single-ended signal is to be used the V_{BB} pin should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. V_{BB} can only source/sink 0.5mA, therefore it should be used as a switching reference for the E137 only.

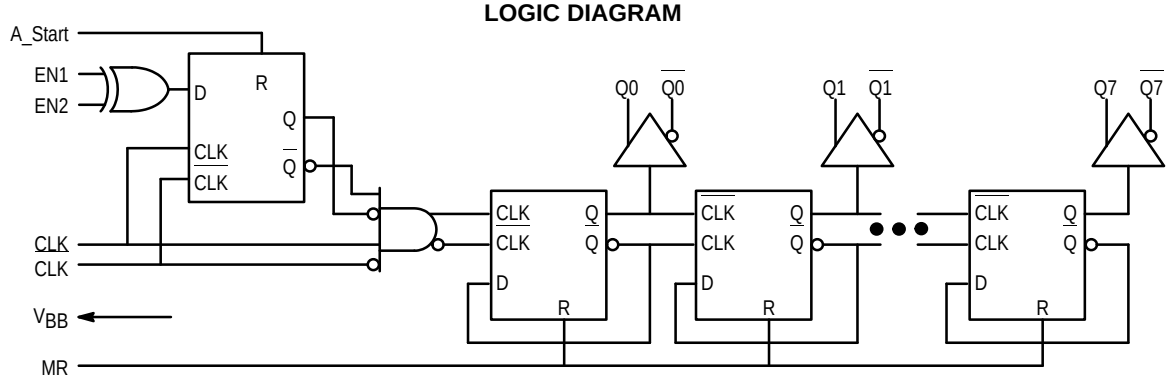
PIN NAMES

PIN	FUNCTION
CLK, $\overline{CLK}$	Differential Clock Inputs
Q0-Q7, $\overline{Q0}$-$\overline{Q7}$	Differential Q Outputs
A_Start	Asynchronous Enable Input
EN1, EN2	Synchronous Enable Inputs
MR	Asynchronous Master Reset
V_{BB}	Switching Refernce Output

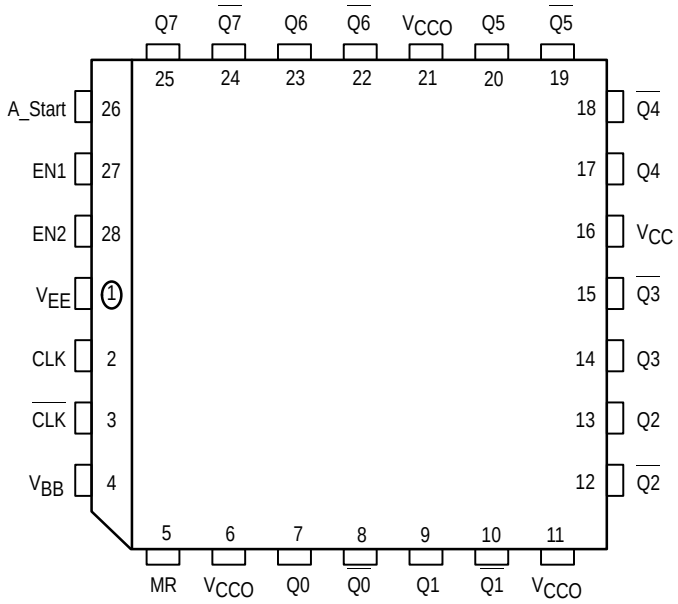
All input pins left open will be pulled LOW via an input pulldown resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

LOGIC DIAGRAM



Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

SEQUENTIAL TRUTH TABLE

Function	EN1	EN2	A_Start	MR	CLK	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L
Count	L	L	L	L	Z	L	L	L	L	L	L	L	H
	L	L	L	L	Z	L	L	L	L	L	L	H	L
	L	L	L	L	Z	L	L	L	L	L	L	H	H
Stop	H	L	L	L	Z	L	L	L	L	L	L	H	H
	H	L	L	L	Z	L	L	L	L	L	L	H	H
Asynch Start	H	L	H	L	Z	L	L	L	L	L	H	L	L
	H	L	H	L	Z	L	L	L	L	L	H	L	H
	L	L	H	L	Z	L	L	L	L	L	H	H	L
Count	L	L	L	L	Z	L	L	L	L	L	H	H	H
	L	L	L	L	Z	L	L	L	L	H	L	L	L
	L	L	L	L	Z	L	L	L	L	H	L	L	H
Stop	L	H	L	L	Z	L	L	L	L	H	L	L	H
	L	H	L	L	Z	L	L	L	L	H	L	L	H
Synch Start	H	H	L	L	Z	L	L	L	L	H	L	H	L
	H	H	L	L	Z	L	L	L	L	H	L	H	H
	H	H	L	L	Z	L	L	L	L	H	H	L	L
Stop	H	L	L	L	Z	L	L	L	L	H	H	L	L
	H	L	L	L	Z	L	L	L	L	H	H	L	L
Count	L	L	L	L	Z	L	L	L	L	H	H	L	H
	L	L	L	L	Z	L	L	L	L	H	H	H	L
	L	L	L	L	Z	L	L	L	L	H	H	H	H
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L

Z = Low to High Transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage										V	
	10E	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19		
	100E	–1.38		–1.27	–1.38		–1.26	–1.38		–1.26		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		121	145		121	145		121	145		
	100E		121	145		121	145		139	167		

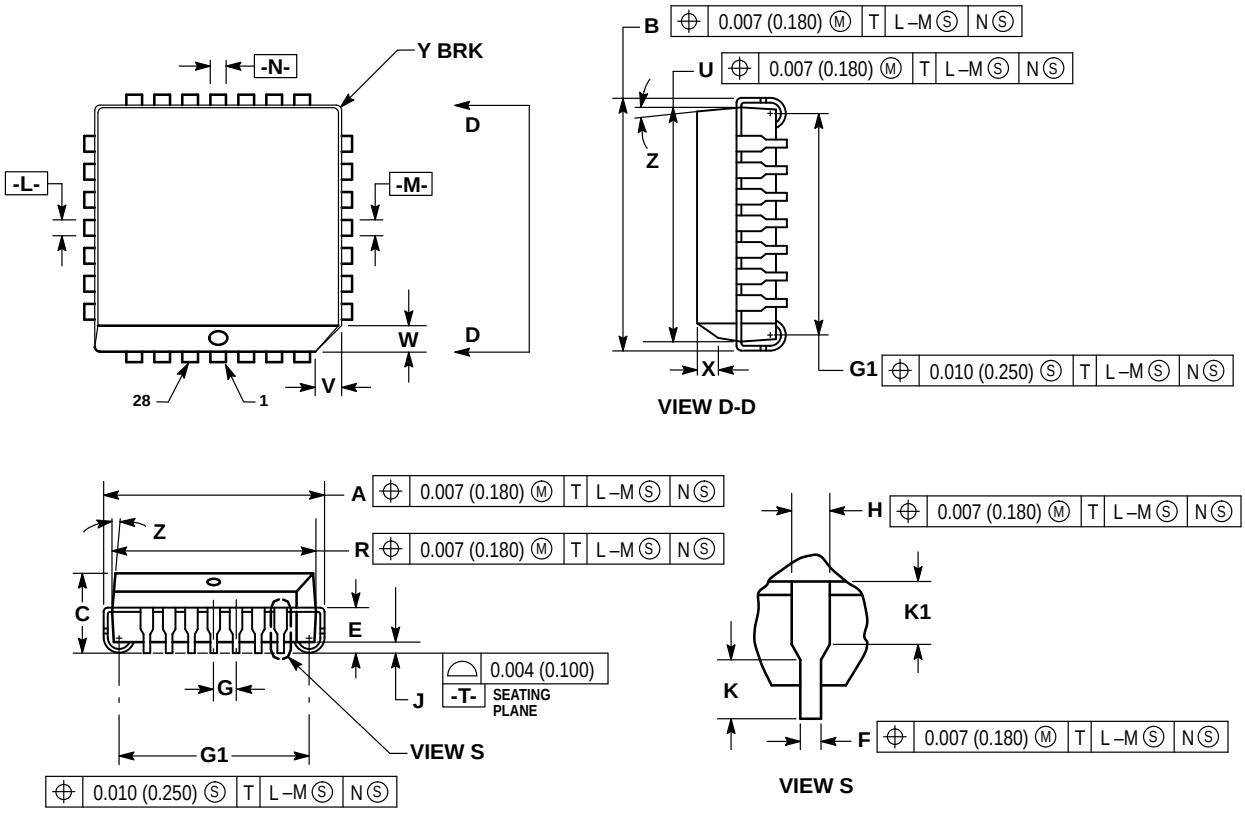
AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{COUNT}	Maximum Count Frequency	1800	2200		1800	2200		1800	2200		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to Q0	1300	1700	2150	1300	1700	2150	1350	1750	2200		
	CLK to Q1	1600	2025	2500	1600	2050	2500	1650	2100	2550		
	CLK to Q2	1950	2425	2925	1950	2450	2925	2025	2500	3000		
	CLK to Q3	2275	2750	3350	2275	2775	3350	2350	2850	3425		
	CLK to Q4	2625	3125	3750	2625	3150	3750	2700	3225	3825		
	CLK to Q5	2950	3450	4150	2950	3475	4150	3050	3550	4250		
	CLK to Q6	3250	3775	4450	3250	3800	4450	3375	3925	4600		
	CLK to Q7	3575	4075	4800	3575	4125	4800	3700	4250	4950		
	A_Start to Q0	950	1325	1700	950	1325	1700	950	1325	1700		
	MR to Q0	700	1000	1300	700	1000	1300	700	1000	1300		
t_S	Setup Time (EN1, EN2)	0	–150		0	–150		0	–150		ps	
t_h	Hold Time (EN1, EN2)	300	150		300	150		300	150		ps	
t_{RR}	Reset Recovery Time										ps	
	MR, A_Start	400	200		400	200		400	200			
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR, A_Start	400			400			400				
V_{PP}	Minimum Input Swing (CLK)	0.25		1.0	0.25		1.0	0.25		1.0	V	Note 1
V_{CMR}	Com Mode Range (CLK)	–0.4		–2.0	–0.4		–2.0	–0.4		–2.0	V	
t_r t_f	Rise/Fall Times										ps	20%–80%
	Q0,Q1	150		400	150		400	150		400		
	Q2 to Q7	275		600	275		600	275		600		

1. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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