

3-Bit Scannable Registered Address Driver

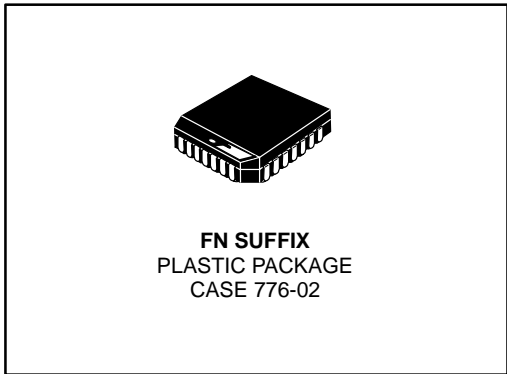
The MC10E/100E212 is a scannable registered ECL driver typically used as a fan-out memory address driver for ECL cache driving. In a VLSI array based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

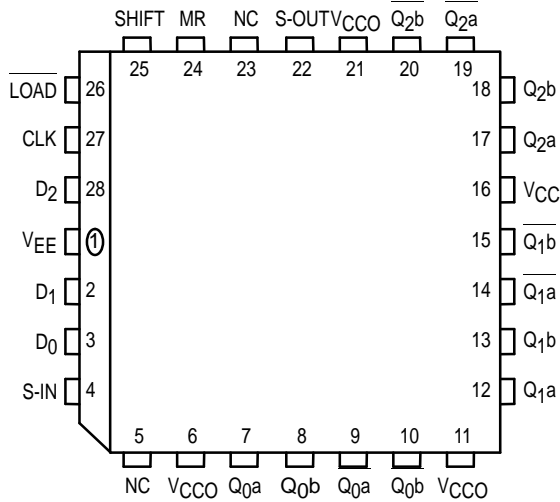
- Scannable Version E112 Driver
- 1025ps Max. CLK to Output
- Dual Differential Outputs
- Master Reset
- Extended 100E V_{EE} Range of - 4.2V to - 5.46V
- Internal 75k Ω Input Pulldown Resistors

MC10E212
MC100E212

3-BIT SCANNABLE REGISTERED ADDRESS DRIVER



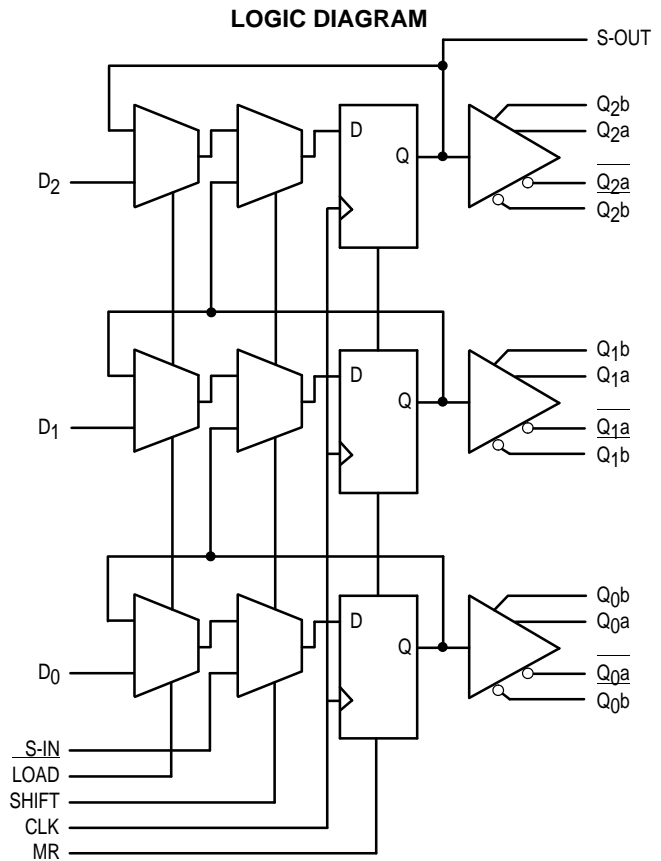
Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CC0} pins are tied together on the die.

PIN NAMES

Pin	Function
$D_0 - D_2$	Data Inputs
S-IN	Scan Input
LOAD	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Reset
S-OUT	Scan Output
$\overline{Q[0:2]a}$, $\overline{Q[0:2]b}$	True Outputs
$Q[0:2]a$, $Q[0:2]b$	Inverting Outputs



MC10E212 MC100E212

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I _{IH}	Input HIGH Current			150			150			150	μA	
I _{EE}	Power Supply Current										mA	
	10E		80	96		80	96		80	96		
	100E		80	96		80	96		92	110		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t _{PLH} t _{PHL}	Propagation Delay to Output CLK MR CLK to S-OUT	575	800	1025	575	800	1025	575	800	1025	ps	
t _s	Setup Time D SHIFT LOAD S-IN	175	25		175	25		175	25			
		150	-50		150	-50		150	-50			
		225	50		225	50		225	50			
t _h	Hold Time D SHIFT LOAD S-IN	250	25		250	25		250	25		ps	
		300	100		300	100		300	100			
		225	0		225	0		225	0			
		300	100		300	100		300	100			
t _{RR}	Reset Recovery	600	350		600	350		600	350		ps	
t _{SKEW}	Within-Device Skew		100			100			100		ps	1
t _{SKEW}	Within-Gate Skew		50			50			50		ps	2
t _r t _f	Rise/Fall Times 20 - 80%	275	425	650	275	425	650	275	425	650	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

FUNCTION TABLE

LOAD	SHIFT	MR	MODE
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

OUTLINE DIMENSIONS


FN SUFFIX
 PLASTIC PLCC PACKAGE
 CASE 776-02
 ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°		10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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