

# SN74LS175

## Quad D Flip-Flop

The LSTTL/MSI SN74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

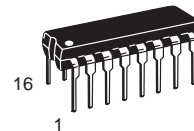
### GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           | Min  | Typ | Max  | Unit |
|-----------------|-------------------------------------|------|-----|------|------|
| V <sub>CC</sub> | Supply Voltage                      | 4.75 | 5.0 | 5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 0    | 25  | 70   | °C   |
| I <sub>OH</sub> | Output Current – High               |      |     | -0.4 | mA   |
| I <sub>OL</sub> | Output Current – Low                |      |     | 8.0  | mA   |

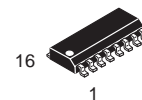


**ON Semiconductor**  
Formerly a Division of Motorola  
<http://onsemi.com>

**LOW  
POWER  
SCHOTTKY**



PLASTIC  
N SUFFIX  
CASE 648



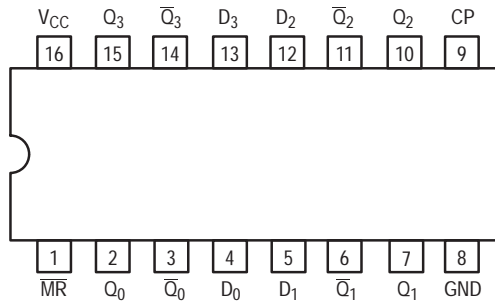
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

| Device     | Package    | Shipping         |
|------------|------------|------------------|
| SN74LS175N | 16 Pin DIP | 2000 Units/Box   |
| SN74LS175D | 16 Pin     | 2500/Tape & Reel |

# SN74LS175

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

|                                   |                                      |
|-----------------------------------|--------------------------------------|
| $D_0 - D_3$                       | Data Inputs                          |
| CP                                | Clock (Active HIGH Going Edge) Input |
| $\overline{MR}$                   | Master Reset (Active LOW) Input      |
| $Q_0 - Q_3$                       | True Outputs                         |
| $\overline{Q}_0 - \overline{Q}_3$ | Complemented Outputs                 |

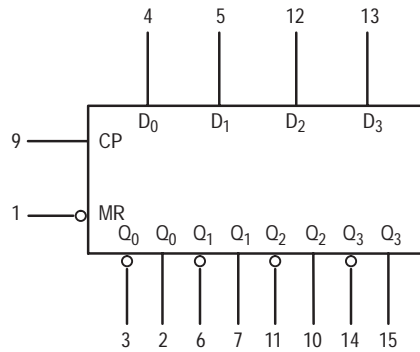
### LOADING (Note a)

|                                   | HIGH     | LOW       |
|-----------------------------------|----------|-----------|
| $D_0 - D_3$                       | 0.5 U.L. | 0.25 U.L. |
| CP                                | 0.5 U.L. | 0.25 U.L. |
| $\overline{MR}$                   | 0.5 U.L. | 0.25 U.L. |
| $Q_0 - Q_3$                       | 10 U.L.  | 5 U.L.    |
| $\overline{Q}_0 - \overline{Q}_3$ | 10 U.L.  | 5 U.L.    |

### NOTES:

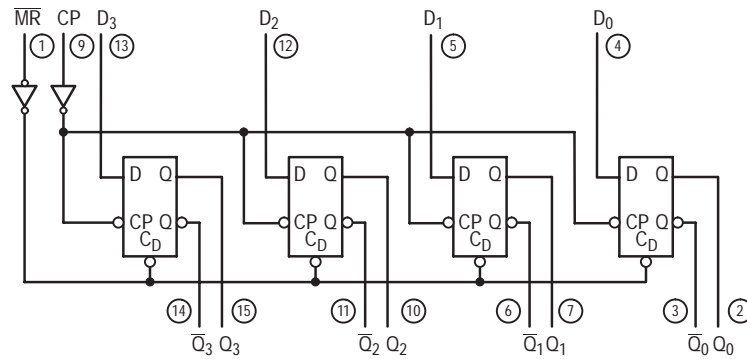
a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

### LOGIC DIAGRAM



$V_{CC}$  = PIN 16  
GND = PIN 8

○ = PIN NUMBERS

## SN74LS175

### FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and  $\bar{Q}$  outputs to

follow. A LOW input on the Master Reset ( $\overline{MR}$ ) will force all Q outputs LOW and  $\bar{Q}$  outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

**TRUTH TABLE**

| Inputs (t = n, $\overline{MR}$ = H) | Outputs (t = n+1) Note 1 |           |
|-------------------------------------|--------------------------|-----------|
| D                                   | Q                        | $\bar{Q}$ |
| L                                   | L                        | H         |
| H                                   | H                        | L         |

Note 1: t = n + 1 indicates conditions after next clock.

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                      | Limits |       |      | Unit | Test Conditions   |
|-----------------|--------------------------------|--------|-------|------|------|---|
|                 |                                | Min    | Typ   | Max  |      |   |
| V <sub>IH</sub> | Input HIGH Voltage             | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs  |
| V <sub>IL</sub> | Input LOW Voltage              |        |       | 0.8  | V    | Guaranteed Input LOW Voltage for All Inputs   |
| V <sub>IK</sub> | Input Clamp Diode Voltage      |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub> | Output HIGH Voltage            | 2.7    | 3.5   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table                            |
| V <sub>OL</sub> | Output LOW Voltage             |        | 0.25  | 0.4  | V    | I <sub>OL</sub> = 4.0 mA<br>V <sub>CC</sub> = V <sub>CC</sub> MIN,<br>V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>per Truth Table |
|                 |                                |        | 0.35  | 0.5  | V    |   |
| I <sub>IH</sub> | Input HIGH Current             |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V  |
|                 |                                |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V  |
| I <sub>IL</sub> | Input LOW Current              |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V  |
| I <sub>OS</sub> | Short Circuit Current (Note 1) | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX   |
| I <sub>CC</sub> | Power Supply Current           |        |       | 18   | mA   | V <sub>CC</sub> = MAX   |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS175

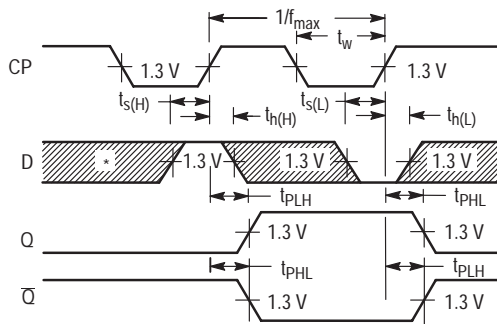
## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

| Symbol                               | Parameter                                    | Limits |          |          | Unit | Test Conditions                                   |
|--------------------------------------|--|--------|----------|----------|------|---|
|                                      |  | Min    | Typ      | Max      |      |   |
| f <sub>MAX</sub>                     | Maximum Input Clock Frequency                | 30     | 40       |          | MHz  | V <sub>CC</sub> = 5.0 V<br>C <sub>L</sub> = 15 pF |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay, $\overline{MR}$ to Output |        | 20<br>20 | 30<br>30 | ns   |   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay, Clock to Output           |        | 13<br>16 | 25<br>25 | ns   |   |

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

| Symbol           | Parameter                            | Limits |     |     | Unit | Test Conditions         |
|------------------|--------------------------------------|--------|-----|-----|------|-------------------------|
|                  |                                      | Min    | Typ | Max |      |                         |
| t <sub>W</sub>   | Clock or $\overline{MR}$ Pulse Width | 20     |     |     | ns   | V <sub>CC</sub> = 5.0 V |
| t <sub>s</sub>   | Data Setup Time                      | 20     |     |     | ns   |                         |
| t <sub>h</sub>   | Data Hold Time                       | 5.0    |     |     | ns   |                         |
| t <sub>rec</sub> | Recovery Time                        | 25     |     |     | ns   |                         |

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

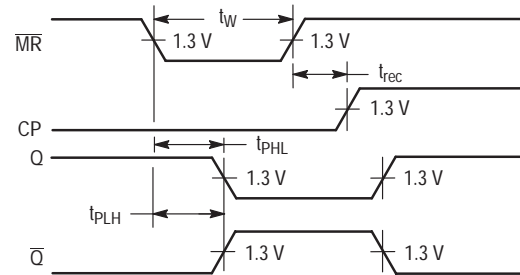


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

## DEFINITIONS OF TERMS

**SETUP TIME (t<sub>s</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>h</sub>)** — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

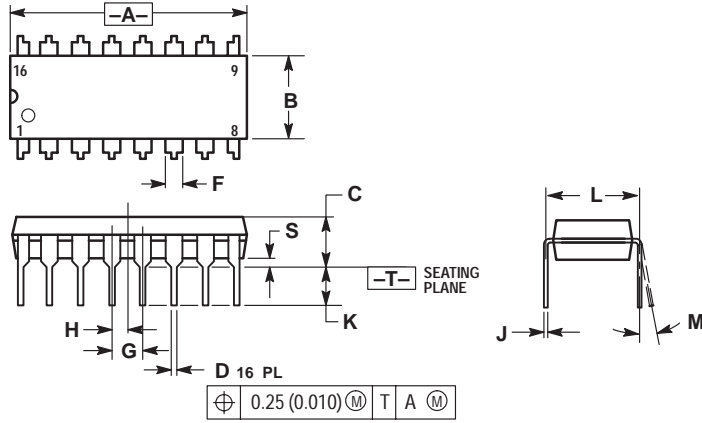
continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

**RECOVERY TIME (t<sub>rec</sub>)** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

# SN74LS175

## PACKAGE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



**NOTES:**

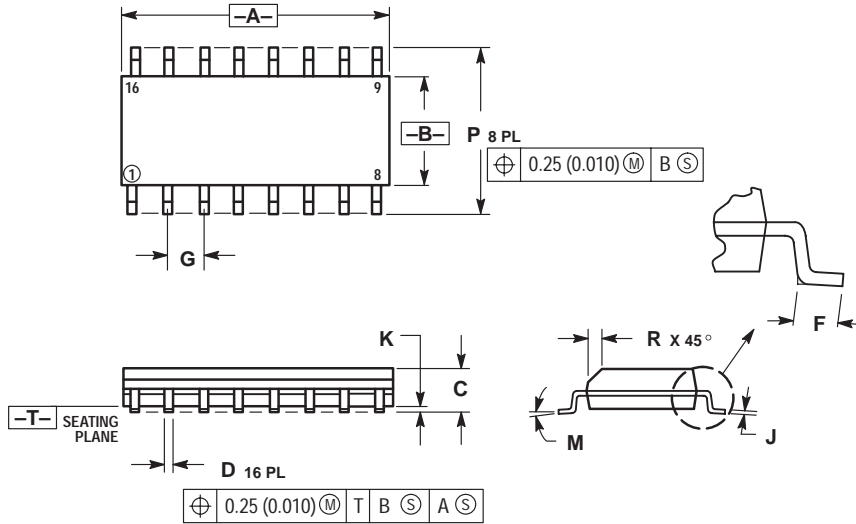
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        |       | 10°         |       |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

# SN74LS175

## PACKAGE DIMENSIONS

**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751B-05  
 ISSUE J




**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

**Notes**

# SN74LS175

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### North America Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

### EUROPE: LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M-F 2:30pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M-F 2:30pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M-F 1:30pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

### ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong 800-4422-3781  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

**Phone:** 81-3-5487-8345  
**Email:** r14153@onsemi.com

**Fax Response Line:** 303-675-2167  
800-344-3810 Toll Free USA/Canada

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local  
Sales Representative.

SN74LS175/D