

# MC10EP35

## JK Flip Flop

The MC10EP35 is a higher speed/low voltage version of the EL35 JK flip flop. The J/K data enters the master portion of the flip flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

- 300ps Propagation Delay
- High Bandwidth to 3 GHz Typical
- High Bandwidth Output Transistors
- PECL mode: 3.0V to 5.5V  $V_{CC}$  with  $V_{EE} = 0V$
- ECL mode: 0V  $V_{CC}$  with  $V_{EE} = -3.0V$  to  $-5.5V$
- 75k $\Omega$  Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at  $V_{EE}$
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.  
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 77 devices

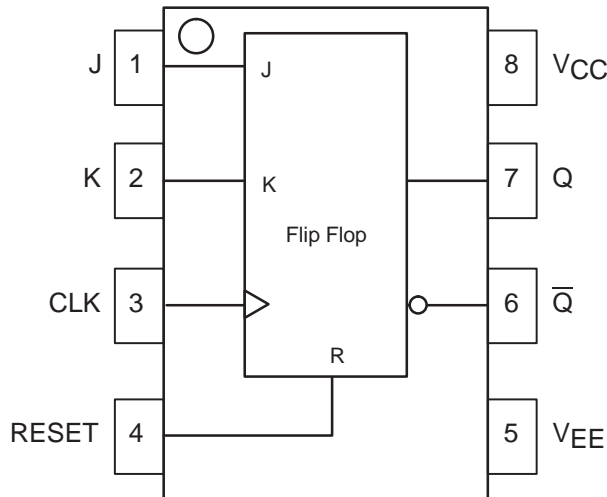
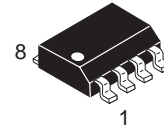


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

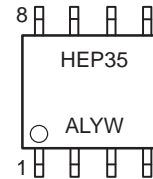


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**SO-8**  
**D SUFFIX**  
**CASE 751**

### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

### PIN DESCRIPTION

PIN	FUNCTION
CLK	ECL Clock Inputs
J, K	ECL Signal Inputs
RESET	ECL Asynchronous Reset
Q, $\bar{Q}$	ECL Data Outputs

### TRUTH TABLE

J	K	RESET	CLK	Q <sub>n+1</sub>
L	L	L	Z	Q <sub>n</sub>
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	$\bar{Q}_n$
X	X	H	X	L

Z = LOW to HIGH Transition

### ORDERING INFORMATION

Device	Package	Shipping
MC10EP35D	SOIC	98 Units/Rail
MC10EP35DR2	SOIC	2500 Tape & Reel

# MC10EP35

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0V$ )	-6.0 to 0	VDC
$V_{CC}$	Power Supply ( $V_{EE} = 0V$ )	6.0 to 0	VDC
$V_I$	Input Voltage ( $V_{CC} = 0V$ , $V_I$ not more negative than $V_{EE}$ )	-6.0 to 0	VDC
$V_I$	Input Voltage ( $V_{EE} = 0V$ , $V_I$ not more positive than $V_{CC}$ )	6.0 to 0	VDC
$I_{out}$	Output Current Continuous Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%	°C/W
$T_{sol}$	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

## DC CHARACTERISTICS, ECL/LVECL ( $V_{CC} = 0V$ ; $V_{EE} = -5.5V$ to $-3.0V$ ) (Note 3.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	30	40	50	30	40	50	30	40	50	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1.  $V_{CC} = 0V$ ,  $V_{EE} = V_{EEmin}$  to  $V_{EEmax}$ , all other pins floating.
2. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.
3. Input and output parameters vary 1:1 with  $V_{CC}$ .

# MC10EP35

## DC CHARACTERISTICS, LVPECL ( $V_{CC} = 3.3V \pm 0.3V$ , $V_{EE} = 0V$ ) (Note 6.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 4.)	30	40	50	30	40	50	30	40	50	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V <sub>OL</sub>	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V <sub>IH</sub>	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V <sub>IL</sub>	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4.  $V_{CC} = 3.3V$ ,  $V_{EE} = 0V$ , all other pins floating.

5. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .

## DC CHARACTERISTICS, PECL ( $V_{CC} = 5.0V \pm 0.5V$ , $V_{EE} = 0V$ ) (Note 9.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 7.)	30	40	50	30	40	50	30	40	50	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V <sub>OL</sub>	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V <sub>IH</sub>	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V <sub>IL</sub>	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7.  $V_{CC} = 5.0V$ ,  $V_{EE} = 0V$ , all other pins floating.

8. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .

# MC10EP35

## AC CHARACTERISTICS ( $V_{CC} = 0V$ ; $V_{EE} = -3.0V$ to $-5.5V$ ) or ( $V_{CC} = 3.0V$ to $5.5V$ ; $V_{EE} = 0V$ )

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>max</sub>	Maximum Toggle Frequency (Note 10.)		3.0			3.0			3.0		GHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay to Output Diff. R, CLK→Q, $\bar{Q}$	150	300	450	170	320	470	180	330	480	ps
t <sub>RR</sub>	Set/Reset Recovery		TBD			TBD			TBD		ps
t <sub>S</sub> t <sub>H</sub>	Setup Time Hold Time	150 200	0 100		150 200	0 100		150 200	0 100		ps
t <sub>SKEW</sub>	Duty Cycle Skew (Note 11.) Skew Part-to-Part		TBD TBD			TBD TBD			TBD TBD		ps
t <sub>PW</sub>	Minimum Pulse Width CLK, RESET		400			400			400		ps
t <sub>JITTER</sub>	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times (20% – 80%) Q, $\bar{Q}$	50	110	180	60	120	200	70	140	220	ps

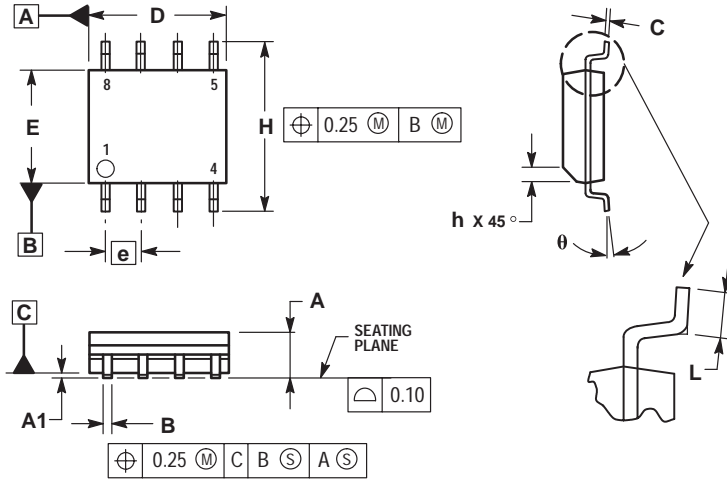
10. F<sub>max</sub> guaranteed for functionality only. V<sub>OL</sub> and V<sub>OH</sub> levels are guaranteed at DC only.

11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

# MC10EP35

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-06  
ISSUE T



### NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

**Notes**

**Notes**

# MC10EP35

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