

# MC14049B, MC14050B

## Hex Buffer

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage,  $V_{DD}$ .

The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{DD}$  supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS-to-TTL/DTL converter ( $V_{DD} = 5.0\text{ V}$ ,  $V_{OL} \leq 0.4\text{ V}$ ,  $I_{OL} \geq 3.2\text{ mA}$ ).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- $V_{IN}$  can exceed  $V_{DD}$
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

| Symbol    | Parameter   | Value                  | Unit               |
|-----------|---|------------------------|--------------------|
| $V_{DD}$  | DC Supply Voltage Range                                   | -0.5 to +18.0          | V                  |
| $V_{in}$  | Input Voltage Range (DC or Transient)                     | -0.5 to +18.0          | V                  |
| $V_{out}$ | Output Voltage Range (DC or Transient)                    | -0.5 to $V_{DD} + 0.5$ | V                  |
| $I_{in}$  | Input Current (DC or Transient) per Pin                   | $\pm 10$               | mA                 |
| $I_{out}$ | Output Current (DC or Transient) per Pin                  | $\pm 45$               | mA                 |
| $P_D$     | Power Dissipation, per Package (Note 3.) (Plastic) (SOIC) | 825<br>740             | mW                 |
| $T_A$     | Ambient Temperature Range                                 | -55 to +125            | $^{\circ}\text{C}$ |
| $T_{stg}$ | Storage Temperature Range                                 | -65 to +150            | $^{\circ}\text{C}$ |
| $T_L$     | Lead Temperature (8-Second Soldering)                     | 260                    | $^{\circ}\text{C}$ |

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating: See Figure 3.

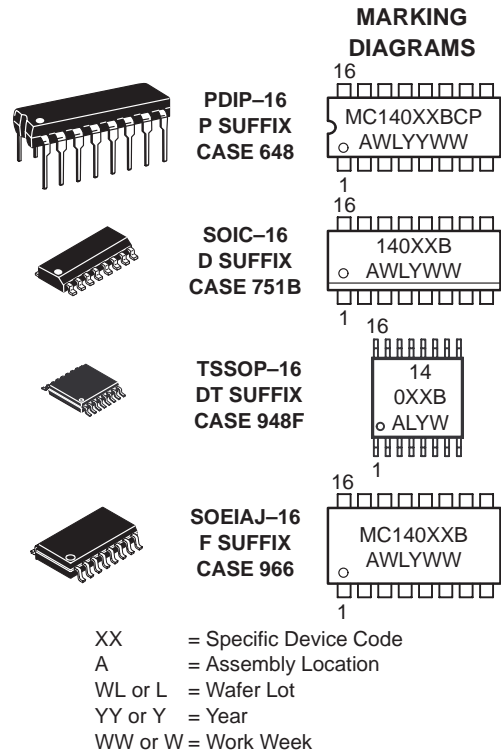
This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the  $V_{SS}$  pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $V_{SS} \leq V_{in} \leq 18\text{ V}$  and  $V_{SS} \leq V_{out} \leq V_{DD}$  are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor

<http://onsemi.com>



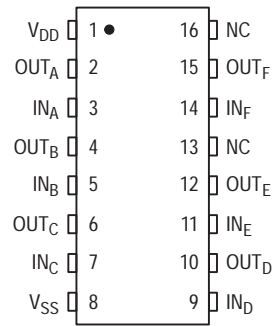
### ORDERING INFORMATION

| Device       | Package   | Shipping         |
|--------------|-----------|------------------|
| MC14049BCP   | PDIP-16   | 2000/Box         |
| MC14049BD    | SOIC-16   | 2400/Box         |
| MC14049BDR2  | SOIC-16   | 2500/Tape & Reel |
| MC14049BF    | SOEIAJ-16 | See Note 1.      |
| MC14050BCP   | PDIP-16   | 2000/Box         |
| MC14050BD    | SOIC-16   | 2400/Box         |
| MC14050BDR2  | SOIC-16   | 2500/Tape & Reel |
| MC14050BDTEL | TSSOP-16  | 2000/Tape & Reel |
| MC14050BF    | SOEIAJ-16 | See Note 1.      |
| MC14050BFEL  | SOEIAJ-16 | See Note 1.      |

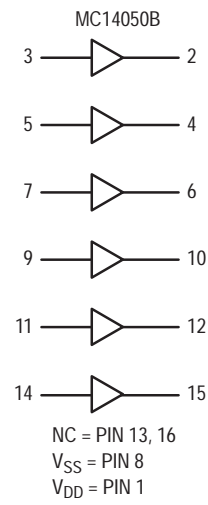
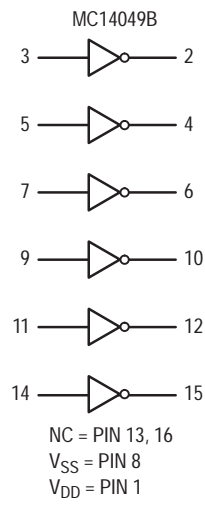
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# MC14049B, MC14050B

## PIN ASSIGNMENT



## LOGIC DIAGRAM



## MC14049B, MC14050B

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

| Characteristic  | Symbol                           | V <sub>DD</sub><br>Vdc | - 55°C  |       | + 25°C |          |       | + 125°C |       | Unit |
|---|----------------------------------|------------------------|---|-------|--------|----------|-------|---------|-------|------|
|   |                                  |                        | Min   | Max   | Min    | Typ (4.) | Max   | Min     | Max   |      |
| Output Voltage<br>V <sub>in</sub> = V <sub>DD</sub><br><br>V <sub>in</sub> = 0  | "0" Level<br><br>V <sub>OL</sub> | 5.0                    | —   | 0.05  | —      | 0        | 0.05  | —       | 0.05  | Vdc  |
|   |                                  | 10                     | —   | 0.05  | —      | 0        | 0.05  | —       | 0.05  |      |
|   |                                  | 15                     | —   | 0.05  | —      | 0        | 0.05  | —       | 0.05  |      |
|   | "1" Level<br><br>V <sub>OH</sub> | 5.0                    | 4.95  | —     | 4.95   | 5.0      | —     | 4.95    | —     | Vdc  |
|   |                                  | 10                     | 9.95  | —     | 9.95   | 10       | —     | 9.95    | —     |      |
|   |                                  | 15                     | 14.95   | —     | 14.95  | 15       | —     | 14.95   | —     |      |
| Input Voltage<br>(V <sub>O</sub> = 4.5 Vdc)<br>(V <sub>O</sub> = 9.0 Vdc)<br>(V <sub>O</sub> = 13.5 Vdc)<br><br>(V <sub>O</sub> = 0.5 Vdc)<br>(V <sub>O</sub> = 1.0 Vdc)<br>(V <sub>O</sub> = 1.5 Vdc)              | "0" Level<br><br>V <sub>IL</sub> | 5.0                    | —   | 1.5   | —      | 2.25     | 1.5   | —       | 1.5   | Vdc  |
|   |                                  | 10                     | —   | 3.0   | —      | 4.50     | 3.0   | —       | 3.0   |      |
|   |                                  | 15                     | —   | 4.0   | —      | 6.75     | 4.0   | —       | 4.0   |      |
|   | "1" Level<br><br>V <sub>IH</sub> | 5.0                    | 3.5   | —     | 3.5    | 2.75     | —     | 3.5     | —     | Vdc  |
|   |                                  | 10                     | 7.0   | —     | 7.0    | 5.50     | —     | 7.0     | —     |      |
|   |                                  | 15                     | 11  | —     | 11     | 8.25     | —     | 11      | —     |      |
| Output Drive Current<br>(V <sub>OH</sub> = 2.5 Vdc)<br>(V <sub>OH</sub> = 9.5 Vdc)<br>(V <sub>OH</sub> = 13.5 Vdc)<br><br>(V <sub>OL</sub> = 0.4 Vdc)<br>(V <sub>OL</sub> = 0.5 Vdc)<br>(V <sub>OL</sub> = 1.5 Vdc) | Source<br><br>I <sub>OH</sub>    | 5.0                    | -1.6  | —     | -1.25  | -2.5     | —     | -1.0    | —     | mAdc |
|   |                                  | 10                     | -1.6  | —     | -1.30  | -2.6     | —     | -1.0    | —     |      |
|   |                                  | 15                     | -4.7  | —     | -3.75  | -10      | —     | -3.0    | —     |      |
|   | Sink<br><br>I <sub>OL</sub>      | 5.0                    | 3.75  | —     | 3.2    | 6.0      | —     | 2.6     | —     | mAdc |
|   |                                  | 10                     | 10  | —     | 8.0    | 16       | —     | 6.6     | —     |      |
|   |                                  | 15                     | 30  | —     | 24     | 40       | —     | 19      | —     |      |
| Input Current   | I <sub>in</sub>                  | 15                     | —   | ± 0.1 | —      | ±0.00001 | ± 0.1 | —       | ± 1.0 | μAdc |
| Input Capacitance (V <sub>in</sub> = 0)   | C <sub>in</sub>                  | —                      | —   | —     | —      | 10       | 20    | —       | —     | pF   |
| Quiescent Current (Per Package)   | I <sub>DD</sub>                  | 5.0                    | —   | 1.0   | —      | 0.002    | 1.0   | —       | 30    | μAdc |
|   |                                  | 10                     | —   | 2.0   | —      | 0.004    | 2.0   | —       | 60    |      |
|   |                                  | 15                     | —   | 4.0   | —      | 0.006    | 4.0   | —       | 120   |      |
| Total Supply Current (5.) (6.)<br>(Dynamic plus Quiescent,<br>per package)<br>(C <sub>L</sub> = 50 pF on all outputs, all<br>buffers switching)   | I <sub>T</sub>                   | 5.0                    | I <sub>T</sub> = (1.8 μA/kHz) f + I <sub>DD</sub><br>I <sub>T</sub> = (3.5 μA/kHz) f + I <sub>DD</sub><br>I <sub>T</sub> = (5.3 μA/kHz) f + I <sub>DD</sub> |       |        |          |       |         |       | μAdc |

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at + 25°C

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

Where: I<sub>T</sub> is in μA (per Package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency and k = 0.002.

## MC14049B, MC14050B

### AC SWITCHING CHARACTERISTICS <sup>(7.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = +25^\circ\text{C}$ )

| Characteristic   | Symbol    | $V_{DD}$<br>Vdc | Min         | Typ <sup>(8.)</sup> | Max             | Unit |
|--|-----------|-----------------|-------------|---------------------|-----------------|------|
| Output Rise Time<br>$t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$<br>$t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$<br>$t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$           | $t_{TLH}$ | 5.0<br>10<br>15 | —<br>—<br>— | 100<br>50<br>40     | 160<br>80<br>60 | ns   |
| Output Fall Time<br>$t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$<br>$t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$<br>$t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$            | $t_{THL}$ | 5.0<br>10<br>15 | —<br>—<br>— | 40<br>20<br>15      | 60<br>40<br>30  | ns   |
| Propagation Delay Time<br>$t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$<br>$t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$<br>$t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$ | $t_{PLH}$ | 5.0<br>10<br>15 | —<br>—<br>— | 80<br>40<br>30      | 140<br>80<br>60 | ns   |
| Propagation Delay Time<br>$t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$<br>$t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$<br>$t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$     | $t_{PHL}$ | 5.0<br>10<br>15 | —<br>—<br>— | 40<br>20<br>15      | 80<br>40<br>30  | ns   |

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

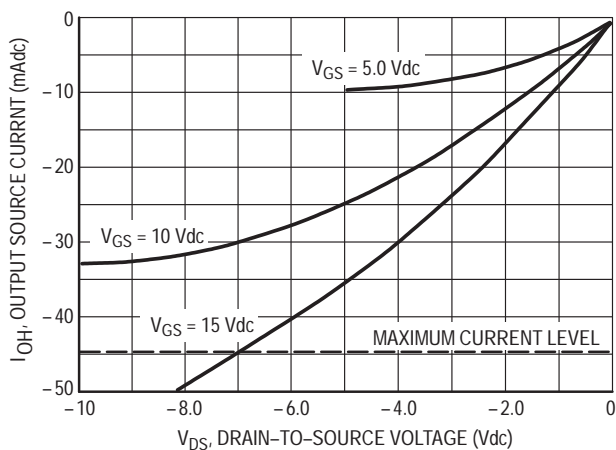
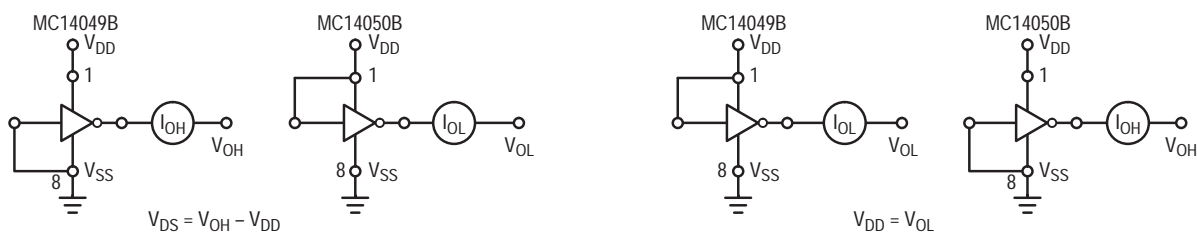


Figure 1. Typical Output Source Characteristics

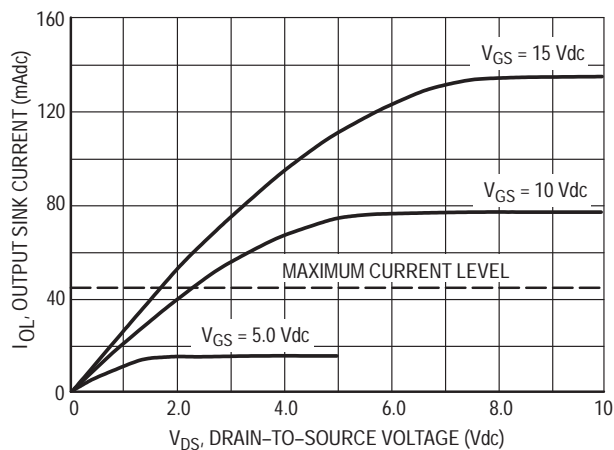


Figure 2. Typical Output Sink Characteristics

## MC14049B, MC14050B

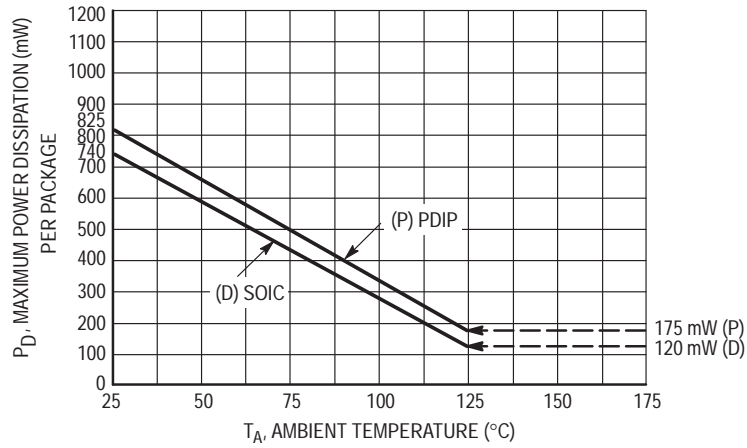


Figure 3. Ambient Temperature Power Derating

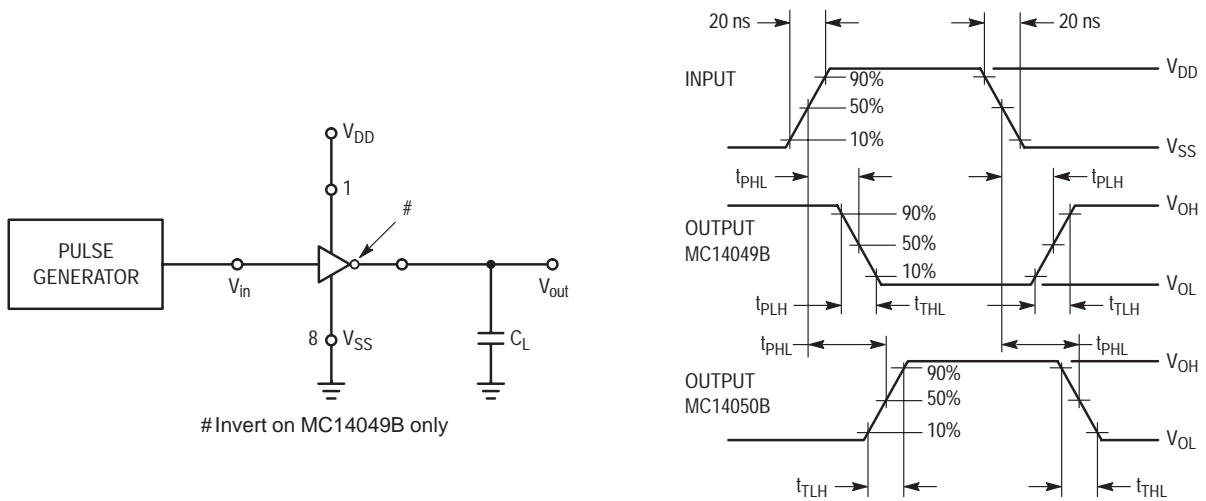
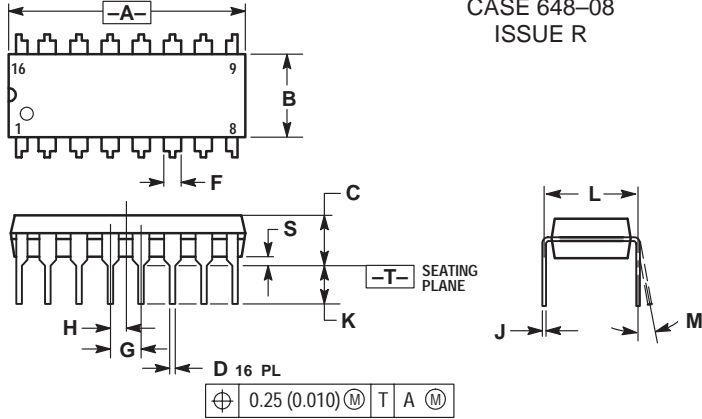


Figure 4. Switching Time Test Circuit and Waveforms

# MC14049B, MC14050B

## PACKAGE DIMENSIONS

### PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

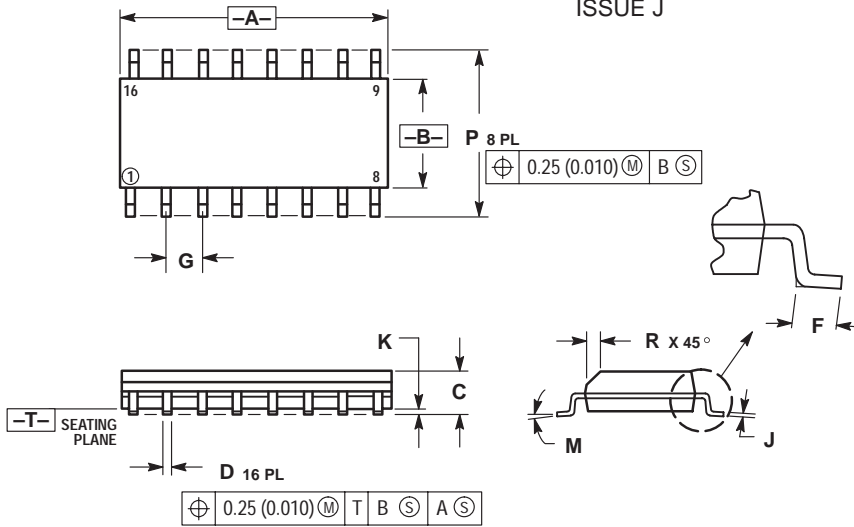


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

### SOIC-16 D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

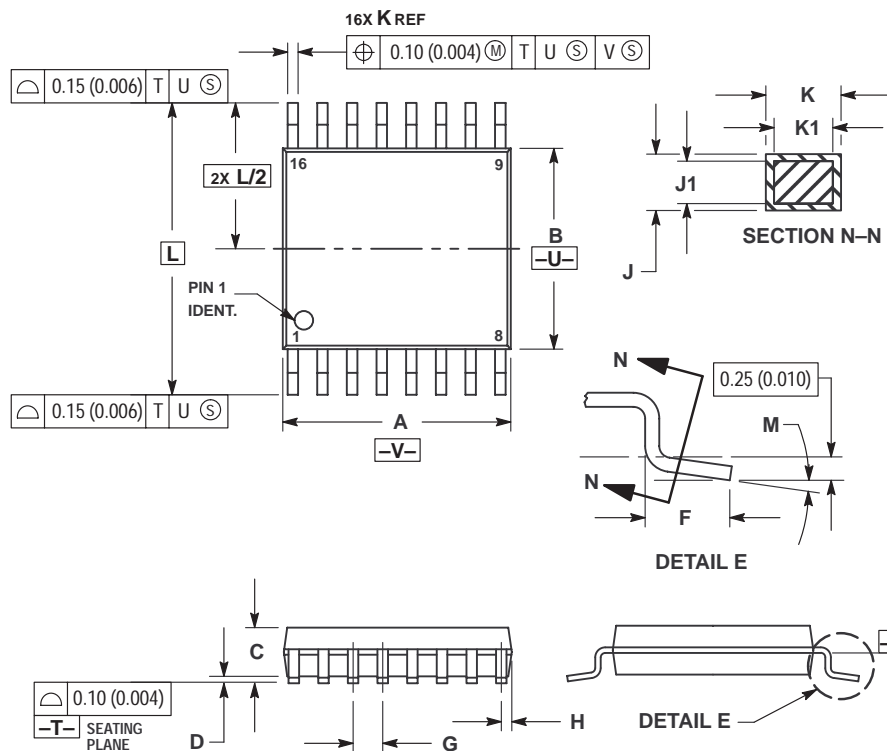
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

# MC14049B, MC14050B

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948F-01  
ISSUE O



### NOTES:

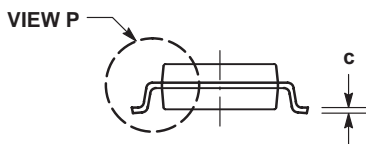
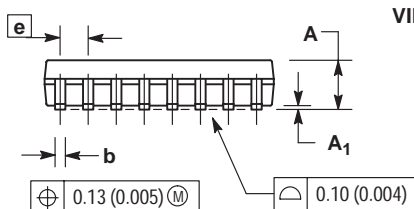
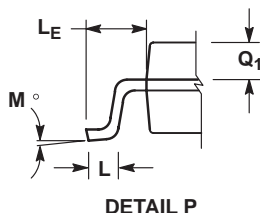
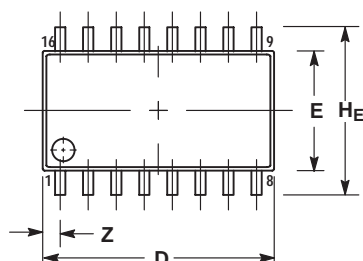
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

# MC14049B, MC14050B

## PACKAGE DIMENSIONS


SOEIAJ-16  
F SUFFIX  
PLASTIC EIAJ SOIC PACKAGE  
CASE 966-01  
ISSUE O



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

### PUBLICATION ORDERING INFORMATION

#### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

#### EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)  
Email: ONlit\_german@hibbertco.com  
French Phone: (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)  
Email: ONlit\_french@hibbertco.com  
English Phone: (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)  
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781

\*Available from Germany, France, Italy, England, Ireland

#### CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
Email: ONlit-spanish@hibbertco.com

#### ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
001-800-4422-3781  
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
Phone: 81-3-5740-2745  
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.