

# MC74HCT14A

## Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

### High-Performance Silicon-Gate CMOS

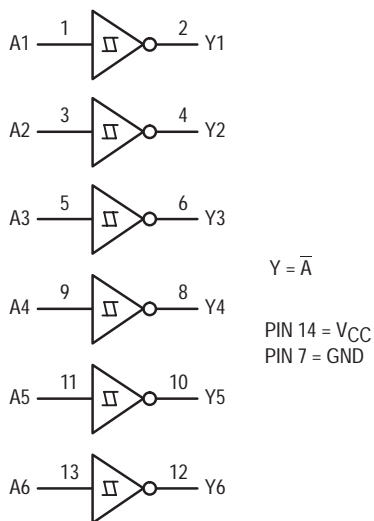
The MC74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The HCT14A is identical in pinout to the LS14.

The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

#### LOGIC DIAGRAM



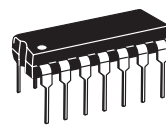
#### FUNCTION TABLE

Input A	Output Y
L	H
H	L



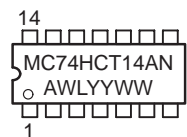
**ON Semiconductor**

<http://onsemi.com>

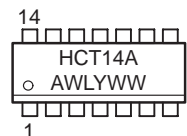


**PDIP-14  
N SUFFIX  
CASE 646**

#### MARKING DIAGRAMS

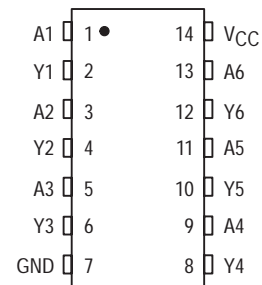


**SOIC-14  
D SUFFIX  
CASE 751A**



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

Device	Package	Shipping
MC74HCT14AN	PDIP-14	2000 / Box
MC74HCT14AD	SOIC-14	55 / Rail
MC74HCT14ADR2	SOIC-14	2500 / Reel

# MC74HCT14A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	—	*	ns

\*No Limit when  $V_{in} \approx 50\% V_{CC}$ ,  $I_{CC} > 1 \text{ mA}$ .

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ Volts	Temperature Limit						Unit
				- 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
$V_{T+ \text{ max}}$	Maximum Positive-Going Input Threshold Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
$V_{T+ \text{ min}}$	Minimum Positive-Going Input Threshold Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
$V_{T- \text{ max}}$	Maximum Positive-Going Input Threshold Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
$V_{T- \text{ min}}$	Minimum Positive-Going Input Threshold Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
$V_H \text{ max}$	Maximum Hysteresis Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
$V_H \text{ min}$	Minimum Hysteresis Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0.4		
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} < V_{T- \text{ min}}$ $ I_{out}  \leq 20 \mu\text{A}$	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		$V_{in} < V_{T- \text{ min}}$ $ I_{out}  \leq 4.0 \text{ mA}$	4.5	3.98		3.84		3.7		

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).  
(continued)

# MC74HCT14A

## DC CHARACTERISTICS (Voltages Referenced to GND) – continued

Symbol	Parameter	Test Conditions	V <sub>CC</sub> Volts	Temperature Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> ≥ V <sub>T+max</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		V <sub>in</sub> ≥ V <sub>T+max</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5		0.26		0.33		0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5		± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5		1.0		10		40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5		≥ – 55°C		25°C to 125°C			mA
					2.9	2.4				

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	Test Conditions		Guaranteed Limit						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (L to H)	V <sub>CC</sub> = 5.0 V ± 10% C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns	Fig. 1 & 2		32		40		48	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time. Any Output	V <sub>CC</sub> = 5.0 V ± 10% C <sub>L</sub> = 50 pF, Input t <sub>r</sub> = t <sub>f</sub> = 6.0 ns	Fig. 1 & 2		15		19		22	ns

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Inverter)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		32		

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

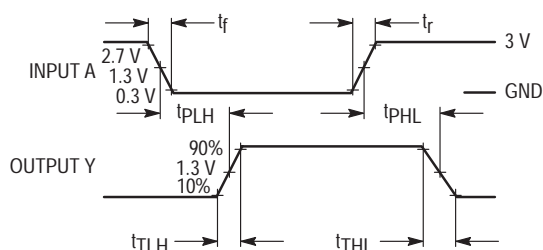
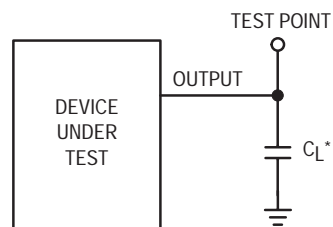


Figure 1. Switching Waveforms



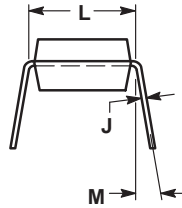
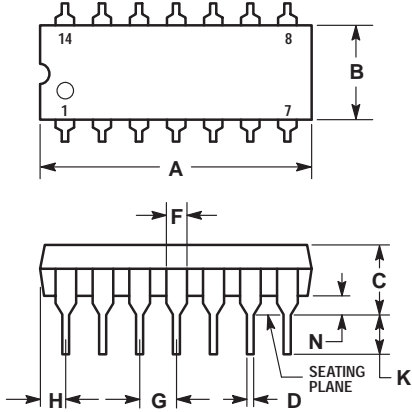
\*Includes all probe and jig capacitance

Figure 2. Test Circuit

# MC74HCT14A

## PACKAGE DIMENSIONS

**PDIP-14**  
**N SUFFIX**  
 CASE 646-06  
 ISSUE L

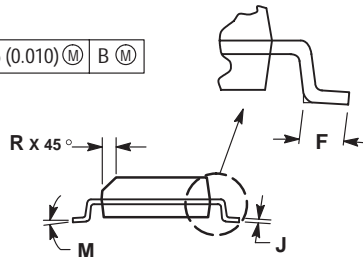
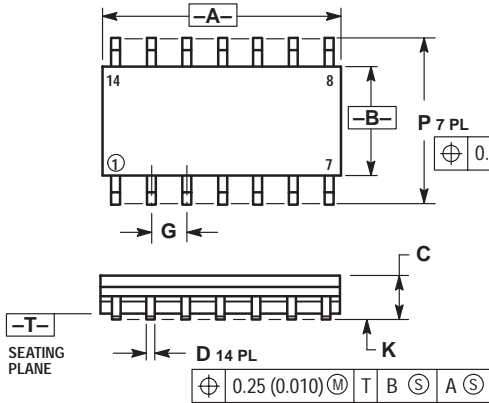


**NOTES:**

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**SOIC-14**  
**D SUFFIX**  
 CASE 751A-03  
 ISSUE F



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

**Notes**

**Notes**

**Notes**

# MC74HCT14A

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### **NORTH AMERICA Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

### **EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, England, Ireland

### **CENTRAL/SOUTH AMERICA:**

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

### **ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.